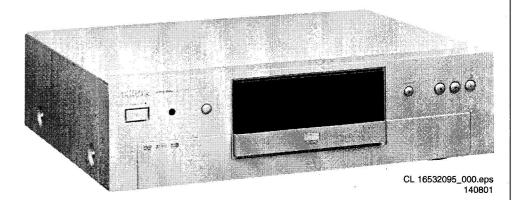
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1967

Technical Specifications and Connection Facilities

General: 1.1 and PHILIPS standard test pattern video signal: -60 dB unweighted Harmonic distortion (1 kHz): : 0.1 % Mains voltage : 230V (198 -264V AC) for Europe/Asia Mains frequency 1.2.7 Tuning 50 Hz - 60Hz Power consumption mains < 32 W Power consumption standby < 7 W **Automatic Search Tuning** Power consumption low power scanning time without antenna : 2.5 min. PAL stand-by : < 3 W stop level (vision carrier) 75 V, 75 Maximum tuning error of a recalled program : ± 62.5 kHz **RF Tuner** 1.2 Maximum tuning error during operation : ± 100 kHz Test equipment:Fluke 54200 TV Signal generator Test streams:PAL BG Philips Standard test pattern **Tuning Principle** automatic B,G, I, DK and L/L'detection 1.2.1 System: manual selection in "STORE" mode PAL B/G, PAL D/K, SECAM L/L', PAL I 1.3 **Analogue Inputs** 1.2.2 RF - Loop Through: SCART II (Connected to TV) 1.3.1 Frequency range : 45 MHz - 860 MHz Pin Signals: Gain: (ANT IN - ANT OUT) : -4 dB /±2 dB 1 - Audio R 1.8V RMS 2 - Audio R 1.2.3 Radio Interference: 3 - Audio L **1.8V RMS** 4 - Audio GND input voltage /3 tone method (+40 5 - Blue/Chroma : typ. 80 dB_µV at **GND** 75Ω 6 - Audio L • 7 - Blue out/ 1.2.4 Receiver: **⊕** Chroma in $0.7Vpp \pm 0.1V$ into 75 Ohm (*) - Function PLL tuning with AFC for optimum reception switch <2V = TV>4.5V / <7V = asp. ratio 16:9 DVD Frequency range: : 45.25 MHz - 860 MHz >9.5V / <12V = asp. ratio 4:3﴾ Sensitivity at 40 dB S/N DVD : \geq 60dBµV at 75Ω 9 - Green GND 10- P50 control (video unweighted) 11- Green 0.7Vpp ± 0.1V into 75 Ohm (*) 12- Nc **Video Performance:** 13- Red/Chroma **GND** Channel 25 / 503,25 MHz, 14- fast switch Test pattern: PAL BG PHILIPS standard test pattern. GND RF Level 74 dBV 15- Red out/ Measured on SCART 1 Chroma out 0.7Vpp ± 0.1V into 75 Ohm (*) Frequency response: : 1 MHz - 4.00 MHz \bigcirc ± 3dB 0.3Vpp Chroma (burst) + 2 dB 16- fast switch Group delay (0.1 MHz - 4.4 MHz) : 0 nsec ± 30 nsec RGB/ CVBS or Y <0.4V into 75 Ohm = CVBS >1V / <3V into 75 Ohm = RGB ➾ 1.2.6 Audio Performance: 17-Y/CVBS **GND** Audio Performance Analogue - HiFi: 18- fast switching Frequency response at SCART 1 **GND** (L+R) output: : 40 Hz - 15 kHz / ± 19-CVBS/Y/RGB 1.5 dB sync 1Vpp ± 0.1V into 75 Ohm (*) S/N according to DIN 45405, 7, 20- CVBS/Y 21- Shield and PHILIPS standard test pattern video signal: : -50 dB unweighted 1.3.2 SCART I (Connected to AUX) Harmonic distortion (1 kHz, ± 25 kHz deviation): : 0.5 % Pin Signals: 1 - Audio R **1.8V RMS** Audio Performance NICAM: 2 - Audio R Frequency response at SCART 3 - Audio L 1.8V RMS 1(L+R) output: : 40 Hz - 15 kHz ± 1.5 4 - Audio GND dB 5 - Blue/Chroma S/N according to DIN 45405, 7,

GND

	6 - Audio L		\odot		SNR Chrominance PM	: > -65 dB
	7 - Blue in/ Chroma out ± 3dB 0.3\	/pp Chroma (burst)	→		Bandwidth Luminance	: 5 MHz ± 1 dB
	8 - Function switch	,	(1.4.2	YC Output Rear (Hosiden ; EXT3)
	9 - Green GND		⊕⊸₊⊕		CNID	05 10
	10- P50 control		⊕		SNR SNR C - AM	: > -65 dB : > -65 dB
	11- Green		€)		SNR C - PM	: > -65 dB
	12- Nc				Bandwidth Y	: 5 MHz ± 1 dB
	13- Red/Chroma GND		1			
	14- fast switch		÷	1.4.3	SCART (RGB)	
	GND		Ţ			
	15- Red in/				SNR	: > -65 dB on all
	Chroma in		Ð			output
	16- fast switch				Bandwidth	: 5 MHz ± 1 dB
	RGB/ CVBS		4			
	or Y 17- CVBS GND		lacksquare	1.5	Audio Performance	
	18- fast switching		7			
	GND		Ť	1.5.1	Cinch Output Rear	
	19- CVBS/Y/RGB		_			
		V into 75 Ohm (*)	<u></u>		Output voltage 2 channel mode	: 2Vrms ± 1.5dB
	20- CVBS/Y		€		Output voltage 5.1 channel Dolby	: 1.41Vrms ± 1.5dB
	21- Shield		÷		Channel unbalance (1kHz) Crosstalk 1kHz	: <0.85dB
	(*) for 100% white				Crosstalk 20Hz-20kHz	: >105dB : >95dB
1.3.3	Audio/Video Front Input Co	nnactore			Frequency response 20Hz- 20kHz	: ± 0.1dB max
1.5.5	Addio/Video i Tont input Co	Intectors			Signal to noise ratio	: >100 dB
	Audio				Dynamic range 1kHz	: >9OdB
	Input voltage	: 2 Vrms			Dynamic range 20Hz-20kHz	: >88dB
	Input impedance	: >10kΩ			Distortion and noise 1kHz	: >9OdB
					Distortion and noise20Hz-20kHz Intermodulation distortion	: >80dB
	Video - Cinch				Phase non linearity	: >87dB : ±1º max.
	Input voltage	: 1 Vpp ± 0.1V	′		Level non linearity	: ± 0.5dB max.
	Input impedance	: 75 Ω			Mute (spin-up, pause, access)	: >100dB
					Outband attenuation:	: > 5OdB above
	Video - YC (Hosiden) Input voltage Y	. 11/22 - 0.11/				25kHz
	Input impedance Y	: 1Vpp ± 0.1V : 75 Ω				
	Input voltage C	: burst 300 mV	/pp ±	1.5.2	Scart Audio	
		{x} dB	FF -		Outrot wells as Outroom lands	0)
	Input impedance C	: 75 Ω			Output voltage 2 channel mode Output voltage 5.1 channel Dolby	: 2Vrms ± 1.5dB : 1.41 Vrms ± 1.5dB
					Channel unbalance (1kHz)	: <0.85dB
1.3.4	Cinch Audio/Video Line Inp	ut Rear			Crosstalk 1kHz	: >10.5dB
					Crosstalk 20Hz-20kHz	: > 95dB
	Audio (EXT1) Input voltage	. 0.1/222			Frequency response 20Hz- 20kHz	: ± 0. 1dB max
	Input impedance	: 2 Vrms : >10k Ω			Signal to noise ratio	: >10 O dB
	input impedance	. >10K 32			Dynamic range 1kHz Dynamic range 20Hz-20kHz	: >90dB : >86dB
	Video (EXT4)				Distortion and noise 1kHz	: >9)dB
	Input voltage	: 1 Vpp ± 0.1V			Distortion and noise20Hz-20kHz	: >8)dB
	Input impedance	: 75 Ω			Intermodulation distortion	: >87 d B
					Phase non linearity	: ± 10 max
1.3.5	YC Input Rear (Hosiden; E)	(T3)			Level non linearity	: ± 6.5dB max
					Mute (spin-up, pause, access)	: >1)OdB
	1 - GND		<u> </u>		Outband attenuation:	: > :OdB above 25(i ⊢lz
	2 - GND					20() 12
	3 - Input voltage Y 1Vpp ± 0.1	W 75 O	⊕	4.0	Digital Control	
	4 - Input voltage	V/ /5 52	U	1.6	Digital Output	
	. •	$nVpp \pm \{x\} dB/75 \Omega$		404	0	
		()		1.6.1	Coaxial	
1.4	Video Performance				CDDA/ LPCM (incl MPEG1)	: acording IEC958
	All - 1 - 1 - 1 - 1				MPEG2, AC3 audio DTS	: acording IEC1937
	All outputs loaded with 75 Oh		ating		טוט	: acording IEC1937, ame indment 1
	SNR measurements over full	Danawidin wililout Weigr	ung.			COLD B (COLOUR)
				160	Ontinal	

1.6.2 Optical

identical to coaxial

1.4.1 CVBS Output Rear (EXT4)

SNR Luminance SNR Chrominance AM : > -65 dB : > -65 dB



Digital Video Input (IEEE 1394)

1.7.1 **Applicable Standards**

Implementation according: IEEE Std 1394-1995

IEC 61883 - Part 1

IEC 61883 - Part 2 SD-DVCR (02-01-1997)

Specification of consumer use digital VCR's using 6.3 mm

magnetic tape - dec.1994

Mechanical connection according:

Annex A of 61883-1

1.7.2 Audio Quality

Output voltage 2 channel mode

: 2Vrms +/- 1.5dB

Channel unbalance (1kHz)

: Tbd

Crosstalk 20Hz-20kHz

Frequency response 20Hz- 12kHz : +/- 0.2dB max

Signal to noise ratio
Dynamic range 1kHz

: >85 dB

Dynamic range 1kHz : tbd

Dynamic range 20Hz-20kHz : Tbd

Distortion and noise 1kHz : >75dB

Distortion and noise 20Hz-20kHz

Distortion and noise 20Hz-20kHz : >75dB Intermodulation distortion : >80dB

Phase non linearity

: tbd

Level non linearity : tbd Mute (spin-up, pause, access) : tbd Level non linearity

: tbd

Outband attenuation

: tbd

1.8 **P50 System Control**

Via SCART pin nr 10

1.9 **Dimensions and Weight**

Place and height of feet

: acc. to Philips

Apparatus tray closed

Harmonisation line : WxDxH:435 x 330 x

110

Apparatus tray open

: WxDxH:435 x 470 x

110

Weight without packaging

: ca. 8.8 Kg \pm 0.5 kg

Weight in packaging

: ca. Tbc (>9 Kg)

1.10 Laser Output Power & Wavelength

1.10.1 DVD

Output power during reading

: 0.8mW

Output power during writing

: 20mW

Wavelength

: 660nm

1.10.2 CD

Output power

: 0.3mW

Wavelength

: 780nm

Warnings And Laser Safety Instructions



WARNING

All ICs and many other semi-conductors are susceptible to electrostatic discharges (ESD). Careless handling during repair can reduce life drastically.

When repairing, make sure that you are connected with the same potential as the mass of the set via a wrist wrap with resistance.

Keep components and tools also at this potential.



(F)

ATTENTION

Tous les IC et beaucoup d'autres semiconducteurs sont sensibles aux décharges statiques (ESD).

Leur longévité pourrait être considérablement écourtée par le fait qu'aucune précaution n'est prise a leur manipulation.

Lors de réparations, s'assurer de bien être relié au même potentiel que la masse de l'appareil et enfiler le bracelet serti d'une résistance de sécurité.

Veiller a ce que les composants ainsi que les outils que l'on utilise soient également a ce potentiel.



WARNUNG

Alle IC und viele andere Halbleiter sind empfindlich gegen elektrostatische Entladungen (ESD). Unsorgfältige Behandlung bei der Reparatur

kann die Lebensdauer drastisch vermindern. Sorgen sie dafür, das Sie im Reparaturfall über ein Pulsarmband mit Widerstand mit dem Massepotential des Gerätes verbunden

Halten Sie Bauteile und Hilfsmittel ebenfalls auf diesem Potential.



WAARSCHUWING

Alle IC's en vele andere halfgeleiders zijn gevoelig voor elektrostatische ontladingen (ESD).

Onzorgvuldig behandelen tijdens reparatie kan de levensduur drastisch doen verminderen.

Zorg ervoor dat u tijdens reparatie via een polsband met weerstand verbonden bent met hetzelfde potentiaal als de massa van het apparaat.

Houd componenten en hulpmiddelen ook op ditzelfde potentiaal.



AVVERTIMENTO

Tutti IC e parecchi semi-conduttori sono sensibili alle scariche statiche (ESD). La loro longevita potrebbe essere forte ridatta in caso di non osservazione della piu grande cauzione alla loro manipolazione. Durante le riparazioni occorre quindi essere collegato allo stesso potenziale che quello della massa dell'apparecchio tramite un braccialetto a resistenza.

Assicurarsi che i componenti e anche gli utensili con quali si lavora siano anche a questo potenziale.



Safety regulations require that the set be restored to its original condition and that parts which are identical with those specified be used.



Veiligheidsbepalingen vereisen, dat het apparaat in zijn oorspronkelijke toestand wordt terug gebracht en dat onderdelen, identiek aan de gespecifieerde worden toegepast.



Bei jeder Reparatur sind die geltenden Sicherheitsvorschriften zu beachten. Der Originalzustand des Gerats darf nicht verandert werden. Fur Reparaturen sind Original-Ersatzteile zu verwenden.



Le norme di sicurezza esigono che l'apparecchio venga rinesso nelle condizioni originali e che siano utilizzati pezzi di ricambiago idetici a quelli specificati.



Les normes de sécurité exigent que l'appareil soit remis a l'état d'origine et que soient utilisées les pièces de rechange identiques à celles spécifiées

SHOCK, FIRE HAZARD SERVICE TEST:

CAUTION: After servicing this appliance and prior to returning to customer, measure the resistance between either primary AC cord connector pins (with unit NOT connected to AC mains and its Power switch ON), and the face or Front Panel of product and controls and chassis bottom,

Any resistance measurement less than 1 Megohms should cause unit to be repaired or corrected before AC power is applied, and verified before return to user/customer. Ref.UL Standard NO.1492.

NOTE ON SAFETY:

Symbol A: Fire or electrical shock hazard. Only original parts should be used to replace any part with symbol A Any other component substitution(other than original type), may increase risk or fire or electrical shock azard.

LASER SAFETY

GB 6

This unit employs a laser. Only a qualified service person should remove the cover or attempt to service this device, due to possible eye injury.

LASER DEVICE UNIT

Type:

SemiconductorlaserGaAlAs

Wave length:

660 nm (DVD) 780 nm (VCD/CD)

Output Power: (out of objective) 20 mW (DVD+RW writing) 0,8 mW (DVD reading) 0,3 mW (VCD/CD reading)

Beam divergence:

60 degree



USE OF CONTROLS OR ADJUSTMENTS OR PERFORMANCE OF PROCEDURE OTHER THAN THOSE SPECIFIED HEREIN MAY RESULT IN HAZARDOUS RADIATION EXPOSURE.

AVOID DIRECT EXPOSURE TO BEAM

WARNING

The use of optical instruments with this product will increase eye hazard. Repair handling should take place as much as possible with a disc loaded inside the player

WARNING LOCATION: INSIDE ON LASER COVERSHIELD

CAUTION VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID EXPOSURE TO BEAM ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING VED ÅBNING UNDGÅ UDSÆTTELSE FOR STRÅLING ADVARSEL SYNLIG OG USYNLIG LASERSTRÅLING NÅR DEKSEL ÅPNES UNNGÅ EKSPONERING FOR STRÅLEN VARNING SYNLIG OCH OSYNLIG LASERSTRÅLNING NÄR DENNA DEL ÄR ÖPPNAD BETRAKTA EJ STRÅLEN VARO! AVATTAESSA OLET ALTTIINA NÄKYVÄLLE JA NÄKYMÄTTÖMÄLLE LASER SÄTEILYLLE. ÄLÄ KATSO SÄTEESEEN <u>VORSICHT</u> SICHTBARE UND UNSICHTBARE LASERSTRAHLUNG WENN ABDECKUNG GEÖFFNET NICHT DEM STRAHL AUSSETSEN DANGER VISIBLE AND INVISIBLE LASER RADIATION WHEN OPEN AVOID DIRECT EXPOSURE TO BEAM ATTENTION RAYONNEMENT LASER VISIBLE ET INVISIBLE EN CAS D'OUVERTURE EXPOSITION DANGEREUSE AU FAISCEAU

CAUTION



ONLY QUALIFIED SERVICE PERSONNEL SHOULD REMOVE THE COVER

OR ATTEMPT TO SERVICE THIS DEVICE.

CL 16532095_052.eps

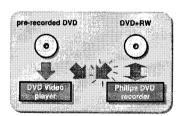
Introduction

DVD Video Recorder

DVD (Digital Versatile Disc) is the new storage medium that combines the convenience of the Compact Disc with the latest advanced digital video technology. DVD Video uses state-of-the-art MPEG2 data compression technology to register an entire movie on a single 5-inch disc. DVD's variable bitrate compression, running at up to 9.8 Mbits/second, captures even the most complex pictures in their original quality. The crystal-clear digital pictures have a horizontal resolution of over 500 lines, with 720 pixels (picture elements) to each line. This resolution is more than double that of VHS, superior to Laser Disc, and entirely comparable with digital masters made in recording

DVD+ReWritable (DVD+RW) is the next step in video technology. DVD+RW uses phase-change media, the same technology that formed the basis for CD-ReWritable. A high-power laser is used to change the reflectivity of the recording layer. This process can be repeated more than a thousand times.

Your Philips DVD recorder is a recorder and player for digital video discs, with a two-way compatibility to the universal DVD Video standard. This means that: - existing pre-recorded DVD Video discs can be played on your Philips DVD recorder and - recordings, made on your Philips DVD recorder, can be played on existing DVD Video players and DVD-ROM drives.



With it, you will be able to record TV programmes or to edit and archive your own camcorder recordings. Superb digital picture and sound quality, quick access to the tracks you have recorded and extensive playback features contribute to a completely new video experience.

From now on you will enjoy full-length movies with true cinema picture quality, and stereo or Multi-channel sound (depending on the disc, and on your playback setup). You will find your recorder remarkably easy to use. by way of the On-Screen Display and recorder display, in combination with the remote control.

Box contents

First check and identify the contents of your DVD recorder package, as listed below:

- DVD recorder
- Remote Control Handset with separately-packed batteries
- 2-core power cord
- SCART cable - S-video cable
- Antenna (aerial) cable
- Audio cable
- Video cable
- DVD+RW disc - User Manual
- Warranty card

If any item should be damaged or missing, please inform your supplier without delay.

Keep the packaging materials; you may need them to transport your recorder in the future.

Placement



- Place the recorder on a firm, flat surface.
- · Keep away from domestic heating equipment and direct sunlight.
- In a cabinet, allow about 2.5 cm (1 inch) of free space all around the recorder for adequate ventilation.
- The lense may cloud over when the DVD recorder is suddenly moved from cold to warm surroundings. Playing a CD/DVD is not possible then. Leave the DVD recorder in a warm environment for two hours before use, so the moisture can evaporate.
- The recorder should not be exposed to dripping or splashing, no object filled with liquids, such as vases, should be placed on the recorder.

Cleaning discs

Some problems may occur because the disc inside the recorder is dirty. To avoid these problems clean your discs regularly, in the following way:

• When a disc becomes dirty, clean it with a cleaning cloth. Wipe the disc from the centre out.

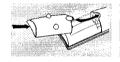
Caution:

Do not use solvents such as benzine, thinner, commercially available cleaners, or anti-static spray intended for analogue discs. Do not use commercially available cleaning discs

to clean the lens, as these discs may damage the optical unit.

Remote control

Loading the batteries





- Open the battery compartment cover.
- Insert two 'AA' (LR-6) batteries as indicated inside the battery compartment.
- Close the cover.

Caution:

Do not mix old and new batteries. Never mix different types of batteries (standard, alkaline, etc.). This may reduce the lifetime of the batteries.

Installation

Connections - back side of your DVD recorder

- Please refer to your TV set, VCR, Stereo System and any other User Manual(s) as necessary to make the optimal connections.
- Do not connect the power until all other connections are made.
- Do not connect your DVD recorder to your TV set via your VCR, because the video quality could be distorted by the copy protection system.
- For better sound reproduction you can connect the recorder audio outputs to your amplifier, receiver, stereo system or AV equipment. For this see 'Connecting to AV' receiver or AV' amplifier'.

Caution:

Do not connect the recorder's audio output to the phono input of your audio system in order to avoid damage to your equipment.

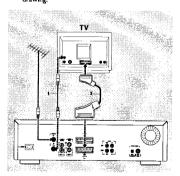
Connecting to the antenna

- Remove the antenna (aerial) cable plug from your TV set and insert it into the antenna socket at the back of the DVD recorder.
- Plug one end of the antenna (aerial) cable supplied (1) into the TV socket on the DVD recorder and the other end into the antenna input socket on your TV set.

Connecting to a TV set

To obtain the highest possible picture and sound quality from your TV set it is recommended to use the SCART connector on both DVD recorder and TV set.

 Connect the bottom SCART connector (EXT 1) to the corresponding connector on the TV set, using the SCART cable supplied (2) as shown in the

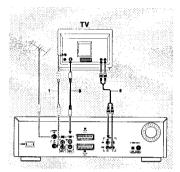


If your TV set is not equipped with a SCART connector, you can connect the DVD recorder with the S-video (Y/C) sockets.

10 INSTALLATION

S-video (Y/C) connection

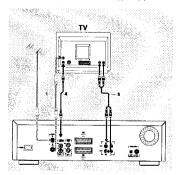
- Connect the S-video output socket to the corresponding input socket on the TV set, using the supplied S-video cable (3).
- Connect the audio Left and Right output sockets to the corresponding sockets on the TV set using the audio cable supplied (5).



If your TV set is not equipped with S-video sockets, then connect the DVD recorder with the CVBS sockets to your TV set.

Video (CVBS) connection

- Connect the Video (CVBS) output socket (yellow) to the corresponding input socket on the TV set using the video cable supplied (4).
- Connect the audio Left (white) and Right (red) output sockets to the corresponding sockets on the TV set using the audio cable supplied (5).



Connecting to audio equipment

Connecting to A/V receiver or A/V amplifier with digital Multi-channel decoder

The best possible sound quality is obtained by connecting your DVD recorder to an A/V receiver with Multi-channel decoder (Dolby Digital, MPEG 2 and DTS).

Digital Multi-channel sound

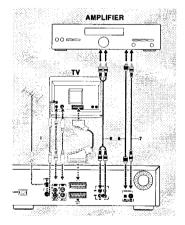
Digital Multi-channel connection provides the optimum sound quality. For this you need a Multi-channel A/V receiver that supports one or more of the audio types supported by your DVD recorder (MPEG 2, Dolby Digital and DTS). For this you can check the receiver manual and the logos on the front of the receiver.

 Connect the recorder's digital audio output to the corresponding input on the receiver. Use a digital coaxial cable (7) or a digital optical audio cable (8).

If you do not have a digital coaxial audio cable, you may use the supplied video cable (4).

Note

If the audio type of the digital output does not match the capabilities of your receiver, the receiver will produce a strong, distorted sound. The audio type of the DVD disc in play is displayed in the Status Window, when changing the language. 6 Channel Digital Surround Sound via digital connection can only be obtained if your receiver is equipped with a Digital Multi-channel decoder.



If you cannot connect your DVD recorder to an A/V receiver with Multi-channel decoder, choose one of the following alternatives.

Connecting to a receiver equipped with two channel digital stereo (PCM)

- Connect the recorder's digital audio output to the corresponding input on your receiver. Use the supplied video (CVBS) cable (7) or an optional digital optical audio cable (8).
- After installation you will need to activate PCM on the DVD recorder's digital output (see 'User Preferences').

Connecting to a receiver equipped with Dolby Pro Logic

- Connect the recorder to the TV set and connect the recorder's audio Left and Right output sockets to the corresponding inputs on the Dolby Pro Logic Audio/Video receiver, using the audio cable supplied (6).
- Make the appropriate Sound settings for Analogue Output in the user preferences menu.

Connecting to a TV set equipped with a Dolby Pro Logic decoder

 Connect the recorder to the TV set as described in chapter 'Connecting to a TV set'.

Connecting to a receiver with two channel analogue stereo

 If you have a receiver with two-channel analogue stereo without any of the above mentioned sound systems, connect the audio Left and Right output sockets to the corresponding sockets on your receiver, amplifier or stereo system. Use the audio cable supplied (6).

INSTALLATION 11

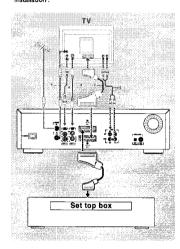
Connecting to other equipment

Use the top SCART connector (EXT 2) on your DVD recorder to make connections to a:

- Satellite receiver or Set top box,
- VCR.
- DVD Video player

Most pre-recorded video cassettes and DVD discs are copy protected. If you try to copy them the display shows COPY PROTECT.

For installation of a decoder, see 'User Preferences' -'installation'.

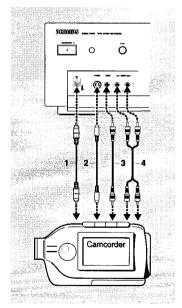


If the power is off or Low Power Standby is selected (see User Preferences - features), the signal from EXT 2 will not be passed on to the TV set on EXT 1.

Connections - frontside of your **DVD** recorder

Camcorder connection

- If you have a DV or Digital 8 camcorder, connect the i-link DV input socket (1) to the corresponding output socket on the camcorder using the i-link cable of your camcorder.
- If you have a Hi-8 or S-VHS(C) camcorder, connect the S-video input socket to the corresponding output socket on the camcorder, using the S-video cable supplied (2) and connect the audio cable (4) supplied.
- Otherwise connect the Video input socket (yellow) to the corresponding output socket on the camcorder using the video cable supplied (3) and connect the audio Left (white) and Right (red) input sockets to the corresponding sockets on the camcorder using the audio cable supplied (4).



Power supply



- Make sure that all necessary connections are made before connecting the DVD recorder to the power
- Plug the power cable supplied into the Power connector on the rear of the recorder.
- Plug the mains plug into an AC outlet.

Always check if the local mains voltage matches the required 220V - 240V.

When the recorder is in the Standby position, it is still consuming some power.

If you wish to disconnect your DVD recorder completely from the mains, withdraw the plug from the AC Outlet. When the DVD recorder is disconnected from the mains, TV channels and timer data will be stored typically 1 year.

First time set-up: virgin mode

After switching on the DVD recorder for the very first time the 'virgin mode screen' will appear.

In 'virgin mode' you may have to set your preferences for some of the recorder features.

If the 'virgin mode screen' does not appear, your DVD recorder has been installed already. You may still change the settings via the 'installation menu'.

Depending on the kind of TV set, preferences will have to be set manually or they will be taken over automatically from the TV set.

Automatic setting

When your TV set is equipped with EasyLink™, Cinema Link™, NexTVIEW Link™, SmartLink™, O-Link™ or MegaLogic™, the TV settings will be taken over from the TV set but they cannot be changed manually afterwards.

When preferences are taken over from your TV set, the message Easy Link loading data from TV - please wait' will appear.

Menus for which no preferences are available will be displayed. They have to be set manually.

Preferences have to be set in the order in which the item menus will appear on the screen.

If the recorder is switched off while setting user preferences, all preferences have to be set again after switching the recorder on again.

The 'virgin mode' will only be concluded after the preferences for the last item have been confirmed.



۰

Manual setting

When a menu is displayed:

- Use OK to confirm your selection and to select the next menu.

The following items may have to be set in virgin mode:

Menu language

The on-screen menus will be displayed in the language you choose.



Audio language

The sound will be in the language you choose, provided this is available on the disc in play. If not, speech will revert to the first spoken language on the disc. Also the DVD Video disc menu will be in the language you choose, provided this is available on the disc.



Subtitle language

The subtitles will be in the language you choose provided this is available on the disc in play. If not, subtitles will revert to the first subtitle language on the disc.

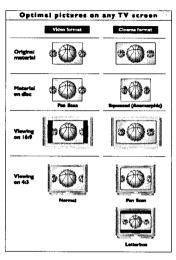


TV Shape

You can choose:

- 16:9 if you have a wide screen (16:9) TV set.
- 4:3 If you have a regular (4:3) TV set. In this case you can also choose between:
- Letterbox for a 'wide-screen' picture with black bars top and bottom,
- Pan Scan, for a full-height picture with the sides trimmed. If a disc has Pan Scan, the picture then moves (pans) horizontally to keep the main action on the screen.





Country

Select your country. This is used as input for the 'Parental Control' feature (see 'Access Control') as well as the searching of TV channels.



Auto TV Channel Search

Make sure the antenna is connected. See 'Connecting to the antenna'. Your DVD recorder will search for all TV channels.

It stores channels in the sequence they are found.

- Confirm with OK.
- > Auto search starts. This can take several minutes.

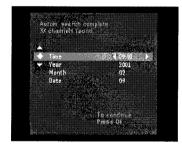


➤ When Auto search is completed 'Autom' search complete - XX channels found' appears on the TV screen.

After Auto channel search you can have TV channels stored automatically in the same order as your TV set. See 'User preferences installation' - 'Follow TV'.

Time/Date

When Channel auto search is completed the actual Time and Date are also set automatically. If the time in the DVD recorder display is not correct, the clock must be set manually.



- Adjust 'Time', 'Year', 'Month', 'Date' if required, with the ♥ (down cursor) or △ (up cursor) key.
- Change values with the the ≤ (left cursor) or ▷ (right cursor) key or the digit keys 0-9.
- To end, press OK.

Note:

All these items may have to be set after first start up ('virgin mode'). After that they can always be adapted in the user preferences menu. When your TV set is equipped with Easy Link the TV set presets will be taken over from the TV set but they connot be changed manually afterwards.

Virgin mode settings are now completed.

All settings can still be changed. See 'User preferences'.

INSTALLATION 15

14 INSTALLATION

Ouick start

Recording and playback are the basic functions of your DVD recorder. In this chapter the elementary operations for recording or playing a disc are presented separately for quick reference purposes. Detailed information on different modes, settings and features can be found in the chapter 'Operation'.

Switching on

- Switch on the TV set and select the programme number that you have chosen for video playback (see operating manual for your TV set).
- Press (1) STANDBY/ON The recorder display lights up, and the 'virgin mode screen' appears.



The virgin mode will only occur after the very first start up of the recorder. In virgin mode you may have to set your personal preferences for some of the recorder's most relevant items. See virgin mode in the previous

Manual recording

Checking input

Normally, the DVD recorder displays the contents of the disc on screen. Use the TUNER key in order to switch to the internal tuner, or whichever other source is selected, if you want to check the input before starting a recording. Press TUNER again to go back to disc mode.

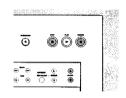
Recording

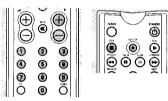
- Insert a recordable DVD+RW disc.
- Use CHANNEL A or CHANNEL ▼ (on the recorder) or P+, P- or the digit keys 0-9 (on the remote control) to select the programme number (programme name) from which you wish to record.

When a TV channel transmits a channel name, it will be shown on the display and on screen.

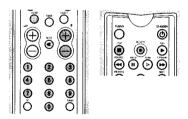
- Press RECORD (on recorder) or REC/OTR (on remote control).
- > RECORD is shown on the display.
- Prace STOP to stop recording.

 MENU UPBATE is shown on the display.





Recording with automatic switch-off (OTR One-Touch Recording)



- Insert a recordable DVD+RW disc.
- Use CHANNEL ▲ or CHANNEL ▼ (on the recorder) or P+, P- or the digit keys 0-9 (on the remote control) to select the programme number (programme name) from which you wish to record
- Press RECORD (on recorder) or RECIOTR (on remote control) twice.
 - A recording will be made of 30 minutes.
 - > The required end time of the recording is shown in the timer box on screen. The remaining recording time is shown in the status box on screen and on the display.



- Press RECORD or REC/OTR again to obtain a 30-minute increment.
- Shortly after pressing REC/OTR, OTR can be cancelled by pressing CLEAR.

Timer programming

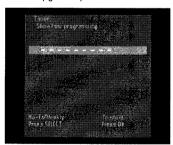
Timer programming with 'ShowView'

A ShowView programming number is a number of up to nine digits, printed in most TV guides next to the start time of a TV programme. It contains all information you need for programming a timer.

- Press TIMER on the remote control.
- Select 'ShowView programming' with △ (up cursor) or ♥ (down cursor).



Press ▷ (right cursor).



- Enter the entire ShowView programming number. You can correct it if you made a mistake, with
- Confirm with OK
- > The data will appear on the TV screen.
- Confirm with the OK key.
- > The data has been stored in a timer block.
- To end, press TIMER.
- Please make sure that you inserted a disc without erase protection. If you inserted a disc with erase protection, it will be ejected.
- Switch off with () STANDBY/ON.

Timer programming without 'ShowView'

- Press TIMER on the remote control.
- Select 'Timer programming' with △ (up cursor) or ♥ (down cursor).
- Press ▷ (right cursor).



- Enter the date with △ (up cursor) or ▽ (down cursor), or with the digit keys 0-9.
- Press ▷ (right cursor).
- Enter the programme number from which you want to record.
- Press ▷ (right cursor).
- Enter the Start time.
- Press ▷ (right cursor).
- Enter the End time. ● If you made a mistake, you can go back with < (left
- Confirm with OK.
- > The data has been stored in a timer block.
- To end, press TIMER. Make sure that you inserted a disc without write protection. If you inserted a write-protected (locked) disc, recording will be refused.
- Switch off with () STANDBY/ON.

Playing a pre-recorded DVD-Video disc



- Insert a pre-recorded DVD-Video disc. ➤ When 'Autoresume' is set to 'On' (see 'User Preferences') playback starts automatically from the point where it was stopped, the last time the disc
- ➤ When 'Autoresume' is set to 'Off', the disc will play from the start of the disc. You can however resume play from the point at which you stopped, the last time the disc was played, by pressing PLAY shortly after the disc starts to play.
- The disc may invite you to select an item from a menu. If the selections are numbered, press the appropriate numerical key; if not, use the ∇ Δ (down up cursor) or < ▷ (left right cursor) keys to highlight your selection, and press OK.
- > The currently playing title and chapter number are displayed in the System menu bar and the recorder display. The elapsed time is shown in the disc status window and the recorder display.



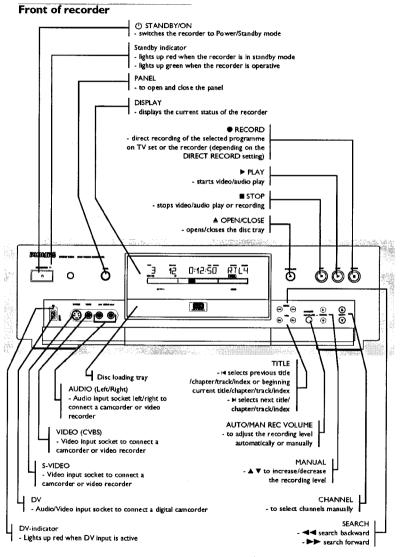
● To stop playback at any time, press ■ STOP or DISC MENU.

Playing a recordable DVD+RW



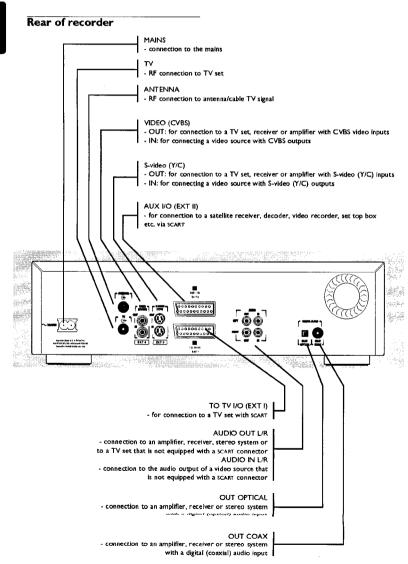
- Insert a recordable DVD+RW disc. ➤ If the disc is a new blank disc, the display will show 'EMPT'S DISE'.
- > If the inserted disc is write-protected, playback always starts automatically.
- When you press ➤ PLAY, playback always starts automatically from the point where it was stopped the last time the disc was played or recorded. If you want to start playback from the beginning of the disc, you can do so via the Index Picture Screen (see 'Index Picture Screen').
- With M PREVIOUS and M NEXT you can go to the previous or next title.
- To stop playback at any time, press STOP or DISC MENU.
- > You return to the Index Picture Screen.

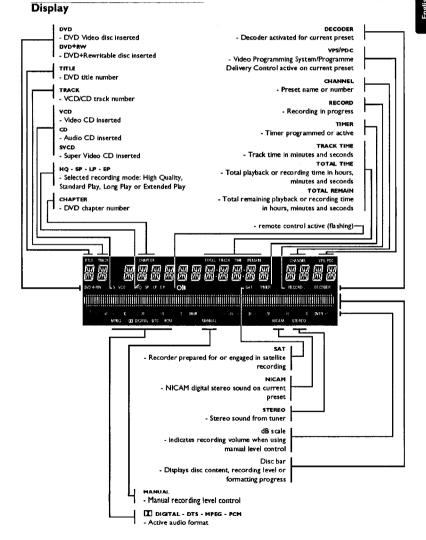
Functional overview



18 QUICK START

FUNCTIONAL OVERVIEW 19





Operation

Important notes for operation

You can switch on the DVD recorder with the (b) STANDBY(ON key. Keep your DVD recorder connected to the mains at all dimes to ensure that programmed recordings can be made and that the television functions normally.



Both the DVD recorder and the remote control have an 'Emergency interrupt' button. You can use the O STANDBY button to interrupt a function. When you have an operating problem, you can interrupt the function and start again.



Loading discs

- 1 Press A OPEN/CLOSE on the front of the recorder. The disc loading tray opens.
- 2 Lay your chosen disc in the tray, label side up. Make sure it is sitting properly in the correct recess.
- 3 Press ▲ OPEN/CLOSE, to close the tray, ➤ "REABING" appears in the status window and on the recorder display. If the Inserted disc is prerecorded or write-protected, playback always starts automatically.

You can always unload a disc by pressing **A OPEN/CLOSE** again or pressing **E STOP** on the remote control for two seconds.

Note: If 'Child Lock' is set to ON and the disc inserted is not in the 'child safe' list (not authorized), the PIN code must be entered and/or the disc has to be authorized. (see 'Access Control')

Disc types

You will recognize the different types of discs, that can be used in your DVD recorder by the logo. Depending on the disc type you can either use it for recording and playback or playback only. Some discs are not suitable at all to be used in the DVD recorder.

In the next table a summary is given of all excisting disc types and their DVD recorder compatibility.

The following disc types can be used for recording and playback:

DVD+RW

Records and plays; In case of a new blank disc, after the first recording, some more time (up to two minutes) is needed to make the disc compatible with DVD video players.



The following disc types can be used for playback only:

DVD-Video





DVD-R
Only plays if it contains DVD-Video.





DVD-RW

Only plays if it is recorded in video mode and has been finalized.





22 FUNCTIONAL OVERVIEW

Remote control

- direct recording of the currently

- previous chapter, track or title

- next chapter, track or title

- TV volume up/down

- TV Mute ON/OFF

- programme up/down

- enlarge video image

- select DVD camera angle

- subtitle language selector

- audio language selector

- displays edit menu for DVD+RW

(

PLO

MEXT

(H)

OK

(3)

(6)

(9)

 (\mathbf{O})

(*****K)

(2)

(5)

(8)

(0)

PHILIPS

In a TV set - DVD recorder - Set top box configuration use the TV/DVD' switch to switch back and forth between Set top box reception and DVD recorder reception. This only functions when you used a Scart cable to connect the DVD recorder to your TV set and if your TV set responds to this switch-over. This function is useful when, for example, you want to watch a channel from the Set top box on your TV set and make at the same time a recording from another

A-B

①

(4)

ANGLE SUBTILE

(H)

REVERSE PREVIOUS STANDBY ()

DISC MENU

picture screen

VADA

RETURN

CLEAR

TIMER

SELECT

in a menu

OK

SYSTEM MENU
- displays recorder menu bar

- down/up/right/left cursor

- go back to previous menu step

- delete last entry/clear TIMER

- switches between different values

- displays the 'timer menu'

- acknowledge menu selection

- switches between disc mode and

enables other keys to operate

changes brightness setting of

- repeat chapter, track, title, disc

- playback of the first 10 seconds

of each chapter within a title (DVD) or the first 10 seconds of each track on a disc (VCD/CD)

the TV set (see Appendix)

- numerical key pad

- select title

tuner mode

REPEAT

REPEAT A-B

- repeat sequence SCAN

SIDE SWITCH

TUNER

- select chapter

- displays DVD disc menu or index

TV/DVD switch
- DVD mode/TV mode selector

selected programme

- search backward

- search forward

for TV set*

- plav

44

- pause

-

EDIT

disc

-++-

⊕ ZOOM

ANGLE

RE AUDIO

SUBTITLE

OPERATION 23



Super Audio CD

Of hybrid SACD discs, the CD layer can be played.

(Super) Video CD

Depending on the material on the disc (a movie, video clips, a drama series, etc.) these discs may have one or more tracks, and tracks may have one or more indexes, as indicated on the disc case. To make access easy and convenient, your recorder lets you move between tracks, and between indexes.



CD-R

Plays if it contains Audio CD.



CD-RW

Plays if it contains Audio CD.



The following disc types cannot be used at all, neither for recording nor for playback: DVD-RAM





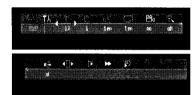
DVD-Audio



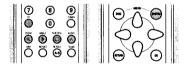


On-screen display information

System menu bar



The System menu bar can be called up by pressing any of the following keys on the remote control: SYSTEM MENU, T/C, ANGLE >, SUBTITLE AUDIO (({ and ZOOM .



A number of recorder functions can be controlled via the system menu bar. You can navigate between the two parts of the system menu bar with the < (left cursor) and the ▷ (right cursor) key.

Menu bar icons

⊕ Zoom

PART 1 PART 2 User preference Title/Track Picture by Picture Chapter/Index Slow motion (√€ Audio language Fast motion Subtitle language Time search 294 Angle

Temporary Feedback Field



The system menu bar contains a 'Temporary Feedback Field' with information concerning prohibited actions, playback modes, available angles, etc.



Child Lock On

Child Safe Action prohibited

User preference menu operation

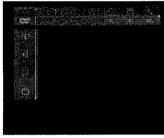
- Press SYSTEM MENU on the remote control. Select Th in the system menu bar and press ♥
- (down cursor). > The user preferences menu appears.
- Use the ▷ ▷ ▷ ♡ (left right up down cursor) keys to toggle through the menus, sub menus and submenu options.
- > When a menu item is selected, the cursor keys (on the remote control) to operate the item are displayed next to the item.
- Press OK to confirm and return to the main menu.



The following functions can be operated via the user preference menu.

User preference menu icons

- Picture settings
- Sound settings
- Language settings
- ٥ Feature settings
- Remote control settings
- Record settings
- Installation
- You can navigate between the various items of the user preferences menu with the \(\Delta \) (up cursor) and the \forall (down cursor) key. To select an item press \triangleright (right cursor) key.





 By pressing SYSTEM MENU the system menu bar will disappear from the screen.

Status box

The status box displays the current status of the recorder and the disc type loaded.







Disc type icons

DVD+RW DVD-Video Video-CD

no disc

① **317** disc error Directions For Use

DVDR1000 /0x1 /69

Disc status icons

recording stop play

Dantas El pause play

● H pause

record pause

erasing B:

fast forward

8 x fast reverse

slow motion

Tuner info box

The tuner info box is located at the bottom left of the screen and is displayed in tuner mode (See: Recording Checking input). It displays the currently selected input. When the tuner is selected it shows programme number and/or channel name.



Current channel



No signal



Copy-protected signal

Timer Info box

The timer info box is located above the tuner info box and is displayed in tuner mode. It displays the current status of the timer.

When a timer is programmed it shows a timer indication and the start time or date of the first programmed recording.



Timer event due today



Timer event due on another day

When an OTR recording is in progress it shows the end



OTR recording in progress

When no timer is programmed it displays the current



Current time

Note: Tuner info box and timer info box disappear during playback and after recording is started.

Warning box

The warning box will be displayed on the location of the status box. For instance: 'Disc locked'



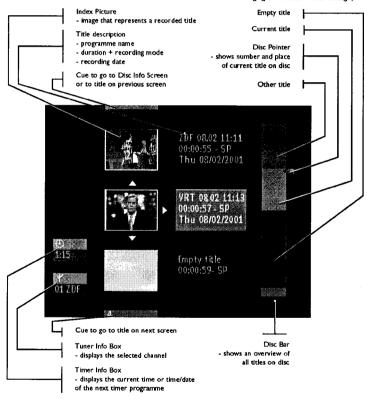
Index Picture Screen

The Index Picture Screen displays an overview of the titles recorded on the disc. Each title is represented by an index picture. Next to the index picture the programme name, duration, recording mode and recording date of the title are shown. If no name is known, the DVD recorder will fill in the source and the time of the recording instead.

Empty spaces (erased titles, or blank space at the end of the disc) are also shown as such.

At maximum three titles will be shown on the screen at once. If more titles are present, you can navigate to those with the $\nabla \Delta$ (down up cursor) keys.

- On the right hand side of the Index Picture Screen. you can see the disc bar. This gives an overview of all titles on the disc, as well as any empty spaces. On the disc bar, an arrow - the disc pointer indicates your current position on the disc. From this point you may resume playback or recording.
- If you navigate trough the list of titles with ♥ △ (down up cursor) or ⋈ PREVIOUS/⋈ NEXT, the disc pointer will move along.
- Press STOP to reset the disc pointer to the beginning of the disc.
- To move the disc pointer to the end of the last title, keep ► NEXT pressed.
- If you navigate from an Index Picture to the box right next to it (containing name, rec mode, etc.), you enter the title settings menu (see under 'Managing disc content - Title settings').



26 OPERATION

OPERATION 27

T User preferences

Setting user preferences

You can set your user preferences for some of the recorder features. (See 'Operation' - 'User preferences menu operation'.)

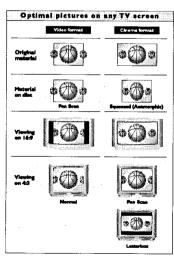
The following items can be adapted:



TV Shape

With TV Shape you can adjust the output of your DVD Video Recorder to optimally fit your TV screen. You can choose:

- 16:9 if you have a wide screen (16:9) TV set.
- 4:3 if you have a regular (4:3) TV set. In this case you can also choose between:
- Letterbox: for a 'wide-screen' picture with black bars at the top and bottom.
- Pan Scan: for a full-height picture with the sides trimmed. If a disc has Pan Scan, the picture then moves (pans) horizontally to keep the main action on the screen.

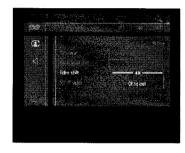


Black level shift (NTSC only)

Adapts the colour dynamics to obtain richer contrasts. Select On or Off.

Video shi

Factory setting is such that the video will be centered on your screen. Use this setting to adjust the position of the picture on your TV set by scrolling it to the left or right.



SCART Vide

Factory setting is RGB. Select S-video (Y/C) via scart when connecting to an S-VHS recorder.

Sound settings

Digital output

Factory setting 'All' means that both coaxial and optical outputs are switched on, and that Dolby Digital and MPEG-2 Mulki-channel is fed to the outputs as such. If your equipment doesn't include a digital Mulki-channel decoder, set the digital output to 'PCM only' (Pulse Code Modulation). Both coaxial and optical outputs are then switched on, and Dolby Digital and MPEG2 Multi-channel are converted to PCM. If you are not connecting equipment with a digital input, change the setting to 'Off'.

Analogue output



Select Stereo, Surround or 3D Sound. Factory setting is Stereo.

Surround: Select this setting when using equipment with a Doby Surround Pro Logic decoder. In this setting the 5.1 audio channels (Doby Digital, MPEG-2) are downmixed to a Surround-compatible 2-channel output.

3D Sound: In a set-up without rear speakers (analogue stereo output), this option remixes the six channels of digital surround (Dolby Digital, MPEG-2) into a two speaker output, while retaining all of the original audio information. The result is the listening sensation of being surrounded by multiple speakers.

Connected audio system	Digital out	Analogue ou
Amplifier or TV with two channel analogue sterea	of f	Stereo
Amplifier or TV with Dolby Surround or Dolby Pro Logic	Off	Surround
Amplifier with two channel digital stereo	PCM only	Stereo
A/V receiver with Multi-channel	AI	Stereo or
decoder (Doby Digital, MPEG, DTS)		Surround
Multi-channel A/V receiver with	Off	Surround

6-ch connectors Night Mode

Night mode optimizes the dynamics of the sound with low volume playback for less disturbance in quiet environments. This only works for Dolby Digital audio on DVD video discs.

Language settings

The preferred language can be adapted via the system menu bar. Also see 'virgin mode'. Settings can be changed for:

- Menu language
- Playback audio language
- Subtitle language
- Country setting.

Feature settings

Access Contro

Access Control contains the following features: Child Lock - When Child Lock is set on, a 4-digit code needs to be entered in order to play discs. Parental Level - Allows the conditional presentation of DVD discs containing Parental Level information. Change country - Allows conditional presentation of DVD-Video discs containing country information. Change code - To change the pin code. See 'Access Control'.

Adapt disc format

This options adapts the menu of a DVD+RW disc, recorded on a different brand of recorder, to the own recorder.

A DVD+RW video disc that has been recorded on a different type or brand of recorder can be played, but may not provide all features commonly available to DVD+RW discs, such as the on-screen disc bar, the disc settings menu, the title settings menu, and editing. If the disc is not write-protected, the disc format can be adapted to the own recorder, after which these functions are available.

Status bo

The status box displays the current status of the recorder and the disc type loaded (See 'Operation' - 'On-screen display information'). You can switch it on or

Off = always Off.

On = displayed together with the system menu bar or displayed temporarily (disappears after time-out) when changing the playback or record status. Factory setting is 'On'.

Low Power Standby

If Low Power Standby is 'On', the recorder will consume minimum power in standby mode.

Factory setting is 'Off'.

Note:

When the recorder is in low power standby mode:

- the output of the equipment connected to EXT 2 will not
be possed through to the TV set on EXT 1,

- the Display will be Off,
- the Standby indicator on the recorder will still light up in standby mode.



Auto resume

The Auto resume setting only applies to pre-recorded DVD-video and Video CD discs only - not only to the disc in the recorder but also to the last twenty discs you

If Autoresume is set to 'On', playback will start from the point where it was stopped the last time the disc was played.

When Autoresume is set to 'Off', the recorder will start playing from the beginning of a disc. In this case you can still resume when repears on screen by pressing PLAY. Factory setting is 'On'.

This feature allows you to disable or enable the PBC (Playback Control) menu of VCD discs. See under 'Special VCD features': Factory settings is 'On'.

Remote Control settings

Key sound

The recorder makes a 'beep' sound upon every key command given via recorder or remote control keys. Select 'Off' to disable this sound. Factory setting is 'On'.

Remote control used

If you want to use the remote control of a Philips DVD player instead of the standard DVD recorder remote control, select 'DVD player'. Factory setting is 'DVD recorder.

Record Settings

Record mode

By selecting a recording mode you define picture quality of recordings and maximum recording time for a disc.

Mode	Picture quality	Total recording time
HQ (High Quality)	best possible picture quality	60 minutes
SP (Standard Play)	pre-recorded DVD quality	120 minutes
LP (Long Play)	better than S-VHS picture quality	180 minutes
EP (Extended Play)	better than VHS picture quality	240 minutes

For playback, the correct recording mode will automatically be selected. Depending on the selected mode the available recording time on a disc varies.

In the record settings menu, select 'Record mode'.



- Alter the recording mode with

 or

 (left right) cursor).
- Confirm with the OK key.
- To end, press SYSTEM MENU.

Direct record

With the Direct Record function switched On and the DVD recorder switched to standby, the channel number selected on your television will be automatically taken over by the DVD recorder, at the moment it starts recording. This only applies for televisions connected via SCART, Easy Link and NEXTVIEW Link. Factory setting is

- In the record settings menu, select 'Direct record'.
- Select On. If you select Off, the function will be switched off.
- Confirm with OK.
- To end, press SYSTEM MENU.

Sat record

You can only use this function, when you have a satellite receiver, which can control other equipment by a 'programming' function. In this mode your DVD recorder starts recording when the satellite receiver releases a signal. The start and end of the recording is controlled via one of the SCART sockets.

- In the record settings menu, select 'Sat record'.
- Select the SCART socket to which the satellite receiver is connected with < or > (left right cursor).
- Confirm with OK.
- Insert a recordable DVD+RW disc.
- Press () STANDBY/ON.
- > When this function is switched on, SAT appears on the display.
- > The DVD recorder is now prepared for recording.

Factory setting is Off.

Auto chapters

If autochapters is 'On' every five to six minutes a chapter marker (beginning of a new chapter) is inserted during recording. This enables easy navigation through a title during playback. In either case, you can manually Insert chapter markers afterwards. (See 'Managing disc content' - 'Edit in playback mode'.)

LP/EP rec mode

In long play or extended play recording mode you can select the Sport setting to optimize the video recording for images that contain fast movements, like sports programmes. The setting does not influence high quality or standard play recording mode. Factory setting is Stndrd.

Installation

Auto TV Channel Search

Your DVD recorder will search for all TV channels. It stores channels in the sequence they are found. (See 'Installation - First time Set-up')

Note: All channels stored so far will be erased.

With Follow TV you can programme the same channel sequence on the DVD recorder as on the TV set. This only functions if the recorder socket (EXT1) and the TV set are connected with a SCART cable. Additional equipment connected to socket EXT2 must be switched



Press OK.

➤ If the DVD recorder recognizes that the TV set has been connected with a SCART cable, "IVD I" appears on the display.



- ➤ When "\\BTP" (no signal from TV set) appears on the display, the TV channels can not be allocated automatically. In this case read 'Manual TV channel
- Select programme number '1' on the TV set.
- Confirm with OK on the remote control of the DVD recorder.
 - > The DVD recorder compares the TV channels on the TV set and the DVD recorder. If the channels match, this channel is stored at 'P01'.
- Walt until 'TFB2' appears and repeat the previous two steps for programme number 2 and the rest of the channels you want to store.
- To end, press SYSTEM MENU.

30 OPERATION

Manual TV channel search

You can perform a search to select and store TV channels manually.

- Press SYSTEM MENU.
- Select Installation
- Select Manual search.
- In the line Channel/freq, select the display for: Freq : frequency CH : channel
- S-CH : special channel
- If you know the frequency or channel of the desired TV channel, you can enter the data in line Entry/search with the digit keys 0-9. If you don't know the frequency or channel of the TV channel of your choice, press (right cursor) to start channel search.
- In the line Programme number select the programme number you want, using ⊲ or ▷ (left right cursor) or digit keys 0-9.
- If you want to change the TV channel name, press the (right cursor) key in line TV channel name.
- Select the character you want to change with the < (left cursor) or ▷ (right cursor) key.
- Change the character with the ∇ (down cursor) or △ (up cursor) key.
- Press OK to confirm.

This DVD recorder can receive HiFi sound transmissions in NICAM Stereo. However, if sound distorsion occurs, due to poor reception, you can switch off NICAM:

 In the line NICAM select On or Off with the < (left) cursor) or > (right cursor) key.

If you want to change the automatic TV channel setting, select the line fine tuning. With the 4 (left cursor) or (right cursor) key you can vary the automatic TV channel setting.

Important: This re-tuning is only necessary and useful in special cases, e.g. when stripes appear on your TV screen when using a cable-TV system.

- Press OK to store the TV channel.
- To end, press SYSTEM MENU.

Connecting a decoder:

- Switch on the TV set and select the programme number for the DVD recorder.
- Select the TV programme you wish to link with the decoder function with P+ or P-.
- Press SYSTEM MENU
- Select Installation
- Select Manual search Select Decoder.
- Select On with < (left cursor) or ▷ (right cursor).
- To end, press SYSTEM MENU.
- > 'DECODER' apperars on the display.

Sort/Clear TV channels manually

- If the DVD recorder is connected to the TV set. with Easy Link or a similar system, manual sort cannot be executed. In all other cases, you can
- Press SYSTEM MENU.
- Select the line 'Installation'
- Select the line 'Sort TV channels'.



- Select the TV channel to which you want to allocate a programme number (starting with P01) with the △ (up cursor) or ♥ (down cursor) key and press the (right cursor) key.
- Select the desired position with △ or ▽ (up down) cursor) key.
- To store, press OK.
- To end, press SYSTEM MENU.

To adjust 'Time', 'Year', 'Month' and 'Date' with the digit keys 0-9. Switch between fields with the $\nabla \triangle$ (down up cursor) keys



Recording

Before you start recording

Recordings on a disc are started from the position of the so-called disc pointer, i.e. the point where the last recording was stopped. From there on earlier recordings may be overwritten without notice, unless the disc is write protected. In this respect your DVD recorder behaves just like a Video Cassette Recorder.

In the Index Picture Screen you can select the point where you want to start your recording. Use the $\nabla \Delta$ (down up cursor) and ← REVERSE/→ FORWARD keys. You can see the the current location on the disc bar, indicated by the arrow.

Your DVD recorder always checks the disc that you have inserted:

- ➤ When a DVD+RW disc is inserted on which recordings have been made, the Index Picture Screen is shown on your TV screen.
- > If the inserted disc is a completely empty recordable disc, the message EPP13 EISE appears, on
- ➤ If the inserted disc is a DVD+RW disc with a content that is not DVD video compatible (e.g. a data disc), a dialog box is shown with the option to erase or eject the disc. You can only record on this disc after erasing it with the RECORD key.

Note: On a disc containing PAL recordings, no NTSC recordings can be made and vice versa. On an empty disc, either type of recordings can be made.



> A disc can hold up to 48 titles (including empty titles). When this maximum is reached the onscreen message 'Too many titles' appears, if you want to make a new recording. You have to erase a title first next to an empty title. See 'Managing Disc Content'.

Switching on

- · Switch on the TV set and select the programme number that you have chosen for video playback (see operating manual for your TV set).
- Press () STANDBY/ON.
 - > The recorder display lights up. If you have not yet installed your DVD recorder, it will enter 'virgin mode'. In this mode you will have to set your personal preferences. (See 'virgin mode'.)



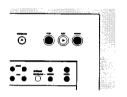
Manual recording

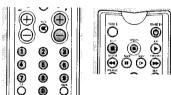
Checking input

Normally, the DVD recorder displays the contents of the disc on screen. Use the TUNER key in order to switch to the internal tuner, or whichever other source is selected, if you want to check the input before starting a recording. Press TUNER again to go back to disc mode.

Recording

- Insert a recordable DVD+RW disc.
- Use CHANNEL ▲ or CHANNEL ▼ (on the recorder) or P+, P- or the digit keys O-9 (on the remote control) to select the programme number (programme name) from which you wish to record.
 ➤ When a TV channel transmits a channel name, it will be shown on the display.





The following programme numbers are provided for recording from external sources:

'EXT1': TV set via SCART 1 socket

'EXT2': for recording from external sources via

SCART 2 socket

'EXT3': rear S-video 'EXT4': rear CVBS

'CAM1': front S-video

'CAM2': front CVBS

'CAM3': front DV.

- Press RECORD (on the recorder) or REC/OTR (on the remote control).
- RECORD is shown on the display.
- Press # STOP to stop recording.
- The Index Picture Screen is updated.
- > MENU UPDATE is shown on the display.

 After a short recording on a new disc, a few minutes will be needed to complete the formatting of the disc.

Direct record

- Make sure 'Direct record' is switched On. (See record settings).
- On the TV set, select the programme number you want make the recording from.
- Press RECORD (on recorder) or REC/OTR (on remote control) with the DVD recorder switched to standby.

Notes:

- Don't select another programme number on your TV set, until the NATT' on the display of your DVD recorder disappears. This can take up to one minute.
- When *NOTE' appears on the display, the programme number could not be found. The DVD recorder switches off automatically.
- If your loudspeakers are connected (via an amplifier / receiver) to your DVD recorder, the sound will be delayed relative to the TV picture when recording directly from the TV set.

Manual audio control

You can control the audio recording level of your DVD recorder manually.

- In tuner mode, press AUTO/MAN REC VOLUME on the DVD recorder.
- ➤ The display will show the current audio level and MANUAL appears.

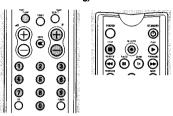


- Adjust the recording level with MANUAL ▲ or ▼
 on the DVD recorder, so that the '0 dB' mark lights
 up during the loudest parts of the recording.
- You can switch back to automatic audio level control by pressing AUTO/MAN REC VOLUME again.
 The display will show the current disc position and MANUAL disappears.

Note:

When DV input is selected, manual volume control is disabled.

Recording with automatic switch-off (OTR One-Touch Recording)



- Insert a recordable DVD+RW disc.
- Use CHANNEL ▲ or CHANNEL ▼ (on the recorder) or P+. P- or the digit keys 0-9 (on the remote control) to select the programme number (programme name) from which you wish to record.
- Press RECORD (on the recorder) or REC/OTR
 (on the remote control) twice.
 - ➤ A recording will be made of 30 minutes.
- The required end time of the recording is shown in the timer box on screen. The remaining recording time is shown in the status box on screen and on the display.



- Press RECORD or REC/OTR again to obtain a 30 minute increment.
- Shortly after pressing REC/OTR, OTR can be cancelled by pressing CLEAR.

Timer programming

The DVD recorder needs the following information for every programmed recording:

- the date on which the recording is to be made;
- the channel;
- the start and stop time of the recording;
- VPS/PDC on or off:
- the recording mode (HO, SP, LP or EP).

The DVD recorder stores all the information mentioned above in a timer block. You can programme up to six timer blocks, one month in advance.

What is 'VPS'/'PDC'?

With VPS/PDC*, the TV station controls the beginning and the length of the programmed recording. This means that the video recorder switches itself on and off at the right time even if a TV programme you have programmed begins earlier or finishes later than expected.

Usually the start time is the same as the VPS/PDC Time. If, however, in the TV guide, in addition to a TV programmes start time, a different VPS/PDC time is given, e.g.: 20.15 (VPS 20.14), you must enter '20.14' as the start time exactly to the minute. If you want to enter a time that differs from the VPS/PDC time, you must switch off VPS/PDC.

When all Timer blocks are full, the options timer programming and ShowView programming cannot be accessed. For clearing a timer block, see 'How to clear a timer block'.

Timer programming with 'ShowView'



A ShowView programming number is a number of up to nine digits, printed in most TV guides next to the start time of a TV programme.

All the information required for a programming is contained encoded in the ShowView programming number.

- Press TIMER on the remote control.
- Select 'ShowView programming' with △ (up cursor) or ▽ (down cursor).



Press ▷ (right cursor).

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- Enter the entire ShowView programming number (up to nine digits) printed in your TV guide next to the start time of a TV programme. If you made a mistake, you can correct it with CLEAR.
- Confirm with OK.
- If the ShowView system does not recognize the TV channel, the message 'Please enter programme number' will appear on screen. Select the required programme number (programme name) with ⊲ ▷ (left right cursor) and confirm with OK.



- ➤ The data will appear on the TV screen.

 Use SELECT to select the programming key at daily or weekly intervals. Mo-Fr. Recording at daily intervals from Mondays to Fridays inclusive. Weekly: Recording at weekly intervals on the same day of the weekly.
- Press ▷ (right cursor).
- Use SELECT to switch VPS/PDC on or off.
 When VPS/PDC is switched on, the start time is marked with an asterisk.
- Use SELECT to select the recording mode (HQ, SB, IB, IB)



- Confirm with OK.
- > The data has been stored in a timer block.
- To end, press TIMER.
- Make sure that you inserted a recordable disc. If you inserted a write-protected disc recording will be refused.
- Switch off with (1) STANDBY/ON.

Timer programming without 'ShowView'



- Press TIMER on the remote control.
- Select 'Timer programming' with △ (up cursor) or ∇ (down cursor).



- Press ▷ (right cursor).
- Enter the date with △ (up cursor) or ∇ (down cursor), or with the digit keys 0-9.

- If desired, select recording at daily or weekly intervals in the field 'Date' with SELECT. 'Mo-Fr': Recording to be made from Mondays to Fridays inclusive. 'Weekly': Recording at weekly intervals on the same day of the week.
- Press ▷ (right cursor).
- Enter the programme number from which you want to record. If you want to record from an external source, select EXT1 , EXT2 , EXT3 , EXT4 , CAM1 , CAM2 or CAM3 with △∇ (up down cursor).
- Press ▷ (right cursor).
- Enter the Start time with △▽ (up down cursor) or the digit keys 0-9.
- After entering the Start time, use SELECT to switch VPS/PDC on or off. With most TV stations the VPS/PDC time is always the same as the start time.
- ➤ When VPS/PDC is switched on, the start time is marked with an asterisk
- Press ▷ (right cursor).
- Enter the End time with △▽ (up down cursor) or the digit keys 0-9.
- Use SELECT to choose the recording mode HQ, LP, SP or EP.
- If you made a mistake, you can go back with <! (left cursor).



- Confirm with OK.
- ➤ The data has been stored in a timer block.
- To end, press TIMER.
- ➤ Make sure that you inserted a disc without write protection. If you inserted a write-protected (locked) disc recording will be refused.
- Switch off with () STANDBY/ON.

Programming with 'NexTVIEW Link'

This DVD recorder is equipped with the function 'NeXTView Link'. If your television is also equipped with this function, you can mark TV programmes on the television for programming. These TV programmes will automatically be transmitted to a timer block on the DVD recorder. If you clear the marking of the TV programme on the television, the corresponding timer block on the DVD recorder will also be cleared. For more information, read the instruction manual of your TV set.

If a timer setting is incorrect

The following warnings can be displayed in the timer

Collision

recording programme overlaps with another recording programme.

Solution:

- Ignore by pressing TIMER. The programme with the earlier start time will be recorded completely before the later programme starts.
- Edit one or both timers.
- Delete one of the recording programmes.

Please enter programme number

The ShowView system does not recognize the TV channel.

Solution:

- Select the required programme number (programme name) with dor b (left right cursor).
- Confirm with OK.

ShowView number wrong

You entered an incorrect ShowView programming number or the incorrect date.

Solution:

Repeat the entry or end by pressing TIMER.

Weekend programming - not possible

Date was incorrectly entered. Daily programming can only be used for recordings to be made from Mondays to Fridays inclusive.

Memory full

The maximum number of recording programmes is used. **Solution:**

Delete one of the recording programmes.

How to check or alter a timer block

- Press TIMER on the remote control.
- Select 'Timer list' with ∇ or △ (down up cursor).



Press ▷ (right cursor).



- Select the timer block you want to check or alter with ∇ or △ (down up cursor).
- Press ▷ (right cursor).
- Select what you want to check or alter with

 or

 (left right cursor).
- Confirm with OK.
- To end, press TIMER.
- Switch off by pressing () STANDBY/ON.

How to clear a timer block



- Press TIMER on the remote control.
- Select Timer list with ∇ or △ (down up cursor).
- Press ▷ (right cursor).
- Select the timer block you want to clear with ∇ or △ (down up cursor).
- Press CLEAR.
- Confirm with OK.
- Switch off by pressing TIMER.

Playback

Playing a pre-recorded DVD-Video disc



Some DVD discs are produced in a way that requires specific operation or allows only limited operation during playback. In these cases the recorder may not respond to all operating commands. When this occurs, please refer to the instructions in the disc inlay. When a $\boxed{\times}$ appears on the TV screen, the operation is not permitted by the recorder or the disc.

- Insert a pre-recorded DVD-Video disc.
 - ➤ When 'autoresume' is set to 'On' (see 'User Preferences') playback starts automatically from the point where it was stopped, the last time the disc was played.
 - ➤ When 'autoresume' is set to 'Off', the disc will play from the start of the disc. You can however resume play from the point at which you stopped, the last time the disc was played, by pressing
- ➤ PLAY when papears on screen.

 ➤ The currently playing title and chapter number are displayed on the recorder display. The elapsed time is shown also

Notes:

- Since it is usual for DVD movies to be released at different times in different regions of the world, all players have region codes and discs can have an optional region code. If you load a disc of a different region code to your recorder, you will see the region code notice on the screen. The disc will not play, and should be unloaded.

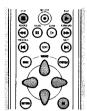


- The region code is stated on a label on the back side of your recorder.
 Regional coding is not applicable for recordable DVD discs.
- The disc may invite you to select an item from a menu. If the selections are numbered, press the appropriate numerical key; if not, use the ∇ △ ▷ △ (down up right left cursor) keys to highlight your selection, and press OK.

Note:

During playback you can display and enter the menu by pressing DISC MENU.

To stop play at any time, press
 STOP.
 The default screen will appear, giving information about the current status of the recorder.



Playing a (Super) Video CD disc



- Insert a (Super) Video CD.
 - ➤ When 'autoresume' is set to 'On' (see 'User Preferences') playback starts automatically from the point where it was stopped, the last time the disc was played.
 - ➤ The disc may invite you to select an item from a menu. If the selections are numbered, press the appropriate numerical key 0-9.
- To stop play at any time, press STOP.
 The default screen will appear.

(a) (b)

(BOI)

Search

 Use the ♥ (down cursor) keys to enter the fast. motion menu.



- Use the Use the (left right cursor) keys to select the required speed: -32, -8 or -4 (backward); 4, 8, 32 (forward).
- Select 1 to play at normal speed again.
- Press ► PLAY to exit fast motion mode.
- Press △ (up cursor) to delete the fast motion menu. To search forward or backward through different speeds. you can also press ← REVERSE or ► FORWARD

Repeat

again.



DVD Discs - Repeat chapter/title/disc

- To repeat the currently playing chapter, press REPEAT.
 - ➤ appears on screen.
- To repeat the currently playing title, press REPEAT a second time.
 - > title appears on screen.
- To repeat the entire disc, press REPEAT a third time.
 - > repeat appears on screen.
- To exit repeat mode, press REPEAT a fourth time.

Video CDs - Repeat track/disc

- To repeat the currently playing track, press REPEAT.
 - appears on screen.
- To repeat the entire disc, press REPEAT a second
- ➤ pepeat appears on screen. To exit repeat mode, press REPEAT a third time.

Playing a DVD+RW disc



Insert a DVD+RW disc.

➤ If the inserted disc is write-protected, playback starts automatically otherwise the Index Picture Screen appears.

Press ► PLAY.

> Playback starts automatically from the point where it was stopped the last time the disc was played or recorded. If you want to start playback from the beginning of the disc, you can do so via the Index Picture Screen (see 'Index Picture Screen'). If the disc is a new blank disc, the display will show 'EMPT' BISE'.

- With ⋈ PREVIOUS and ⋈ NEXT you can go to the previous or next title.
- To stop playback at any time, press STOP. You return to the Index Picture Screen.

General features





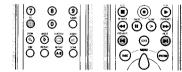




Note: Unless stated otherwise, all operations described are based on remote control operation. A number of operations can also be carried out via the system menu bar on the screen. (see 'System menu bar operation')

Moving to another title/track

When a disc has more than one title or track, you can move to another title as follows:



- Press ➤ NEXT during play to step forward to the
- Press ⋈ PREVIOUS during play to return to the beginning of the current title. Rapidly press M PREVIOUS twice to step back to the previous
- To go directly to any title or track, enter the title number using the numerical keys 0-9.

- If the number has more than one digit, press the keys in rapid succession.
- If the system menu bar is on screen, make sure the T icon is selected.





Moving to another chapter/index

When a title on a disc has more than one chapter or a track has more than one index, you can move to another chapter/index as follows:

- Press ► NEXT during play to select the next chapter/index.
- Press ► PREVIOUS during play to return to the beginning of the current chapter/index. Rapidly press ► PREVIOUS twice to step back to the previous chapter/index.
- To go directly to any chapter or index, enter the chapter or index number using the numerical keys 0-9.

- If the system menu bar is on screen, make sure the ${\sf C}$ icon is selected.

- If the number has more than one digit, press the keys in rapid succession.

Use <> ▷ (left right cursor) keys to select previous

You can also step forward by using the # PAUSE repeatedly on the remote control.

Slow Motion

motion menu.

• Select (Slow motion) in the system menu bar.

● Use the ♥ (down cursor) key to enter the slow

6 6 5 × 3

1 (2 14414)

1/8, 1/4, 1/2 or 1 (forward).

> SLOW key on the remote control.

Still Picture and Step Frame

(EM)

台

or next picture.

(H)

(-)

Select

Select 1 to play at normal speed again.

● Press ▶ PLAY to exit slow motion mode

➤ The recorder will now go into pause mode.

Use the ▷ (left right cursor) keys to select the

• If II PAUSE is pressed, the speed will be set to 0.

Press △ (up cursor) to delete the slow motion menu.

(picture by picture) in the system menu

Use the ∇ (down cursor) key to enter the picture

➤ The recorder will now go into pause mode.

You can also select Slow motion speeds by using the

required speed: -1, -1/2, -1/4 or -1/8 (backward);

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Directions For Use

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Repeat A-B



To repeat or loop a sequence in a title:

- Press REPEAT A-B at your chosen starting point;
- ➤ appears on screen.
- Press REPEAT A-B again at your chosen end
- ➤ repeat appears on screen, and the repeat sequence begins.
- To exit the sequence, press REPEAT A-B.

Scan



Plays the first 10 seconds of each chapter/index on the disc

- Press SCAN.
- To continue play at your chosen chapter/index, press SCAN again or press ▶ PLAY.

Time search

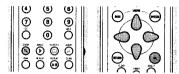
The Time Search function allows you to start playing at any chosen time stamp.

- Select (Time Search) in the system menu bar.
- Press ∇ (down cursor).
 - ➤ The recorder will now go into pause mode. > A time entry box appears on the screen showing the elapsed playing time of the current disc.



- Use the digit keys 0-9 to enter the required start time. Enter hours, minutes and seconds in the box. > Each time an item has been entered, the next item will be highlighted.
- Press OK to confirm the start time. ➤ The time entry box will disappear and play starts from the selected time position.

Zoom



The Zoom function allows you to enlarge the video image and to pan through the enlarged image.

- Select ⊕ Zoom in the system menu bar.
- function and select the required zoom factor; 1.33 or 2 or 4.
- ➤ The recorder will go into pause mode.
- > The selected zoom factor appears below the Zoom icon in the system menu bar and 'Press OK to pan' appears below the system menu bar.



- ➤ The picture will change accordingly.
- Press OK to confirm the selection. ➤ The panning icons appear on the screen: ∇ △ ▷ (down up right left cursor) and OK.
- Use the ∇△▷
 (down up right left cursor) keys to pan all over the screen.
- When OK is pressed only the zoomed picture will be shown on the screen.
- If you wish to zoom at any moment, press ⊕ Zoom and select the required zoom factor as described
- Press ➤ PLAY to exit zoom mode.

Special DVD-Video features

Menus on the disc

For titles and chapters, selection menus may be included on the disc.

The DVD's menu feature allows you to make selections from these menus. Press the appropriate numerical key; or use the ♥ △ ▷ ♦ (down up right left cursor) keys to highlight your selection, and press OK.

Title menus



- Press DISC MENTI
- > If the current title has a menu, this appears on the screen. If no menu is present in the title, the disc menu will be displayed.
- The menu can list camera angles, spoken language and subtitle options, and chapters for the title.
- To exit the title menu, press DISC MENU again.

Note: Most DVD discs do not have seperate disc and title menus, but only a disc menu.

Disc menu



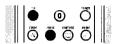
- Press T/C followed by DISC MENU.
- > The disc menu is displayed.
- To remove the disc menu, press DISC MENU again.

Camera Angle

If the disc contains sequences recorded from different camera angles, the angle icon appears, showing the number of available angles, and the angle being shown. You can then change the camera angle if you wish.







- Use the ∇ △ keys to select the required angle in the angle icon.
- To go to any angle directly, enter the angle number using the numerical keys 0-9.
- After a small delay, play changes to the selected angle. The angle icon remains displayed until multiple angles are no longer available.

Changing the audio language



- Select of (Audio) in the system menu bar.
- Press (AUDIO or ♥ △ (down up cursor) repeatedly to step through the different languages.
- You can enter the required language number directly using the numerical keys 0-9.



Subtitles



- Select (Subtitle) in the system menu bar.
 Press SUBTITLE or ∇ △ (down up cursor)
- repeatedly to step through the different subtitles or to switch subtitles off.
- You can enter the required subtitle number directly using the numerical keys 0-9.



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2

Directions For Use

DVDR1000 /0x1 /691

GB

Repeat track/disc



- To repeat the currendy playing track, press REPEAT.
- ➤ Repeat track appears on screen.
- To repeat the entire disc, press REPEAT a second time.
- ➤ Repeat disc appears on screen.

 To exit repeat mode, press REPEAT a third time.

Repeat A-B



To repeat or loop a sequence:

- Press REPEAT A-B at your chosen starting point;
 Repeat A appears on screen.
- Press REPEAT A-B again at your chosen end point;
 - ➤ Repeat A-B appears on the display, and the repeat sequence begins.
- To exit the sequence, press REPEAT A-B again.

Scan

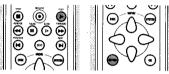


Plays the first 10 seconds of each track on the disc.

- Press SCAN.
- To continue play at your chosen track, press SCAN again or press > PLAY.

Special VCD features

Playback Control (PBC)



- Make sure PBC is switched On. See 'User Preferences-features settings'.
- Load a (Super) Video CD with PBC and press
 PLAY.
- ➤ The PBC menu appears on screen.
- Go through the menu with the keys indicated on the TV screen until your chosen passage starts to play.
 If a PBC menu consists of a list of titles, you can select a title directly.
- Enter your choice with the numerical keys 0-9.
- Press RETURN to go back to the previous menu.

Playing an audio CD

- Insert the disc.
- ➤ After loading the disc, playback starts automatically.
- ➤ If the TV set is on, the Audio CD screen appears.
 ➤ During play, the current track number and its
- ➤ During play, the current track number and its elapsed playing time will be shown on the screen and the recorder display.



To stop play at any time, press
 STOP.
 The number of tracks and the total playing time will be shown on the screen and the recorder display.

Moving to another track

desired.

FORWARD.

➤ Search begins.

or >> FORWARD again

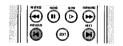
or >> FORWARD again.

▶ FORWARD is pressed.

Pause

Press II PAUSE during play.

To return to play, press ► PLAY.



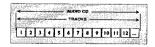
To search forwards or backwards through the disc

● To return to 4x normal speed, press ◄ REVERSE

To end the search, press ➤ PLAYor ■ STOP as

> Search goes to 8x speed, and the sound is muted.

- Press MNEXT during play to step forward to the next track.
- Press ► PREVIOUS during play to return to the beginning of the current track. Rapidly press ► PREVIOUS twice to step back to the previous track.
- To go directly to any track, enter the track number using the numerical keys 0-9.



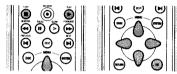
Access control

Child Lock (DVD and VCD)

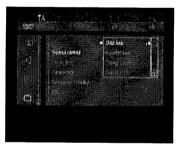
When activating Child lock, only discs that are authorised can be played without PIN code.

The recorder memory maintains a list of 50 authorized ('Child safe') disc titles. A disc will be placed in the list when 'Play Always' is selected in the 'Child protect' dialog. Each time a 'Child safe' disc is played it will be placed on top of the list. When the list is full and a new disc is added, the least recently used disc will be removed from the list.

Activating/deactivating the child lock



- Select Access control in the features menu using ∇ △ (down up cursor) and press ▷ (right cursor).
- Enter a 4-digit PIN code of your own choice using the digit keys 0-9.
- Enter the code a second time.



- Select using \(\sigma \) (down up cursor).
- Press OK or d (left cursor) to confirm and press SYSTEM MENU to exit the menu.
 ➤ Now unauthorized discs will not be played unless the 4-digit code is entered.
- Select to deactivate the Child Lock.

Note: Reconfirmation of the 4-digit PIN code is necessary when: The code is entered for the very first time (see above); The code is changed (see 'Changing the 4-digit code'); The code is cancelled (see 'Changing the 4-digit code'); Both Child Lock and Parental Control are switched Off and the code is requested.

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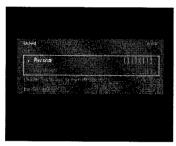
Authorizing discs when Child Lock is activated

Insert the disc.

The 'Child protect' dialog will appear. You will be asked to enter your secret code for 'Play once' or 'Play always.' If you select 'Play once', the disc can be played as long as it is in the recorder and the recorder is in the On position. If you select 'Play always', the disc will become Child safe (authorized) and can always be played even if the Child lock is set to On.

Note: Double sided DVD discs may have a different ID for each side. In order to make the disc 'Child safe', each side has to be authorized.

Multi volume VCD disc may have a different ID for each volume. In order to make the complete set 'Child safe', each volume has to be authorized.



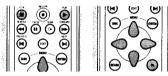
Securing discs

- Insert the disc.
- Playback starts automatically.
- Press STOP while ③ is visible.
- will appear and the disc is now banned i.e. it is not Child safe any longer.

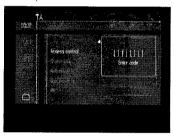
Parental Level (DVD-Video only)

Movies on pre-recorded DVD discs may contain scenes not suitable for children. Therefore discs may contain "Parental Control" information which applies to the complete disc or to certain scenes on the disc. These scenes are rated from 1 to 8 and alternative, more suitable scenes are available on the disc. Ratings are country dependent. The "Parental Control" feature allows you to prevent discs from being played by your children or to have certain discs played with alternative scenes.

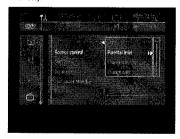
Activating/Deactivating Parental Control



 Select Access control in the features menu using ∇ △ (down up cursor) and press ▷ (right cursor).



- Enter your 4-digit PIN code using the digit keys 0-9.
 If necessary enter the code a second time.
- Move to Parental level using ∇ △ (down up cursor).
 Move to the Value Adjustment bar using ▷ (right cursor).



 Use the ∇ △ (down up cursor) keys or the numerical keys 0-9 on the remote control to select a rating from 1 to 8 for the disc inserted.
 Rating 0 (displayed as '--'):

Parental Control is not activated. The disc will be played in full

Rotings 1 to 8 (1 = childsofe - 8 = adults only): The disc contains scenes not suitable for children. If you set a rating for the recorder, all scenes with the same rating or lower will be played. Higher rated scenes will not be played unless an alternative is available on the disc. The alternative must have the same rating or a lower one. If no suitable alternative is found, play will stop and the 4-digit code has to be entered.

Press OK or < (left cursor) to confirm and press
 SYSTEM MENU to exit the menu.

Country

- Select Access control in the features menu using ∇ △ (down up cursor) and press ▷ (right cursor).
- Enter the four digit PIN code.
- Press ▷ (right cursor).
- Select a country using ∇ △ (down up cursor).

Changing the 4-digit code

- Select Access control in the features menu using ∇ △ (down up cursor) and press ▷ (right cursor).
- Enter the old code.
- Move to Change code using ∇ (down cursor).
- Press ▷ (right cursor).
- Enter the new 4-digit PIN code.
- Enter the code a second time and reconfirm with
- Press SYSTEM MENU to exit the menu.

Note: If you forgot your code, press **STOP** four times while in the access control PIN code box and exit with **OK**. Access control is now switched off. You can then enter a new code as described above.

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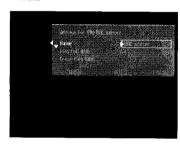
Managing disc content

Title settings

For each title on the discs the default settings can be changed to your personal preference in the title settings

Changing the title name

- In the Index Picture Screen, select the required title with $\nabla \triangle$ (down up cursor).
- Press > (right cursor) to enter the title settings



- Enter the new name. A name may contain a maximum of 64 characters.
- Use < □ (left right cursor) for the position of the characters. Use ♥ △ (down up cursor) to change
- Use SELECT to toggle between capitals and lower case characters.
- Confirm by pressing OK.

Play full title

- In the Index Picture Screen, select the required title with $\nabla \Delta$ (down up cursor)
- Press > (right cursor) to enter the title settings menu
- Select 'Play full title'.

When this item is selected the title will be played in full, including hidden chapters. Follow the instructions on the screen. (See 'Operation - managing disc content -Current chapter')

Erasing a title

You may simply erase a title by recording over it, but if you want to erase the whole title instantly, do the following:

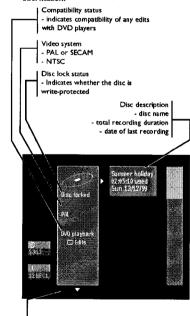
- In the Index Picture Screen, select the required title with $\nabla \triangle$ (down up cursor).
- Press > (right cursor) to enter the title settings
- Select Erase this title: > The message 'This will completely erase this title, Press OK to confirm is shown.
- Press OK to confirm.
- > 'Erasing title...' is shown until the action is completed.

> After the title has been erased, the Index Picture Screen will show an empty space instead. If there was an empty space in front of or behind this title. then these are combined into one empty space. Empty spaces of less then one minute will not be

Disc Info Screen

- When on the Index Picture Screen, press STOP or keep is PREVIOUS pressed for about two seconds.
- > You are now on Title 1. Press △ (up cursor).
- > You enter the Disc Info Screen.
- Press ♥ (down cursor) to exit the Disc Info Screen.

The Disc Info Screen contains the following information:



Cue to go back to the Index Picture

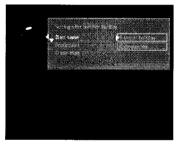
Disc Settings

For each disc the settings can be changed to your personal preference in the disc settings menu.

- In the Disc Info Screen press > (right cursor).
- > You will now enter the 'disc settings' menu.

Changing the Disc Name

 In the Disc Info Screen press ▷ (right cursor). ➤ You will now enter the 'disc settings' menu.



- Enter the new name. A name may contain a maximum of 64 characters.
- Use ▷ (left right cursor) for the position of the characters. Use the $\nabla \Delta$ (down up cursor) keys to change characters.
- Use SELECT to toggle between capitals and lower case characters.
- Confirm by pressing OK.

Protection of recordings

- In the Disc Info Screen press ▷ (right cursor). > You will now enter the 'disc settings' menu.
- Select Protection and press ▷ (right cursor).
- Select 'Protected' with $\nabla \triangle$ (down up cursor).
- Press OK on the remote control to confirm.
- > No further changes can be made to the disc. It will also disable most title/disc manipulation screen entries, as well as the complete edit menu.
- > Future editing is only possible after resetting the Protection feature to 'Unprotected' again.

Erasing a disc

- In the Disc Info Screen press ▷ (right cursor).
 You will now enter the 'disc settings' menu.
- Select 'Erase disc' and press OK.
 The message 'This will erase all titles' is displayed.
- Press OK to confirm or < (left cursor) to cancel.
 ➤ 'Erasing tissc' is shown until the action is completed.
 - ➤ After the disc has been erased the Index Picture Screen will show the free space on the disc.

Making your edits DVD-compatible

If one or more titles have been edited (see 'Favourite Scene Selection'), then the edits will play on your DVD recorder, but a DVD player may show the original versions instead of the edits. You can prepare your discs so that also a DVD player will show the edited version.

 If the Disc Settings menu shows the option 'Make edits DVD-compatible', select this option. If the menu does not show this option, then your disc is already compatible, and no conversion is needed.



- Press OK on the remote control to confirm.
 The messages 'This will take ...' and 'Press OK to confirm' will appear to indicate how long the action will take.
- Press OK on the remote control to confirm.
 'Processing...' and a progress bar are shown until the action is completed.

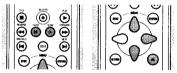
Favourite Scene Selection

With the EDIT key on the remote control the Favourite Scene Selection (FSS menu) for editing functionality can be called up. The basic function of any edit operations is to improve accessibility and handling of your recordings. For instance: scenes you do not want to see during playback (e.g. commercials during a movie) can be marked as chapters and made hidden. During playback you will see your recording without the hidden chapters as one sequence.

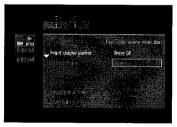
Note: In between the scenes the picture may freeze for a short moment.

Each title consists of chapters. With the FSS menu any chapter can be made hidden or made visible again. Normally, during recording, chapter markers are inserted automatically every five to six minutes (this setting can be changed in the record settings menu). After the recording is finished, you can manually add and remove chapter markers via the FSS menu. Both automatically generated and manually inserted chapter markers can be removed.

Edit in playback mode



 Press the EDIT key on the remote control.
 The video image is overlayed with a transparant edit menu. Title and chapter information appear in an information box at the top of the screen.



 Use ∇ or △ (down up cursor) to toggle through the menu's functions:

Insert chapter marker

To insert a chapter marker on the current position of the title that is playing.

• Press OK on the remote control to insert a marker. The maximum number of chapter markers per tide is 99. Per disc the maximum number of chapter markers is 254. When this maximum is reached the on-screen message Too many chapters' appears. You have to delete some, before inserting new chapter markers.

Hide chapters

Initially all chapters are visible. You can hide chapters or make them visible again on playback. In edit mode however hidden chapters are displayed in a dimmed mode.



- Select Visible or Hidden with the ▷ (right cursor) keys.
- Press OK on the remote control to confirm.

Delete chapter marker

To delete the chapter marker at the beginning of the current chapter.

Press OK on the remote control to confirm.
 Deleting markers' will appear.

Delete all markers in title

To delete all chapter markers (manually and automatically generated) for this title.

Press OK on the remote control to confirm.
 Deleting marker5' will appear.

Use picture as index

To define the current video frame as a miniature picture to be used for this title's entry in the Index Picture Screen.

- You can use II PAUSE and/or ▷ SLOW to
- accurately choose the desired picture.

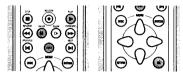
 Press OK on the remote control to confirm.

 'Updating menu'.

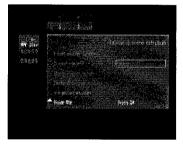
After editing, the modified version of a title is the default playback version. The original can be accessed via the 'Play full title' option in the title settings menu. Other DVD players may still play the original. To guarantee that the edited version will play on these DVD players, choose 'Make edits DVD-compatible' in the disc settings menu.

Divide a title

If you want to divide one title into two seperate titles, do the following:



- On the Index Picture Screen, select the title you want to divide.
- Press ► PLAY.
- Go to the point where you want to divide the title and press II PAUSE.
- Press EDIT.
- ➤ The Favourite Scene Selection menu is shown.
- Select 'Divide title'.



Press OK on the remote control to confirm.
 Dividing title...' is shown until the action is completed. This divide operation cannot be undone.

The Index Picture Screen will show two titles instead of one. Both will have the same name. If you want to change the name, you can do so in the title settings menu. For one of the two resulting titles, a new index picture is created.

If you want to divide one title into more than two titles, use the above procedure several times.

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50 MANAGING DISC CONTENT

If you want to append a video recording to an earlier recorded title, do the following.

- On the Index Picture Screen, select the title to which you want to add a video recording.
- Press ► PLAY.
- At the point where you want to append the title press # PAUSE.
- To monitor the video input you may press TUNER.
- Press RECORD (on the recorder) or REC/OTR (on the remote control).

The video recording will now be appended from this point. Video material beyond this point is overwritten. This may include titles following the current title.

Any remaining video material that is not overwritten, which may include the last part of the original title, is maintained. You can access these titles from the Index Picture Screen.

Edit in record mode

- Press the EDIT key on the remote control during recording.
- ➤ A chapter marker is inserted at the current position. 'Inserting marker' appears in the status box at the top of the screen. The maximum number of chapter markers per title is 99. Per disc the maximum number of chapter markers is 254. When this maximum is reached the on-screen message. 'Too many chapters' appears. You have to delete some, before inserting new chapter markers.



If it appears that the DVD recorder is faulty, first consult this checklist. It may be that something has been overlooked. Under no circumstances attempt to repair the system yourself; this will invalidate the warranty. Look for the specific symptom(s). Then perform only the actions listed to remedy the specific symptom(s).

Symptom	Remedy
The recorder does not respond to the remote control	The remote control may be configured for a second DVD recorder.
	Hold SELECT+1 pressed simultaneously to revert to DVD recorder 1 Aim the remote control directly at the sensor on the front of the recorder.
	Avoid all obstacles which may interfere with the signal path. Inspect or replace the batteries.
No power	Check if both plugs of the mains cord are properly connected. Check if there is power at the AC outlet by plugging in another appliance.
No picture	Check if the TV set is switched on. Check the video connection.
Distorted picture distorted sound	Check the disc for fingerprints and clean with a soft cloth, wiping from centre to edge.
	Sometimes a small amount of picture distortion may appear. This is not a malfunction.
Recorder does not play disc	Ensure the disc label is upwards and that the right disc type is inserted. Clean the disc.
	Check if the disc is defective by trying another disc
	Check if the region code of the disc matches the region code of the
	recorder. (pre-recorded DVD discs only). See 'playing a pre-recorded
	DVD-Video disc'. Check if Child Lock is activated.
No sound	Check audio connections.
	If using a HiFi amplifier, try another sound source.
Distorted sound from HiFi amplifier	Check to make sure that no audio connections are made to amplifier phono input.
	Check to make sure that analogue input of the amplifier is not connected to the digital output of DVD the recorder.
Distorted or black and white picture with	
DVD or Video CD disc	The disc format is not according to the TV set used (PAL/NTSC).
No audio at digital output	Check the digital connections.
	Check the settings menu to make sure that the digital output is set to on.
	Check if the audio format of the selected audio language matches your
	receiver capabilities.
Keys on the DVD recorder do not work	Disconnect and reconnect the DVD recorder from the mains. If this
	does not solve the problem. Check if the remote control still works. If
	so, the recorder is probably in trade mode. Disconnect the recorder from the mains and reconnect it while holding A OPEN/CLOSE and
	STOP pressed.
Recorder does not respond to all	
operating commands during playback	Some operations are not permitted by the disc. Refer to the

instructions in the disc inlay.

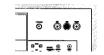
No new title can be recorded	Check if the maximum number of titles has been reached (message: 'too many titles' on screen). If so, delete a title next to a free space. Check if the disc is write protected. If so, unlock the disc in the disc settings menu (message: 'Disc locked' on screen).
Two languages are 'mixed' when recording from a stereo VCR	When the TV set does not automatically detect the dual-language signal, use left/right audio balance on the TV set to amplify the one or the other language.
The disc cannot be erased because the Index Picture Screen does not appear	Open the tray while leaving the disc in. Hold CLEAR pressed for around 5 seconds. The tray closes and the disc will be erased.
The Index Picture Screen does not appear but the titles on the disc can still be played	Take out the disc. Clear the disc. Insert the disc. Choose 'Adapt to own disc format' (See 'User Preferences - Features).
A DVD player shows the Index Picture Screen but does not react to the PLAY key	Press ■ STOP to exit the Index Picture Screen, then press ▶ PLAY.

Diagnosis programme

If the recorder is still faulty you can start the Diagnosis Programme in the recorder.

You can operate the Diagnosis Programme by following the instructions step by step.

Instructions



- Unplug the power cord of the recorder.
- Press the PLAY key and keep them pressed while you plug the recorder.
 - ➤ On the display the message BUSE appears together with a counter. This counter indicates the termination of the test when zero is reached. After a few minutes the message on the local
 - display changes over from BUSY to FAIL or to
 - ➤ If the message FAIL appears on the display. there is apparently a failure in your recorder and your recorder should be repaired.
- Consult your dealer or the Philips Customer Care Centre for the nearest Service Repair Shop in your country. The phone number is given in your warranty booklet.
- If the message PRSS appears on the display, there is apparently no failure in your recorder, in this case the failure can be caused by incorrect interpretation of the operating instructions or a wrong disc is used or your recorder is not correctly connected. In this case you should consult your dealer or the Philips Customer Care Centre for further assistance in solving the problem.
- If the problem remains, then consult your Philips Customer Care Centre.

System limitations

A DVD+RW disc may not play on certain DVD Video

A DVD+RW video disc that has been recorded on a different type or brand of recorder can be played, but may not provide all features commonly available to DVD+RW discs, such as the on-screen disc bar, the disc settings menu, the title settings menu, and editing. Refer to 'Adapt disc format'. If the disc is writeprotected, the status cannot be changed.

When using manual recording, the DVD recorder will warn before adapting the format of the disc or removing non-video data. When using timer recording however, the DVD recorder will always start to record, unless the disc is write-protected. Menus, edits and other data recorded on a different device (e.g. a PC) may be lost.

Because of the Variable Bit Rate, a title map take up less or more space than the overwritten title, even though the duration is the same. As a result, a part of the original title may remain, or a part of the next title may be lost. The maximum deviation is five minutes.

After a power interruption during recording, the Index Picture Screen will may not match with the actual video content on the disc. The last recorded title may be lost.

Glossary

This section explains most important terms, abbreviations, and acronyms used in this document.

Term	Explanation	
AC-3	Audio Coding 3, also known as Dolby Digital, Multi-channel digital audio compression system from Dolby Labs.	
A/V	Audio∕Video	
Chapter	A part of a title.	
Disc Bar	A graphical representation of the contents of a (DVD+RW) disc.	
Disc Pointer	An arrow indicating the current playback/recording position on the DVD+RW disc, displayed on the 'disc bar'.	
DTS	Digital Theater System, A high-end Multi-channel audio compression format.	
DV	Digital Video. A camcorder format for high-quality video, different from MPEG. It is converted into MPEG 2 Video when recorded on DVD+RV	
DVD	Digital Versatile Disc	
DVD+RW	DVD+ReWritable. The disc standard used by the DVD recorder.	
EasyLink	If your TV set and your video recorder are equipped with this feature, they can exchange information to adjust certain settings to each other, such as the TV channel order and other user preferences.	
I.LINK	Also known as 'FireWire' and 'IEEE 1394'. A cable for transfer of high- bandwidth digital signals, as used by Digital Video camcorders.	
Index Picture Screen	A screen that gives an overview of a DVD+RW disc, with 'index pictures' that each represent a recording.	
MPEG	Motion Picture Experts Group. A collection of compression systems for digital audio and video.	
NexTView Link	A system that enables easy programming of a video recorder via a TV set. Also see EasyLink.	
NICAM	System for reception of digital stereo TV sound.	
NTSC	See TV system.	
OSD	On-screen Display. The 'user interface' by which you can control the DVD recorder via the TV screen.	
OTR	One-Touch Recording. With this feature you can easily start a recording (by pushing just one button) and select the switch-off time in intervals of 30 minutes.	
PAL	See TV system.	
roc	Prayback Control. A special feature on a VCD 2.0 or Super VCD disc that enables interactive use.	
РСМ	Pulse Code Modulation. A digital audio encoding system.	

Program Delivery Control
Red-Green-Blue. A top-quality video connection where red, green and blue components of a video signal are carried through separate wires.
Also known as Euro-AV cable, This standard cable is an easy way to connect various AV devices and televisions. In addition to audio and video it can carry control signals.
See TV system.
A system by which you can easily program the Timer of your DVD- recorder by entering a code of maximum nine digits, which is printed in TV guides. 'ShowView' is a trademark of Gemstar Development Group.
Sometimes also called S-VHS or Super-VHS. A high-quality video connection standard.
It is the name given to the unit of recording on the disc. A title, typically, represents one recording.
A system for simulating Multi-channel sound reproduction via a two- channel set-up, by SRS Labs, Inc.
There are various systems for transmitting television signals, for example PAL, PAL-I, PAL-BG, SECAM, SECAM-DK, NTSC, etc. The TV system is country dependant.
Video Compact Disc
Video Cassette Recorder
Video Programming System

Appendix

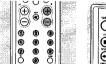
Using your DVD recorder remote control with your TV set

Your DVD recorder remote control can transmit several commands to TV sets of different brands. The following keys will always operate the TV set:



- - + increase TV volume - - decrease TV volume - 🕸 mute TV

Some other keys normally operate the DVD recorder, but will operate the TV set when you keep the button on the side of the remote control pressed:



next TV programme number previous TV programme number -0-9 choose TV channel

- Ф switch TV to standby

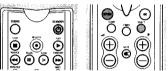
Remote control set-up codes	BSR321
for television	BTC
ioi television	
AOC046, 057	Bang & Olufsen 592
Acura	Basic Line 036, 245
Admiral 120, 490	Baur 064, 037, 581
	Baysonic
Adyson	Beaumark 205
Aiko	Beko
Akai	Belcor046
Akura 245, 291	Bell & Howell 181
Alaron	Beon
Alba 064, 036, 245, 063, 398	Binatone 244
Allorgan 321	Blaupunkt 581
America Action207	Blue Sky 245
Amplivision 244	Blue Star
Amstrad 198, 398, 036, 064	Boots 244
Anam 207, 036	Bradford 207
Anitech	Brandt
Arcam	Britannia 243
Asuka 245	Brockwood046
Atlantic 233	Broksonic 263, 490
Audiosonic 064, 136	Bush 064, 398, 245, 036, 063,
Audiovox 119, 207, 478	
Autovox 233	CCE
BPL309	CS Electronics 243

58 APPENDIX

If your TV set does not respond to the remote control. you can re-programme your remote control. Below you will find a list of all available remote control codes for various TV brands. The following procedure reprogrammes your remote control:

- Look up the set-up code for your TV set in the code list below.
- Press and hold the RETURN and SELECT key simultaneously for at least 3 seconds.
- Release both keys.
- Enter, within 30 seconds, the correct three-digit code with the digit keys 0-9.
- If the selected code does not work with your TV set, or if the brand of your TV set is not in the list, try out the codes one after the other.

Alternative procedure:



- Switch on your television set.
- Press and hold the RETURN and SELECT key simultaneously for at least 3 seconds.
- Release both keys.
- Point the remote control to your TV set.
- Press and hold the (1) STANDBY key. ➤ Your TV set switches off when the right code is
- When your TV set switches off, immediately release the (1) STANDBY key.
- > Your remote control is now re-programmed.
- This complete procedure may take up to 2 minutes.

CXC207	172, 181, 193, 478
Candle 057, 083	Cybertron
Carnivale	Daewoo 119, 046, 401, 478,
Carrefour	
Carver	Dainichi
Cascade 036	Dansai
Cathay	Dayton 036
Celebrity	Daytron 046
Centurion	Decca 064, 099
Cimline	Denon 172
Cineral 478, 119	Dixi
Citizen 083, 057, 066, 087,	Dual Tec
	Dumont044, 046, 097
Clarivox	Electroband027
Clatronic	Elin 064
Concerto	Elite
Condor	Elta 036
Contec 036, 063, 207, 243	Emerson 263, 207, 205, 206,
Craig	490, 309, 066, 046, 181
Crosley	Envision
rown 397, 036, 064, 066,	Erres 039, 064
207, 445	Expert
Crystal 458	Ferguson 136, 064
Curtis Mathes 087, 057, 066,	Fidelity 243
074, 078, 081, 083, 120,	Finlux. , 064, 132, 097, 099, 206

Firstline 348, 036, 243, 244,	Koyoda 036	Philco . , 172, 046, 057, 081, 490	Siemens
,	LG083	Philips 064, 039, 081, 401, 581	Silver
Fisher 244, 181, 397	LXI 181, 074, 081, 183, 205	Phonola	Sinudyne 129, 037, 321
Flint	Leyco 099, 064, 291, 321	Pilot 046, 057, 066	Sonoko 036, 064
Formenti 347, 064	Liesenk & Tter 064	Pioneer 136, 193	Sontec
Frontech 458, 291	Luma	Portland 046, 066, 119	Sony 037, 063, 027
Fulltsu 206, 099, 233	Luxman	Prism	Soundesign 205, 206, 207
Funal 321, 198, 206, 207, 291	M Electronic 132, 244, 036,	Profex	Soundwave 064, 445
Futuretech 207	064, 136, 401	Proline 348	Squareview 198
GE 048, 074, 078, 205, 478,	MGA 177, 046, 057, 205	Proscan 074	Standard 244, 245, 036
	MTC 087, 057, 046, 083, 243	Protech 064, 129, 036, 458,	Starlite 207
GEC 099, 064, 244	Magnadyne 129	244, 291, 445	Stern
GPM245	Magnafon129		
		Proton 205	Sunka+
Geloso 036	Magnavox 081, 057, 063, 206	Pulsar 044, 046	Supra
Genexxa 245	Manesth 347, 244, 291	Pye	Supreme
Gibralter 044, 046, 057	Marantz 064, 081, 057		
		Quasar 078, 277, 192, 677	Susumu 245
GoldStar 064, 046, 057, 205,	Mark	Quelle 064. 097, 037, 581	Sylvania 081, 057
244, 083, 136	Matsul . 036, 064, 244, 398, 062,	Questa 063	Symphonic 198
Goodmans 064, 099, 206,			
		R-Line064	Sysline
398, 063, 244, 401	Matsushita	RBM	TMK 083, 205
Gorenje	Mediator 039, 064	RCA 074, 046, 078, 117, 120	Tandy 245, 099, 244, 120
Gradiente 083, 080	Megatron 172, 205	Radio Shack 192, 207, 057,	Tashiko 063, 244
Gramda 064, 099, 244	Memorex 205, 036, 083, 177,	205, 066, 181, 046,	Tatung 099, 244, 064
Grandin	181, 277, 490	074, 083	Tec244
Grundig 097, 581, 064	Midland 044, 066, 074, 078	Radiola 064, 039	Technema 347
Grunpy 206, 207	Minerva	Rank Arena	Technics 078, 277, 677
HCM036, 309	Minutz048	Realistic 192, 207, 181, 057.	
			Technol Ace 206
Hallmark 205	Mitsubishi 063, 135, 177, 205.	066, 205, 046, 083	Techwood 078, 083
Hanseatic	046, 120	Revox	Teknika 081, 206, 207, 046,
Harley Davidson 206	Mivar243	Rex 233, 291	066, 119, 083, 087, 177
Harman/Kardon 081	Motorola120	Rhapsody 243	Telefunken
Harvard	Multitech 036, 129, 207, 243,	Roadstar 036, 291, 245, 445	Telemeister
Hinari 036, 063, 064, 245,		Runco 044, 057	Teletech
	NAD 183, 193, 205	SBR 039, 064	Teleton 233, 063, 244
Hisawa	NEC 057, 063, 046, 083, 482	SEG 244, 063, 291	Tensal 245, 321, 347
Hitachi 136, 071, 172, 244,			
	NEI	SEI 129, 037, 321	Texet243, 245
	NTC119	SKY	Thomson
Huanyu 243, 401	Neckermann 064, 581	SSS 046, 207	Thorn 064, 062, 099
Hypson 291, 064, 309	Nesco	Saba	Tomashi 309
ICE , , . , 244, 291, 398	Netsat	Saisho 036, 291, 458	Toshiba 062, 183, 063, 097,
ICeS 245	Nikkai . 064, 062, 245, 099, 243,	Sambers 129	087, 181
ITS 398		Sampo 057, 066	Totevision
Imperial	Nikko 205, 057, 119	Samsung 064, 046, 205, 244,	Uher 233, 347
Indiana	Nobiko129	291, 397, 036, 057,	Ultravox 129
Infinity	Nordmende	066, 083, 087, 117	Universum 132, 064, 291, 397
Inno Hit	Onwa 207	Sams ux	Vector Research 057
Innova	Optimus 277, 193, 181, 677	Sandra	Vestel 064
Inteq044	Optonica 120, 192	Sansel 478	Victor
Interfunk	Orion . 321, 490, 064, 206, 263,	Sansul	Videotechnic 244
Intervision 064, 129, 244, 291		Sanyo 181, 063, 099	Vidikron
Isukat 245	Osaki 099, 244, 245, 291	Schneider 064, 245, 398	Vidtech 046, 063, 205
JBL 081	Oso	Scimitsu	Vision
JCB 027	Osume 099	Scotch	Waltham
IVC 080, 063, 398, 680			
	Otto Versand 064, 037, 063,	Scott 263, 046, 205, 206, 207	Wards 081, 192, 205, 046,
KEC 207	244, 347, 581	Sears 181, 083, 183, 074, 081,	048, 057, 083, 206
KTV 207, 244, 057, 066	Palladium 397, 445	198, 205, 206	Watson347.064
Kaisul 245, 244, 036, 243, 309	Panama 244, 291	Seleco 233	Watt Radio
Kamp 243	Panasonic 078, 277, 677	Semivox	Wega 063
Kapsch	Pathe Cinema 347, 243	Semp	White Westinghouse 347,
Kawasho243	Pausa	Sentra	
Kendo			
	Penney 074, 087, 057, 048,	Sharp , 120, 192, 063, 066	Yamaha 046. 057
Kenwood	Penney 074, 087, 057, 048,		Yamaha
Kenwood	Penney 074, 087, 057, 048, 205, 078, 066, 046,	Shogun	Yoko 244, 064, 291, 458
Kingsley	Penney 074, 087, 057, 048, 205, 078, 066, 046, 083, 183	Shogun	Yoko 244, 064, 291, 458 Zanussi
	Penney 074, 087, 057, 048, 205, 078, 066, 046,	Shogun	Yoko 244, 064, 291, 458

Dismantling Instrutions

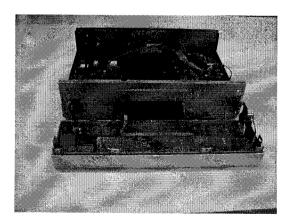
Mechanical Instructions

DISMANTLING INSTRUCTIONS See exploded view for item numbers Cover 151 mounting ⇒ Remove 9 screws 171→174 at both sides 175→179 at the rearside ⇒ Lift the cover at the rearside to remove Front assy Switched Operating Power supply 1002 Progressive Scan board 1007 **DVDR LOADER 81** Analog board 1003 ⇒ open the tray and remove the (Only for DVDR1000/171) ⇒ Remove the connections tray front 65 ⇒ Remove the connections ⇒ Remove screws 204 → 205 ⇒ release snaps of 3 spacers ⇒ remove 4 screws 75→ 78 ⇒ remove 1 screw(206) ⇒ Remove 4 screws (192 → 194) (board → frame) ⇒ demount the board (board → frame) (front assy → frame 181) (air filter 191 → loader 81) ⇒ Remove screw 268 > remove screws (cinches → ⇒ remove screw 72 ⇒ Remove screw 196 (mains inlet → backplate) backplate) (flap motor assy → frame 181) (air filter inlet 198 → frame 181) ⇒ release the snaps of 4 spacers DVIO board 1005 ⇒ Release the snaps of 2 spacers \Rightarrow remove the feet (251 \rightarrow 254) ⇒ Remove air filter assy (board → frame) 183 and 184 (board → frame) and the bottomplate (231) ⇒ Remove 2 screws 217 and 218 ⇒ Open the tray and remove ⇒ Demount the board demount the board (DVIO board → frame 181) the tray front 65 ⇒ unlock the front from the ⇒ Remove 4 screws frame by releasing ⇒ Release the snaps of 2 spacers 200 → 203 (loader 81→frame 181 successively 6 snaps (DVIO board → Digital board) (1 on the left, 2 in the middle. ⇒ Demount the DVDR loader ⇒ demount carefully the board. 1 on the right and 2 in the (board to board connection to bottom of the frame. The the Digital board) snaps in the bottom can be released inside the set via the holes in the bottom. Digital board 1001 ⇒ Remove the connections

⇒ Remove 4 screws 207 → 210

⇒ demount the board.

(Digital board → frame 181)



Display board 1004

(board → front)

demount the board

⇒ Remove 6 screws 33 → 38

IR/STBY Board 1004

⇒ remove screw 30

⇒ demount the board

(board → front)

FRONT AV Board1004

(board → front)

⇒ demount the board

⇒ remove screws 31+32

FRONT DV Board 1006

⇒ Remove screw 17

(board → front)

⇒ demount the board

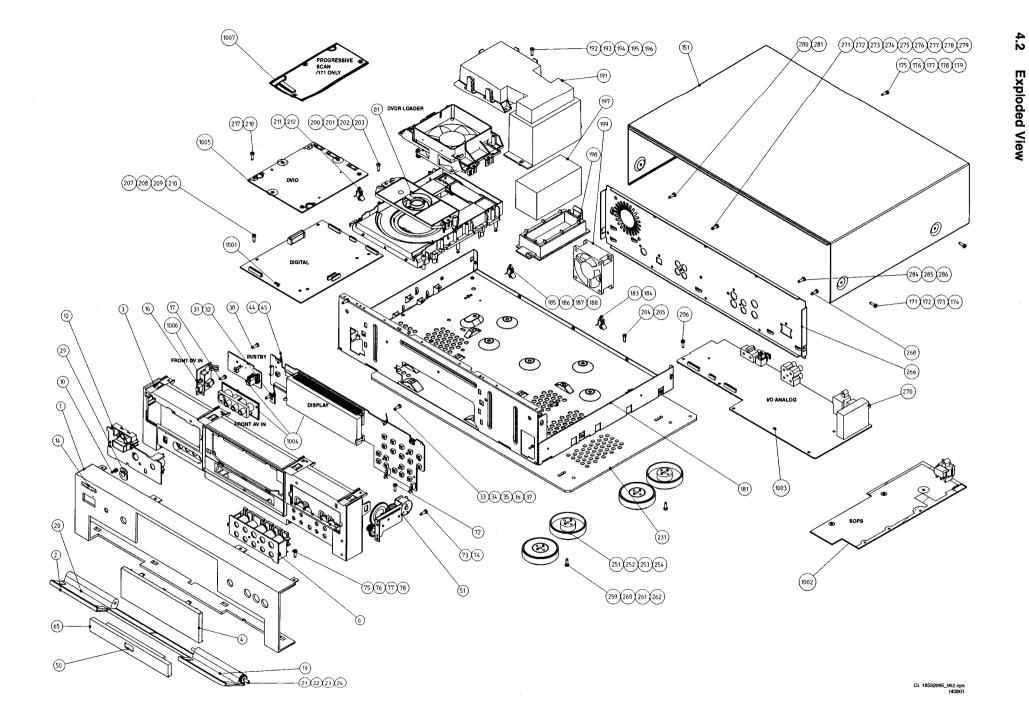
Manually removal of tray front 65

In case the loader is defective and cannot be opened electrically, you can open the tray after demounting the loader as follows:

- ⇒ Remove the connections to the loader
- ⇒ Remove 4 screws (192 → 194)
- (air filter 191 → loader 81)
- ⇒ Remove screw 196
- (air filter inlet 198 → frame 181)
- ⇒ Remove air filter assy
- ⇒ Remove 4 screws
- 200 → 203 (loader 81→ frame 181)

 ⇒ Lift the loader a the rear side. The tri
- ⇒ Lift the loader a the rear side. The tray front jumps off from the loader.
- ⇒ demount the loader
- Push the white pin of the slider at the bottom side of the loader in the direction indicated by the arrow. Open the unlocked tray.

CL 16532095_061.eps 140801



Service Hints 4.3

4.3.1 **DVDR Module VAE8010/01**

This module, item 81 in exploded view, must be exchanged completely in case of failure. A new unit can be ordered with codenumber 9305 025 81001.

4.3.2 Service Positions

Front

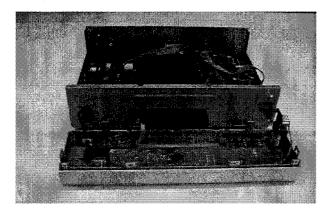


Figure 4-1

DVIO Board

To put the DVIO board in a service position, an extender board must be used. This extender board can be ordered with codenumber 3104 128 07770.

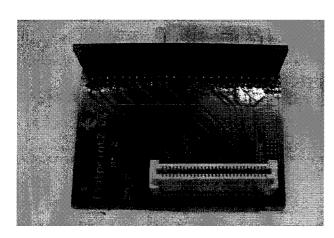


Figure 4-2

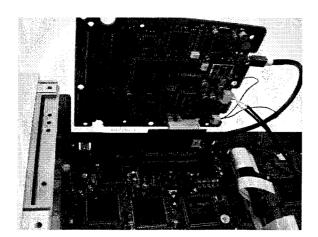


Figure 4-3

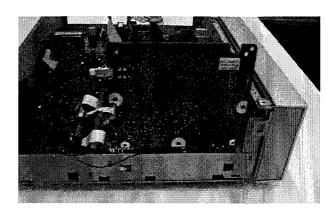


Figure 4-4

Digital Board

After demounting of DVIO board, the top side of the digital board is in reach. To reach the bottom side of the digital board, the DVDR module must be demounted together with the digital board. Connected to each other, the assembly can be set in a service position. In this position, the bottom side of the digital board and the servo board are in reach to be serviced.

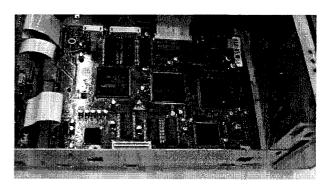


Figure 4-5

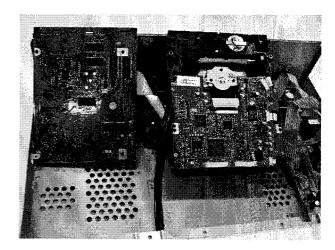


Figure 4-6

Analog Board

To put the analog board in service position, demount the assembly of analog board and backplate as follows:

- 1. Remove 3 screws from the backplate to 1 the frame
- Remove the screw from the backplate b the mains inlet of the power supply
- Remove the screw of the analog board the frame

GB 36

4. Release the snaps of the 4 spacers of the analog board to the frame.

Turn the assembly of the backplate and the analog board against the loader.

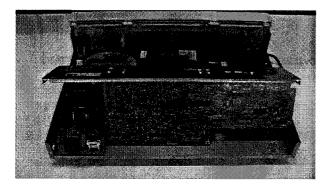


Figure 4-7

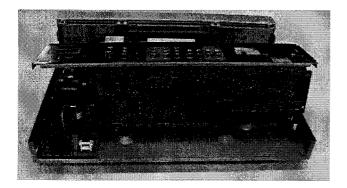


Figure 4-8

Diagnostic Software and Faultfinding Trees 5.

Due to the complexity of the DVD recorder, the time to find a defect in the recorder can become long. To reduce this time, the recorder has been equipped with Diagnostic and Service software (DS). The DS offers functionality to diagnose the DVDR hardware and tests the following:

- Interconnections between components
- Accessibility of components
- Functionality of the audio and video paths

This functionality can be accessed via several interfaces:

- 1. End user/Dealer script interface
- Player script interface
- Menu and command interface

5.1 **End User/Dealer Script Interface**

5.1.1 Description

The End user/Dealer script interface gives a diagnosis on a stand alone DVD recorder; no other equipment is needed. During this mode, a number of hardware tests (nuclei) are automatically executed to check if the recorder is faulty. The diagnosis is simply a "fail" or "pass" message. If the message "FAIL" appears on the display, there is apparently a failure in the recorder. If the message "PASS" appears, the nuclei in this mode have been executed successfully. There can be still a failure in the recorder because the nuclei in this mode don't cover the complete functionality of the recorder.

Contents

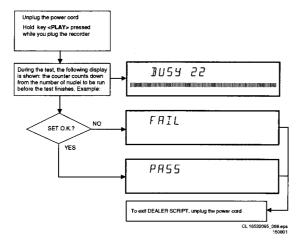


Figure 5-1

The End use/Dealer script executes all diagnostic nuclei that do not need any user interaction and are meaningful on a standalone DVD recorder. The nuclei called in the End user/ Dealer script are the following:

22	HostdSdramWrR	check of all memory locations of the 4MB SDRAMS
21	HostdDramWrR	check of all the DRAMS
20	Hostdl2cNvram	check of the data line and the clock line of the I2C bus between the host decoder and NVRAM
19	SAA711XI2c	checks the interface between the host I2C controller and the Video Input Processor SAA7118
18	VideoEncl2c	checks the interface between the host I2C controller and the Video Encoder SAA6750

	T	T
17	AudioEncl2c	checks the I2C connection be- tween the host decoder and the audio encoder
16	AudioEncAccess	this nucleus tests the HIO8 inter- face lines between the host de- coder and the audio encoder
15	AudioEncS- ramAccess	check of the access of the SRAM by the audio encoder (address and data lines)
14	AudioEncS- ramWrR	tests the SRAM connected to the audio encoder
13	AudioEncInter- rupt	tests the interrupt line between the host decoder and the audio encoder
12	VsmAccess	checks the data and address bus and the interrupt register of the VSM
11	VsmInterrupt	checks both interrupt lines be- tween the VSM and the host de- coder
10	VsmSdramWrR	tests the entire SDRAM of the VSM
9	Clock11_289MHz	switches the A_CLK of the micro clock to 11.2896 MHz
8	Clock12_288MHz	switches the A_CLK of the micro clock to 12.288 MHz
7	BeS2Bengine	checks the S2B interface with the Basic Engine by sending an echo command
6	DisplayEcho	checks the interface between the host processor and the slave processor on the display board
5	AnalogueEcho	checks the interface between the host processor and the micro- processor on the analogue board
4	AnalogueNvram	checks the NVRAM on the analogue board
3	AnalogueTuner	checks whether the tuner on the analogue board is accessible
2	LoopAudioUser- Dealer	tests the components on the audio signal path Host decoder Analogue board Audio encoder VSM
1	LoopVideoUser- Dealer	tests the components on the vid- eo signal path VIP VSM Host decoder

5.2 **Player Script Interface**

5.2.1 Description

The Player script will give the opportunity to perform a test that will determine which of the DVD record∌r's modules are faulty, to read the error log and to perform an endurance loop test. To successfully perform the tests, the DVD recorder must be connected to a TV set.

To be able to check results of certain nuclei, the player script expects some interaction of the user (i.e. to approve a test picture or a test sound). Some nuclei (e.g. Luclei that test functionality of the DVDR module) require \$\text{at a DVD+RW}\$ disc is inserted.

Only tests within the scope of the diagnostic software will be executed hence only faults within this scopecan be detected.

5.2.2 Structure of the Player Script

The player script consists of a set of nuclei testing the hardware modules in the DVD recorder: the Display PWB, the Digital PWB, the Analogue In/Out PWB and the DVDR module.

DVDR1000 /0x1 /691

Nuclei run by the player test need some user interaction; in the next table this interaction is described. The player test is done in two phases:

- Interactive tests: this part of the player test depends strongly on user interaction and input to determine nucleus results and to progress through the full test. Reading the error log information can be useful to determine any errors that occurred recently during normal operation of the DVD player.
- The loop test will perform the same nuclei as the dealer test, but it will loop through the list of nuclei indefinitely.

STEP 1	Press OPEN/CLOSE and STOP at the same time and POWER ON the recorder to start the playerscript	NUCLEU
2	The local display shows FPSEGMENTS. Press PLAY to start the test.	5
-	First the starburst pattern is lit, then the horizontal segments are lit, followed by the vertical	3
	segments and the last test is light all segments test. After each of the 4 tests the user has to	
	confirm that the correct pattern was lit.	
	Press PLAY to confirm that the correct pattern was lit (four times if the FPSEGMENTS test	
	was successful).	
	Press RECORD to indicate that the correct pattern was not successfully lit. Press STOP to skip this nucleus.	
3	The local display shows FPLABELS. Press PLAY to start the test.	5
ı ı	Press PLAY to confirm that all labels are lit.	3
	Press RECORD to indicate that not all labels are lit.	
	Press STOP to skip this nucleus.	
4	The local display shows FPLIGHT ALL. Press PLAY to start the test.	5
	Press PLAY to confirm that everything was lit.	
	Press RECORD to indicate that not all patterns are lit.	
5	Press STOP to skip this nucleus. The local display shows FPLED. Press PLAY to start the test.	-
· ·	Press PLAY to confirm that the led is lit.	5
	Press RECORD to indicate that the led is not lit.	
	Press STOP to skip this nucleus.	
6	The local display shows FPFLAP OPEN. Press PLAY to start the test.	5
	Press PLAY to confirm that the flap has opened.	
	Press RECORD to indicate that the flap did not open.	
	Press STOP to skip this nucleus.	
7	The local display shows FPKEYBOARD. Press PLAY to start the test.	5
	Attention all keys have to be pressed to get a positive result!	
	Press PLAY for more than one second to confirm that all the keys were pressed and shown on the local display. If not all the keys were pressed, a FAIL message will appear on the	
	local display.	
	Press RECORD for more than one second to indicate that not all keys were pressed and	
	shown on the local display.	
	Press STOP for more than one second to skip this nucleus.	
8	The local display shows FPREMOTE CONTROL. Press PLAY to start the test.	5
	Press PLAY to confirm that a key on the remote control was pressed and shown on the	
	local display. Only one key has to be pressed to get a successful result.	
- 1	Press RECORD to indicate that the key on the remote control was pressed but not shown on the local display.	
i	Press STOP to skip this nucleus.	
9	The local display shows FPDIMMER. Press PLAY to start the test.	5
·	Press PLAY to confirm that the text on the local display was dimmed.	J
	Press RECORD to indicate that the text on the local display was not dimmed.	
	Press STOP to skip this nucleus.	
10	The local display shows FPBEEPER. Press PLAY to start the test.	5
i	Press PLAY to confirm that the beeper on the front panel sounded.	
l	Press RECORD to indicate that the beeper on the front panel did not sound.	
11	Press STOP to skip this nucleus. The local display shows FPFLAP CLOSE. Press PLAY to start the test.	·
11	Press STOP to skip this nucleus.	5
12	The local display shows ROUTE VIDEO. Press PLAY to start the test.	7
'-	Press STOP to skip this nucleus.	,
13	The local display shows ROUTE AUDIO. Press PLAY to start the test.	7
	Press STOP to skip this nucleus.	•
14	The local display shows COLOUR-BAR ON. Press PLAY to start the test.	1:
	Press STOP to skip this nucleus.	
15	The local display shows PINK NOISE ON. Press PLAY to start the test.	1
	Press STOP to skip this nucleus.	
16	The local display shows PINK NOISE OFF. Press PLAY to start the test.	1
	Press STOP to skip this nucleus. The legal display shows SIME ON Press BLAY to short the test	
17	The local display shows SINE ON. Press PLAY to start the test. Press STOP to stop the sine.	1
1	Press STOP to skip this nucleus.	
18	The local display shows COLOUR-BAR OFF. Press PLAY to start the test.	1:
	Press STOP to skip this nucleus.	14
19	The local display shows BERESET. Press PLAY to start the test.	60
	Press STOP to skip this nucleus.	0.
20	The local display shows BETRAY OPEN. Press PLAY to start the test.	6
	Press STOP to skip this nucleus.	
21	The local display shows BETRAY CLOSE. Press PLAY to start the test.	61
	Press STOP to skip this nucleus.	
22	The local display shows BEWRITE READ . Press PLAY to start the test.	61
- 22	Press STOP to skip this nucleus.	
23	The local display shows BETRAY OPEN. Press PLAY to start the test. Press STOP to skip this nucleus.	61
24	The local display shows BETRAY CLOSE. Press PLAY to start the test.	
24	Press STOP to skip this nucleus.	6
25	The local display shows READ ERRORLOG. Press PLAY to start the test.	63
20	Press STOP to skip this nucleus.	63
	If the player test succeeded, the user/dealer script will start in an endless loop,	
- 1		
	If the player test failed, the local display will display FAIL and the error code	

5.

In case of failure, the display shows " FAIL 00000 ". The description of the shown error code can be retrieved in the survey of Nuclei Error Codes (paragraph 5.4). Once an error occurs, it is not possible to continue the player script. Unplug the set and restart the player script. By pressing the STOP key, it is possible to jump over the failure and to continue the player script.

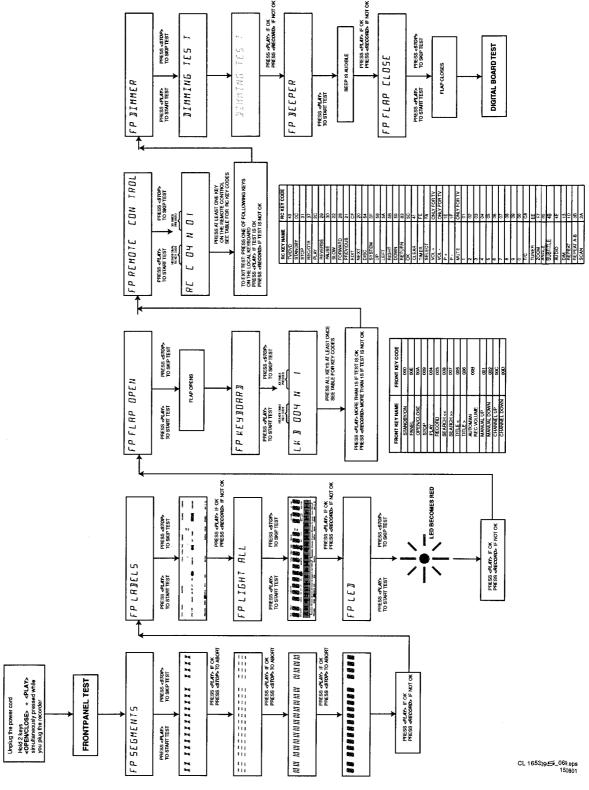


Figure 5-2

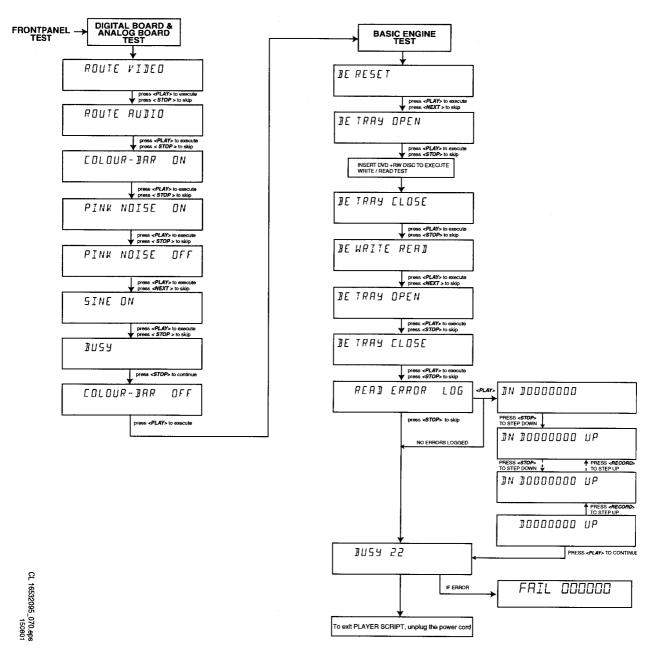


Figure 5-3

5.2.3 ErrorLog

Explanation:

The application errors will be logged in the NVRAM. The maximum number of error bytes that will be visible is 19. The last reported error is shown as DN D0000000, the oldest visible error as D0000000 UP and the errors in between as DN D0000000 UP. DN stands for DOWN, UP stands for UPWARDS. The shown error codes are identical to the Nuclei Error Codes (paragraph 5.4).

5.2.4 Trade Mode

TRADE MODE

When the recorder is in Trade Mode, the recorder cannot be controlled by means of the front key buttons, but only by means of the remote control.

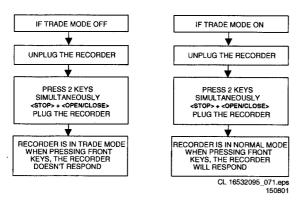


Figure 5-4

5.3 **Menu and Command Mode Interface**

5.3.1 **Nuclei Numeration**

Each nucleus has a unique number of four digits. This number is the input of the command mode.

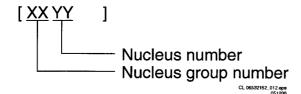


Figure 5-5

The following groups are defined:

Group number	Group name
0	Basic / Scripts
1	Host decoder (Sti5505 and memory)
2	Audio / video encoder (DVDR only)
3	VSM (DVDR only)
4	NVRAM
5	Front Panel
6	Basic Engine
7	Analogue board (DVDR only)
8	DVIO (DVDR only)
9	Loop nuclei (DVDR only)
10	Library sub nuclei (I2C nuclei)
11	User interface
12	Furore (SACD only)
13	DAC (SACD only)
14	Miscellaneous

5.3.2 Error Handling

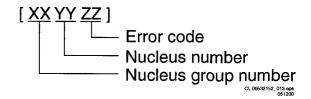


Figure 5-6

The nucleus group numbers and nucleus numbers are the same as above.

Command Mode Interface 5.3.3

Set-Up Physical Interface Components

Hardware required:

- Service PC
- one free COM port on the Service PC

special cable to connect DVD recorder to Service PC The service PC must have a terminal emulation program (e.g. OS2 WarpTerminal or Procomm) installed and must have a free COM port (e.g. COM1). Activate the terminal emulation program and check that the port settings for the free COM port are: 19200 bps, 8 data bits, no parity, 1 stop bit and no flow control. The free COM portmust be connected via a special cable to the RS232 port of the DVD recorder. This special cable will also connect the test pin, which is available on the connector, to ground (i.e. activate test pin). Code number of PC interface cable: 3122 785 90017

Activation

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

DVD Video Recorder Diagnostic Software version 48 Basic SDRAM Data bus test passed Basic SDRAM Address bus test passed Basic SDRAM Device test passed (M) enu, (C) ommand or (S) 2B-interface? DD:> [M] : @ C 🚽

Figure 5-7

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing C has made a choice for Command Interface, the prompt ("DD>") will appear. The diagnostic software is now ready to receive commands. The commands that can be given are the numbers of the nuclei.

Command Overview

We provide an overview of the nuclei and their numbers. This overview is preliminary and subject to modifications.

Host Decoder [01]

[xx yy] Number	Nuclei
100	Checksum Flash
101	Flash Write Access 1
102	Flash Write Access 2
103	Flash Write Read
104	SdRam Write Read
105	SdRam Write Read Fast
106	Dram Write Read
107	Dram Write Read Fast
108	Hardware Version
109	Mute On
110	Mute Off
115	Pink Noise On
116	Pink Noise Off
117	Sine On
118	Sine Burst 1kHz
119	Sine Burst 12kHz
120	Colour-bar On
121	Colour-bar Off
122	NvramWrR
123	Nvraml2c
130	Boot Version
131	Application Version
132	Diagnostics Version
133	Download Version
134	Write / read I2C message to / from digital board

Audio Video Encoder [02]

[xx yy] Number	Nuclei
200	Video Encoder I2C
202	SAA711x I2C
203	Audio Encoder SRAM Access
204	Audio Encoder Access
205	Audio Encoder SRAM Write Read
206	Audio Encoder Interrupts

[xx yy] Number	Nuclei
207	Audio Encoder I2C
208	SAA7118 select input

VSM [03]

[xx yy] Number	Nuclei
300	Register Access
301	SDRAM Access
302	SDRAM Write Read
303	Interrupt lines
304	VSM Interconnection
305	UART

NVRAM [04]

[xx yy] Number	Nuclei
400	Reset
401	Read
402	Modify
403	UniqueNr Read
404	Read Error Log
407	Reset Error Log
409	Line2 Region-Code Reset
410	UniqueNr Store

Front Panel [05]

[xx yy] Number	Nuclei
500	Echo
501	Version
502	Segment
503	Label
504	Led
505	Keyboard
506	Remote-Control
507	Segment Starburst
508	Segment Vertical
509	Segment Horizontal
514	Beeper
515	Discbar
516	Discbar Dots
517	Vu / Grid
518	Dimmer
519	Blinking
520	Light All Segments
522	Flap Open
523	Flap Close

Basic Engine [06]

[xx yy] Number	Nuclei
600	S2B Pass
601	S2B Echo
602	Version
603	Reset
604	Focus On
605	Focus Off
606	Disc Motor On
607	Disc Motor Off
608	Radial On
609	Radial Off
615	Tray In
616	Tray Out
617	Write Read
618	Write Read Endless Loop
619	Selftest
620	BE Test
621	Laser Test
622	Spindle (Disc) Motor Test
623	Focus Test
624	Sledge Motor Test
625	Sledge Motor Slow
626	Tilt
627	EEPROM Read
628	EEPROM Write
629	Optimise Jitter
630	Radial ATLS Calibration
631	Get Statistics Information
632	Reset Statistics Information
633	BE Read Error Log
634	BE Reset Error Log
638	Get Self Test Result
639	Radial Initialisation

Analogue Board [07]

[xx yy] Number	Nuclei
700	Echo
703	Boot Version
704	Hardware Version
705	Clock Adjust
706	Tuner
707	Frequency Download
708	Data Slicer
709	Sound Processor
710	AV Selector
711	Nvram
712	Route Video
713	Route Audio
714	Validate CVBS
715	Set Slash Version
716	Application Version
717	Diagnostics Version
718	Download Version
719	Initiate Output Of Clock Reference
720	Adjust Clock reference
721	Adjust Bargraph Level
723	Revirginize Recorder
724	Flash Checksum
726	Tuner frequency selection

[xx yy] Numbe	er Nuclei
727	Set virgin bit
728	Clear Virgin Bit
729	Write / read I2C message to / from analogue board
730	Store external presets

DVIO [08]

[xx yy] Number	Nuclei
800	Check DVIO board presence
801	Reset DVIO
802	DVIO Access
803	Get DVIO error codes
804	Get DVIO module Ids

Loop Nuclei [09]

[xx yy] Number	Nuclei
900	Digital Audio Loop
901	Audio User Dealer Loop
902	Digital Video Loop
903	Digital Video VBI Loop
904	System Video Loop
905	System Video VBI Loop
906	Video User Dealer Loop
907	Video VBI User Dealer Loop
908	System Audio Loop SCART
909	System Audio Loop CINCH
910	Digital DVIO Video Loop

Miscellaneous [14]

[xx yy] Number	Nuclei
1400	Clock 11.289 MHz
1401	Clock 12.288 MHz
1412	Progressive Scan I2C
1413	Progressive Scan test image on
1414	Progressive Scan test image off

Scripts [00]

	[xx yy] Number	Nuclei
	1	UserDealer Script
ĺ	2	Player Script

5.3.4 Menu Mode Interface

Activation

Plug the recorder to the mains and the following text will appear on the screen of the terminal (program):

	ic SDRAM Address bus test ic SDRAM Device test pass		
Das	ic sham bevice test pass	sea	
(M)	enu, (C) ommand or (S) 2	B-interface?	[M] : 0 M
Madi	n Menu		
Mal.	n Menu		
1.	Digital Board	->	
2.	Analogue Board	->	
3.	Front Panel	->	
4.	Basic Engine	->	
5.	DVIO	->	
6.	Progressive Scan Board	->	
7.		->	
8.	Log	->	
9.	Scripts	~>	

Figure 5-8

The first line indicates that the Diagnostic software has been activated and contains the version number. The next lines are the successful result of the SDRAM interconnection test and the basic SDRAM test. The last line allows the user to choose between the three possible interface forms. If pressing M has made a choice for Menu Interface, the Main Menu will appear.

Menu Structure

The following menu structure is given after starting up the DVD recorder in menu mode. The symbol → indicates that the current menu choice will invoke the display of a submenu.

Main Menu

- 1. Digital Board →
- 2. Analogue Board →
- 3. Front Panel →
- 4. Basic Engine →
- 5. DVIO →
- 6. Progressive Scan Board →
- 7. Loop Tests →
- 8. Log →
- 9. Scripts →

Digital Board Menu

- 1. Host Decoder →
- 2. VSM →
- 3. AVENC →
- 4. NVRAM →

Host Decoder Menu

- 1. Flash Checksum
- 2. Flash1 Write Access
- 3. Flash2 Write Access
- 4. Flash Write/Read
- 5. Host SDRAM Write/Read
- 6. Host SDRAM Fast Write/Read
- 7. Host DRAM Write/Read
- 8. Host DRAM Fast Write/Read
- 9. I2C NVRAM
- 10. NVRAM Write/Read
- 11. Engine S2B Echo
- 12. Versions →
- 13. Audio Mute →
- 14. Colourbar →
- 15. Pink Noise →
- 16. Sine Generate →

Digital Board Versions Menu

- 1. Hardware Version
- 2. Bootcode version
- 3. Applications Version
- 4. Diagnostics Version

5. Download Version

Audio Mute Menu

- 1. Audio Mute On
- 2. Audio Mute Off

Colourbar Menu

- 1. Colourbar On
- 2. Colourbar Off

Pink Noise Menu

- 1. Pink Noise On
- 2. Pink Noise Off

Sine Generate Menu

- 1. Sine On
- 2. Sine Burst 1kHz
- 3. Sine Burst 12kHz

VSM Menu

- 1. Register Access
- 2. SDRAM Access
- 3. VSM SDRAM Write/Read
- 4. Interrupt Lines
- 5. VSM Interconnection
- 6. UART

AVENC Menu

- 1. Video Encoder →
- 2. Audio Encoder →
- 3. Video Input Processors →

Video Encoder Menu

1. I2C Access

Audio Encoder Menu

- 1, I2C Access
- 2. Interrupt Line
- 3. Encoder Register Access
- 4. SRAM Write/Read
- 5. SRAM Access

Video Input Processors Menu

1. SAA711X I2C Access

NVRAM Menu

- 1. Read Error Log
- 2. Reset Error Log
- 3. Read DVIO Unique ID

Analogue Board Menu

- 1. Echo
- 2. Show Guide Channels
- 3. Video Routing
- 4. Audio Routing
- 5. Flash Checksum
- 6. Versions →
- 7. Components →
- Re-virginize Recorder →

Analogue Board Versions Menu

- 1. Hardware Version
- 2. Bootcode version
- 3. Application version
- 4. Diagnostics version
- 5. Download version

Analogue Components Menu

- 1. Tuner
- 2. Data Slicer
- 3. Sound Processor
- 4. AV Selector

5. NVRAM

Analogue Board Re-virginize Menu

- 1. Re-virginize Recorder
- 2. Set Virgin-bit
- 3. Clear Virgin-bit
- 4. Store external presets

Front Panel Menu

- 1. Echo
- 2. Version
- 3. Flap Control →
- 4. Segment Test →
- 5. Light Labels
- 6. Led test
- 7. Keyboard test
- 8. Remote Control
- 9. Beep
- 10. Disc Bar
- 11. Disc Bar Dots
- 12. Vu Grid
- 13. Dimmer
- 14. Blink
- 15. Light All Segments

Flap Control Menu

- 1. Open Flap
- 2. Close Flap

Segment Test Menu

- 1. Starburst
- 2. Light Horizontal Segments
- 3. Light Vertical Segments
- 4. Light All Segments

Basic Engine Menu

- 1. Reset
- 2. S2B Pass
- 3. S2B Echo
- 4. Version
- 5. Self Test
- 6. Get Self Test Result
- 7. Basic Engine Test
- 8. Laser Test
- 9. Focus Test
- 10. Tilt Test
- 11. Optimise Jitter
- 12. Statistics Info
- 13. Log →
- 14. Spindle Motor →
- 15. Radial →
- 16. Sledge →
- 17. Tray →

Basic Engine Error Log

- 1. Read Error Log
- 2. Reset Error Log

Basic Engine Spindle Motor Menu

- 1. Spindle Motor On
- 2. Spindle Motor Off
- 3. Spindle Motor Test

Basic Engine Radial Menu

- 1. Radial On
- 2. Radial Off
- 3. Radial Initialisation
- 4. Radial ATLS Calibration

Basic Engine Sledge Menu

- 1. Sledge test
- 2. Sledge test slow

Basic Engine Tray Menu

- 1. Tray In
- 2. Tray Out

DVIO Menu

- 1. Check Presence
- 2. Reset
- 3. Access
- 4. Error Codes
- 5. Module Identifiers

Progressive Scan Board Menu

- 1. I2C Access
- 2. Test Image On
- 3. Test Image Off

Loop Tests Menu

- 1. Digital Board Loops →
- 2. User/Dealer Loops →
- 3. System Loops →
- 4. Basic Engine Loops →

Digital Board Loops Menu

- 1. Digital Audio Loop
- 2. Digital Video Loop
- 3. Digital Video Loop VBI

User/Dealer Loops Menu

- 1. User/Dealer Audio Loop
- 2. User/Dealer Video Loop
- 3. User/Dealer Video Loop VBI

System Loops Menu

- 1. System Video Loop
- 2. System Video Loop VBI
- 3. System Audio Loop SCART
- 4. System Audio Loop SCART

Basic Engine Loops Menu

- 1. Basic Engine write read
- 2. Basic Engine write read endless loop

Log Menu

- 1. Read Error Log
- Reset Error Log

Script Menu

- 1. User/Dealer Script
- 2. Player Script

5.4 **Nuclei Error Codes**

In the following table the error codes will be described.

Error Nr	Error String
10000	"Checksum is OK"
10001	"segment name Checksum doesn't match" or "segment name segment not found!"
10100	88
10101	"FLASH 1 Write access test failed"
10200	DII
10201	"FLASH 2 Write access test faile("
10300	ни
10301	"FLASH write test failed"
10302	"FLASH write command failed"
10303	"FLASH write test done max. nunber of times"
10400	nii .
10401	"HostDec SDRAM Memory data Dus test goes wrong."

ErrorNr	Error String
10402	" HostDec SDRAM Memory address bus test goes
	wrong."
10403	" HostDec SDRAM Physical memory device tes
10500	goes wrong."
10500	III III ADA ADDAMA MARKATANIA ANALASA
10501	" HostDec SDRAM Memory data bus test goes wrong."
10502	" HostDec SDRAM Memory address bus test goes
10302	wrong."
10503	" HostDec SDRAM Physical memory device test
	goes wrong."
10600	ш
10601	"HostDec DRAM Memory data bus test goes
	wrong."
10602	"HostDec DRAM Memory address bus test goes
	wrong."
10603	"HostDec DRAM Physical memory device test
10700	goes wrong."
10700	
10701	"HostDec DRAM Memory data bus test goes wrong."
10702	"HostDec DRAM Memory address bus test goes
10702	wrong."
10703	"HostDec DRAM Physical memory device test
	goes wrong."
10800	"Host Decoder version(cut) number: version
	number" "Digital hardware version"
10801	"Can not find version in FLASH."
10900	MII
10901	"Error muting audio"
11000	ин
11001	"Error demuting audio"
11500	ин
11501	"Init of I2C failed"
11502	"The selection of the clock source failed"
11504	"The demute of the audio failed"
11600	
11601	"Init of I2C failed"
11602	"The mute of the audio failed"
11700	
11701	"Init of I2C failed"
11702	"The muting of the audio failed"
11703	"The demute of the audio failed"
11704	"The selection of the clock source failed"
11707	"Setup of Front panel failed"
11708	"Sine on Front panel keyboard failed"
11800	
11801	"Init of I2C failed"
11802	"The muting of the audio failed"
11803	"The demute of the audio failed"
11804	"The selection of the clock source failed"
11805	"Error cannot start VSM audio in port"
11900	
11901	"Init of I2C failed"
11902	"The muting of the audio failed"
11903	"The demute of the audio failed"
11904	"The selection of the clock source failed"
1905	"Error cannot start VSM audio in port"
2000	AB
2100	
2200	NOO been been been been been been been be
2201	"I2C bus busy before start" "NVRAM access time-out"
	NVHAM 2009S TIME-OUT"

Error N	Error String
12203	"No NVRAM acknowledge"
12204	"NVRAM time-out"
12205	"NVRAM Write/Read back failed"
12300	HII
12301	"I2C bus busy before start"
12302	"NVRAM read access time-out"
12303	"No NVRAM read acknowledge"
12304	"NVRAM read failed"
13000	"Bootcode application version : bootversion"
13000	"Can not find version in FLASH."
13100	"Recorder application version : recorderversion"
13100	"Can not find version in FLASH."
13200	"Diagnostics application version : diagversion"
13200	"Can not find version in FLASH."
13300	E .
13301	"Download application version : downloadversion" "Can not find version in FLASH."
	Carriot find version in FLASH.
20000	
20001	"I2C bus busy before start" "Video Encoder access time-out"
	•
20003	"No acknowledge from Video Encoder" "No data send/received to or from Video Encoder"
20005	"SAA711x VIP can not be initialised"
20201	"I2C bus busy before start"
20202	"SAA711X VIP access time-out"
20203	"No acknowledge from SAA711X VIP"
20204	"No data received from SAA711X VIP"
20300	
20301	"Error audio encoder SRAM access cannot initialise I2C"
20302	"Error audio encoder SRAM access cannot reset DSP through I2C"
20303	"Error audio encoder SRAM access cannot down- load boot"
20304	"Error audio encoder cannot download test code"
20305	"Error audio encoder cannot obtain result of test"
20306	"Error audio encoder SRAM access stuck-at-zero data line "
20307	"Error audio encoder SRAM access stuck-at-one data line "
20308	"Error audio encoder SRAM access stuck-at-one address line "
20309	"Error audio encoder SRAM access address line address line x is connected to data line data line y"
20310	"Error audio encoder SRAM access address lines address line x and address line y are connected "
20311	"Error audio encoder SRAM access data lines data line x and data line y are connected "
20312	"Error audio encoder SRAM access illegal data re- ceived"
20400	ши
20401	"Error audio encoder access cannot initialise I2C"
20402	"Error audio encoder access cannot reset DSP through I2C"
20403	"Error audio encoder accessing ICR register"
20404	"Error audio encoder access stuck-at-zero of data line "
20405	"Error audio encoder access stuck-at-one of data line "
20406	"Audio encoder access data lines data line x and data line y are interconnected "
20500	ня

	Error String
20501	"Error audio encoder SRAM WRR cannot initialise I2C"
20502	"Error audio encoder SRAM WRR cannot rese DSP through I2C"
20503	"Error audio encoder WRR cannot download boot
20504	"Error audio encoder cannot download test code"
20505	"Error audio encoder SRAM WRR cannot obtair
	result of test"
20506	"Error audio encoder WRR SRAM stuck-at-zero data bit "
20507	"Error audio encoder WRR SRAM stuck-at-one data bit "
20508	"Error audio encoder WRR SRAM data lines data line x and data line y are connected"
20509	"Error audio encoder WRR SRAM illegal data re ceived"
20600	ми
20601	"Error audio encoder interrupt cannot initialise
20602	"Error audio encoder interrupt cannot reset DSF through I2C"
20603	"Error audio encoder cannot download test code"
20604	"Error audio encoder interrupt cannot download
	boot"
20605	"Error occurred accessing VSM"
20606	"Audio encoder interrupt not received"
20700	1111
20701	"Error audio encoder I2C cannot reset DSF through I2C"
20702	"Error audio encoder cannot download boot"
20703	"Error audio encoder cannot download TEST code"
20704	"Error audio encoder I2C bus busy"
20704	"Error audio encoder I2C cannot write slave ad-
20706	dress" "Error audio encoder I2C no acknowledge re- ceived"
20707	"Error audio encoder I2C cannot send/receive data"
20708	"Error audio encoder received data through I2C
	was invalid"
20800	
20801	"I2C access failed."
20802	"SAA7118 VIP can not be initialised."
20803	"Invalid input"
30000	н
30001	"VSM SDRAM Bank1 Memory databus test goes wrong."
30002	"VSM SDRAM Bank1 Memory addressbus test goes wrong."
30003	"VSM SDRAM Bank1 Physical memory device test goes wrong."
30004	" VSM SDRAM Bank2 Memory databus test goes wrong."
30005	" VSM SDRAM Bank2 Memory addressbus test goes wrong."
	" VSM SDRAM Bank2 Physical memory device
30006	test goes wrong."
30006	
	"VSM SDRAM Bank1 VSM interrupt register A has a -stuck at- error for value:" "VSM SDRAM Bank2 VSM interrupt register A has
30007	"VSM SDRAM Bank1 VSM interrupt register A has a -stuck at- error for value:" "VSM SDRAM Bank2 VSM interrupt register A has a -stuck at- error for value:"
30007	"VSM SDRAM Bank1 VSM interrupt register A has a -stuck at- error for value:" "VSM SDRAM Bank2 VSM interrupt register A has

goes wrong." 30103 "VSM SDRAM Bank1 Physical memory device test goes wrong." 30104 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30105 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30106 "VSM SDRAM Bank2 Physical memory device test goes wrong." 30200 "" 30201 "VSM SDRAM Bank1 Memory addressbus test goes wrong." 30202 "VSM SDRAM Bank1 Memory addressbus test goes wrong." 30203 "VSM SDRAM Bank1 Physical memory device test goes wrong." 30204 "VSM SDRAM Bank1 Physical memory device test goes wrong." 30205 "VSM SDRAM Bank2 Memory databus test goes wrong." 30206 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30300 "" 30301 "VSM SDRAM Bank2 Physical memory device test goes wrong." 30302 "VSM SDRAM Bank2 Physical memory device test goes wrong." 30303 "Interrupt register A has a -stuck at- error for value:" 30303 "Interrupt A wasn't raised." 30304 "Interrupt B wasn't raised." 30305 "Interrupts A and B were raised.' 30400 "VSM SDRAM Bank1 Memory addressbus test goes wrong." 30401 "VSM SDRAM Bank1 Memory addressbus test goes wrong." 30402 "VSM SDRAM Bank1 Physical memory device test goes wrong." 30403 "VSM SDRAM Bank1 Physical rnemory device test goes wrong." 30404 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30405 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30406 "VSM SDRAM Bank2 Physical rnemory device test goes wrong." 30500 "" 30500 "" 30600 "" 30700 "" 30700 "" 30800 "" 30900 "" 3		
goes wrong." 30103 "VSM SDRAM Bank1 Physical memory device test goes wrong." 30104 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30105 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30106 "VSM SDRAM Bank2 Physical memory device test goes wrong." 30200 "" 30201 "VSM SDRAM Bank1 Memory addressbus test goes wrong." 30202 "VSM SDRAM Bank1 Memory addressbus test goes wrong." 30203 "VSM SDRAM Bank1 Physical memory device test goes wrong." 30204 "VSM SDRAM Bank1 Physical memory device test goes wrong." 30205 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30206 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30300 "" 30301 "VSM SDRAM Bank2 Physical memory device test goes wrong." 30302 "VSM SDRAM Bank2 Physical memory device test goes wrong." 30303 "Interrupt register A has a -stuck at- error for value:" 30303 "Interrupt A wasn't raised." 30304 "Interrupt B wasn't raised." 30305 "Interrupt B wasn't raised." 30306 "" 30401 "VSM SDRAM Bank1 Memory addressbus test goes wrong." 30402 "VSM SDRAM Bank1 Memory addressbus test goes wrong." 30403 "VSM SDRAM Bank1 Physical memory device test goes wrong." 30404 "VSM SDRAM Bank1 Physical rnemory device test goes wrong." 30405 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30406 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30407 "VSM SDRAM Bank2 Physical rnemory device test goes wrong." 30408 "VSM SDRAM Bank2 Physical rnemory device test goes wrong." 30500 "" 30600 "" 30701 "VSM SDRAM Bank2 Physical rnemory device test goes wrong." 30702 "SDRAM Bank2 Physical rnemory device test goes wrong." 30703 "VSM SDRAM Bank2 Physical rnemory device test goes wrong." 30709 "VSM SDRAM Bank2 Physical rnemory device test goes wrong." 30709 "	Error Nr	Error String
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30405 "VSM SDRAM Bank2 Memory addressbus test goes wrong." 30406 "VSM SDRAM Bank2 Physical memory device test goes wrong." 30500 "" 30501 "Communication with the analogue board fails." 30502 "Echo test to analogue board returned wrong string." 40000 "" 40001 "NVRAM Reset; I2C failed" 40100 "NVRAM address = 0xaddress → Byte value = 0xvalue" 40101 "NVRAM Read; I2C failed" 40102 "NVRAM Read; Invalid input" 40200 "" 40201 "NVRAM Modify; I2C failed" 40202 "NVRAM Modify; Invalid input" 40300 "DV Unique ID = id" 40301 "NVRAM Read DV Unique ID; I2⟩ failed" 40400 "\\n rorror log:\\n rerorString \\n \overline{\chi} \overline	30404	" VSM SDRAM Bank2 Memory databus test goes
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"Echo test to analogue board returned wrong string." 40000 "" 40001 "NVRAM Reset; I2C failed" 40100 "NVRAM address = 0xaddress >> Byte value = 0xvalue" 40101 "NVRAM Read; I2C failed" 40102 "NVRAM Read; Invalid input" 40200 "" 40201 "NVRAM Modify; I2C failed" 40202 "NVRAM Modify; Invalid input" 40300 "DV Unique ID = id" 40301 "NVRAM Read DV Unique ID; I2; failed" 40400 "\r\n Error log:\r\n errorString \r\r\overline{\Omega}"	30500	au
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40300 "DV Unique ID = id" 40301 "NVRAM Read DV Unique ID; I2; failed" 40400 "\rangle \text{n} \text{ Frior log:\rangle \text{n} errorString \rangle \rangle \rangle \text{\rangle \text{\rang		
40301 "NVRAM Read DV Unique ID; I2; failed" 40400 "\r\n Error log:\r\n errorString \r\n \o "		
40400 "\r\n Error log:\r\n errorString \r\n\O"		
	40401	"NVRAM error log; I2C failed"
40402 "NVRAM error log is invalid"		
40403 "Front panel failed"		
40700		
40701 "NVRAM error log reset; I2C faile	40/01	INVITAM error log reset; I2C tallet

Error Nr	Error String
40900	"Region code Change counter is reset"
40901	"NVRAM region code reset; I2C failed"
41000	1115
41001	"NVRAM Store DV Unique ID; I2C failed"
41002	"NVRAM Store DV Unique ID; Invalid input"
50000	nu
50007	"Execution of the command on the analogu
	board failed."
50008	"The frontpanel could not be accessed by the ar alogue board."
50009	"The echo from the frontpanel processor was no correct."
50100	" Front panel version: FPversion "
50102	"Execution of the command on the analogu board failed."
50103	"The frontpanel could not be accessed by the an alogue board."
50200	ни
50204	"Execution of the command on the analogu- board failed."
50205	"The frontpanel could not be accessed by the an
	alogue board."
50206	"The frontpanel did not show a starburst."
50207	"The user skipped the FP-which pattern test."
50208	"The user returned an unknown confirmation: confirmation "
50209	"The frontpanel did not show horizontal seg ments."
50210	"The frontpanel did not show vertical segments."
50300	III
50304	"Execution of the command on the analogue board failed."
50305	"The frontpanel could not be accessed by the an alogue board."
50306	"The frontpanel did not light all labels."
50307	"The user skipped the rest of the FP-label test."
50308	"The user returned an unknown confirmation
	confirmation"
50400	
50404	"Execution of the command on the analogue board failed."
50405	"The frontpanel could not be accessed by the an alogue board."
50406	"The LED's could not be turned on."
50407	"The user skipped the rest of the FP-LED test."
	"The user returned an unknown confirmation
	confirmation"
50500	110
50502	"Front panel Keyboard; test failed"
50503	"Front panel Keyboard; test aborted"
50504	"Front panel Keyboard; not all keys were pressed
	"Front panel keyboard I2C connection failed"
	nn
	"Front panel Remote control; test failed"
	"Front panel Remote control; test aborted"
	"Front panel remote control; can not access FP"
	"Front panel remote control; no user input re
	ceived"
00700	
	"Execution of the command on the analogue board failed."
0702	"The frontpanel could not be accessed by the an
	alogue board."

Error Nr	Error String
50704	"The user skipped the FP-starburst test."
50705	"The user returned an unknown confirmation: con-
50800	firmation "
50801	"Execution of the command on the contract
	"Execution of the command on the analogue board failed."
50802	"The frontpanel could not be accessed by the an- alogue board."
50803	"The frontpanel did not show vertical segments."
50804	"The user skipped the FP-vertical segments test."
50805	"The user returned an unknown confirmation: confirmation "
50900	н
50901	"Execution of the command on the analogue board failed."
50902	"The frontpanel could not be accessed by the an- alogue board."
50903	"The frontpanel did not show horizontal segments."
50904	"The user skipped the FP-horizontal segments test."
50905	"The user returned an unknown confirmation: confirmation "
51400	Diff
51401	"Execution of the command on the analogue board failed."
51402	"The frontpanel could not be accessed by the an- alogue board."
51403	"The beeper did not sound."
51404	"The user skipped the FP-Beep test."
51405	"The user returned an unknown confirmation: confirmation"
51500	IIN
51501	"Execution of the command on the analogue board failed."
51502	"The frontpanel could not be accessed by the an- alogue board."
51503	"The discbar did not display properly."
51504	"The user skipped the discbar test."
51505	"The user returned an unknown confirmation: confirmation"
51600	111
51601	"Execution of the command on the analogue board failed."
51602	"The frontpanel could not be accessed by the an- alogue board."
51603	"The discbar dots did not display properly."
51604	"The user skipped the discbar dots test."
51605	"The user returned an unknown confirmation: confirmation"
51700	011
51701	"Execution of the command on the analogue board failed."
51702	"The frontpanel could not be accessed by the an- alogue board."
51703	"The VU grid did not display properly."
51704	"The user skipped the VU gridtest."
51705	"The user returned an unknown confirmation: confirmation"
51800	ин
51801	"Execution of the command on the analogue board failed."
51802	"The frontpanel could not be accessed by the an- alogue board."
51803	"The frontpanel could not be dimmed."

51804	Error String
	"The user skipped the FP-Dim test."
51805	"The user returned an unknown confirmation confirmation"
51900	HIL
51901	"Execution of the command on the analogue board failed."
51902	"The frontpanel could not be accessed by the an- alogue board."
51903	"The frontpanel did not show segments blinking."
51904	"The user skipped the FP-blinking test."
51905	"The user returned an unknown confirmation
	confirmation"
52000	
52001	"Execution of the command on the analogue board failed."
52002	"The frontpanel could not be accessed by the an- alogue board."
52003	"The frontpanel did not show all segments lit."
52004	"The user skipped the FP-light all segments test."
52005	"The user returned an unknown confirmation
-	confirmation"
52200	пп
52201	"Communication with Analogue Board fails."
52202	"Frontpanel can not be accessed by the Analogue
	Board."
52300	пя
52301	"Communication with Analogue Board fails."
52302	"Frontpanel can not be accessed by the Analogue
	Board."
60000	RU
60100	БИ
60101	"Basic Engine returned error numbe
50101	Oxerrornumber"
60102	"Parity error from Basic Engine to Serial"
60103	"Communication time-out error"
60104	"Unexpected response from Basic Engine"
60104	"Echo loop could not be closed"
60106	
	"Wrong echo pattern received"
60200	"Version: nr1.nr2.nr3"
60201	"Basic Engine returned error number 0xerrornumber"
60202	"Parity error from Basic Engine to Serial"
60203	"Communication time-out error"
60204	"Unexpected response from Basic Engine"
60205	"Front Panel failed."
60300	MI
60301	"Basic-Engine time-out error"
60400	п
	"Basic Engine returned error number
60401	0xerromumber"
	0xerrornumber"
60402	, -
60402 60403	Oxerromumber" "Parity error from Basic Engine to Serial" "Communication time-out error"
60402 60403 60404	Oxerromumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine"
60402 60403 60404 60405	Oxerromumber" "Parity error from Basic Engine to Serial" "Communication time-out error"
60401 60402 60403 60404 60405 60500 60501	Oxerromumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "Focus loop could not be closed" "" "Basic Engine returned error number
60402 60403 60404 60405 60500 60501	Oxerromumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "Focus loop could not be closed" "" "Basic Engine returned error number Oxerrornumber"
60402 60403 60404 60405 60500 60501	Oxerromumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "Focus loop could not be closed" "" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial"
60402 60403 60404 60405 60500 60501 60502 60503	Oxerromumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "Focus loop could not be closed" "" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial" "Communication time-out error"
60402 60403 60404 60405 60500 60501 60502 60503 60504	Oxerromumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "Focus loop could not be closed" "" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine"
60402 60403 60404 60405 60500 60501 60502 60503	Oxerromumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "Focus loop could not be closed" "" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial" "Communication time-out error"

	Error String
60602	"Parity error from Basic Engine to Serial"
60603	"Communication time-out error"
60604	"Unexpected response from Basic Engine"
60700	nu .
60701	"Basic Engine returned error number
60702	Oxerrornumber" "Parity error from Basic Engine to Serial"
60702	
60704	"Communication time-out error"
60800	"Unexpected response from Basic Engine"
60801	Basic Engine returned error number
00801	"Basic Engine returned error number Oxerrornumber"
60802	"Parity error from Basic Engine to Serial"
60803	"Communication time-out error"
60804	"Unexpected response from Basic Engine"
60805	"Radial loop could not be closed"
60900	III
60901	"Basic Engine returned error number
	Oxerrornumber"
60902	"Parity error from Basic Engine to Serial"
60903	"Communication time-out error"
60904	"Unexpected response from Basic Engine"
61500	ин
61501	"Basic Engine returned error number
	0xerrornumber"
61502	"Parity error from Basic Engine to Serial"
61503	"Communication time-out error"
61504	"Unexpected response from Basic Engine"
61600	ISH
61601	"Basic Engine returned error number
	0xerrornumber"
61602	"Parity error from Basic Engine to Serial"
61603	"Communication time-out error"
61604	"Unexpected response from Basic Engine"
61700	
61701	"BE tray-in command failed"
61702	"BE read-TOC command failed"
61703 61704	"BE VSM interrupt initialisation failed"
	"BE set irq command failed"
61705 61706	"BE no disc or wrong disc inserted"
61706	"BE rec-pause command failed" "BE VSM BE out DMA initialisator failed"
61707	
61708	"BE VSM BE out initialisation failed"
61709	"BE VSM BE out DMA start failed" "BE VSM BE out start failed"
61710	"BE rec command failed"
61712	"BE VSM out underrun error occurred"
61712	
61714	"BE get ira command foiled"
61715	"BE get irq command failed"
61716	"BE VSM DMA out not finished"
61716	"BE stop command after writing belod"
61717	"BE VSM Sector processor initial after writing a filed"
	"BE VSM Sector processor initials ation failed"
61719	"BE VSM sector processor DVIA initialisation failed"
	"BE VSM sector processor DMAstart failed"
	"BE VSM sector processor bm/sstart alled"
	"BE seek command failed"
	"BE VSM sector processor error curred" "BE read timeout occurred"
01/20	"BE stop command after readingfailed"

61726 "BE difference found in data at disc sector Oxdiscsector" 61727 "This nucleus cannot be executed because the Self-Test failed" 61800 "" 61801 "BE izc initialisation failed" 61802 "This nucleus cannot be executed because the Self-Test failed with result: Oxnr1 Oxnr3 "Basic Engine returned error number Oxerrornumber" 61901 "The SelfTest failed with result: Oxnr1 Oxnr3 "Parity error from Basic Engine to Serial" 61903 "Parity error from Basic Engine to Serial" 61904 "Communication time-out error" 61905 "Unexpected response from Basic Engine" 62000 "" 62001 "Self-Test : errorstring1 Laser-Test : errorstring2 SpindleM-Test: errorstring3 SledgeM-Test : errorstring4 Focus-Test : errorstring5" 62101 "Basic Engine returned error number Oxerrornumber" 62102 "Parity error from Basic Engine to Serial" 62103 "Communication time-out error" 62104 "Unexpected response from Basic Engine" 62200 "" 62201 "The BE-self-diagnostic-spindle-motor-test failed oxerrornumber" 62203 "Parity error from Basic Engine to Serial" 62204 "Communication time-out error" 62205 "Unexpected response from Basic Engine" 62301 "The BE-focus-test failed" 62302 "Basic Engine returned error number Oxerrornumber" 62303 "Parity error from Basic Engine to Serial" 62304 "Communication time-out error" 62305 "Unexpected response from Basic Engine" 62307 "Basic Engine returned error number Oxerrornumber" 62400 "" 62401 "The BE-self-diagnostic-sledge-motor-test failed" 62302 "Basic Engine returned error number Oxerrornumber" 62400 "" 62401 "The BE-self-diagnostic-sledge-motor-test failed" 62505 "Unexpected response from Basic Engine" 62600 "" 62701 "Basic Engine returned error number Oxerrornumber" 62702 "Basic Engine returned error number Oxerrornumber" 62703 "Oxerrornumber" 62704 "Communication time-out error" 62705 "Beself-diagnostic-sledge-motor-test failed" 62706 "" 62707 "Basic Engine returned error number Oxerrornumber" 62708 "Besic Engine returned error number Oxerrornumber" 62709 "Besic Engine returned error number Oxerrornumber" 62701 "Besic Engine	Error Nr	Error String
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	62300 62301 62302 62303 62304 62305 62400 62401 62402 62403 62404 62405 62500 62700 62701 62702 62703 62704 62705 62800	"Unexpected response from Basic Engine" "" "The BE-focus-test failed" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "" "The BE-self-diagnostic-sledge-motor-test failed" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "" "BE EEPROM address = address -> Byte value = Oxvalue" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "BE read EEPROM; invalid input" ""
62803 "Communication time-out error"	62300 62301 62302 62303 62304 62305 62400 62401 62402 62403 62404 62405 62500 62700 62701 62702 62703 62704 62705 62800 62801	"Unexpected response from Basic Engine" "" "The BE-focus-test failed" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "" "The BE-self-diagnostic-sledge-motor-test failed" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "" "" "BE EEPROM address = address -> Byte value = Oxvalue" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial" "Communication time-out error" "Parity error from Basic Engine to Serial" "Communication time-out error" "Unexpected response from Basic Engine" "BE read EEPROM; invalid input" "" "Basic Engine returned error number Oxerrornumber"
	62300 62301 62302 62303 62304 62305 62400 62401 62402 62403 62404 62405 62500 62700 62701 62702 62703 62704 62705 62800 62801	"Unexpected response from Basic Engine" "" "The BE-focus-test failed" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial!" "Communication time-out error" "Unexpected response from Basic Engine" "" "The BE-self-diagnostic-sledge-motor-test failed" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial!" "Communication time-out error" "Unexpected response from Basic Engine" "" "" "BE EEPROM address = address -> Byte value = Oxvalue" "Basic Engine returned error number Oxerrornumber" "Parity error from Basic Engine to Serial!" "Communication time-out error" "Unexpected response from Basic Engine to Serial!" "Basic Engine returned error number Oxerrornumber!" "BE read EEPROM; invalid input" "" "Basic Engine returned error number Oxerrornumber!" "Parity error from Basic Engine to Serial!"

Error Nr	Error String
62804	"Unexpected response from Basic Engine"
62805	"BE write EEPROM; invalid input"
62900	ип
62901	"Basic Engine returned error number
	0xerrornumber"
62902	"Parity error from Basic Engine to Serial"
62903	"Communication time-out error"
62904	"Unexpected response from Basic Engine"
62905	"Radial loop could not be closed"
63000	IIII
63001	Basic Engine returned error number
	0xerrornumber"
63002	"Parity error from Basic Engine to Serial"
63003	"Communication time-out error"
63004	"Unexpected response from Basic Engine"
63100	" Number of times Tray went Open/Closed: nr1" " Total hours the CD laser was on: nr2" " Total hours the DVD laser was on: nr3" " Total hours the write laser was on: nr4"
63101	
	0xerrornumber"
63102	"Parity error from Basic Engine to Serial"
63103	"Communication time-out error"
63104	"Unexpected response from Basic Engine"
63200	
63201	"Basic Engine returned error number 0xerrornumber"
63202	"Parity error from Basic Engine to Serial"
63203	"Communication time-out error"
63204	"Unexpected response from Basic Engine"
63300	Momentary errors (Byte 1 - Byte 7): 0xb1 0xb2
63301	Cumulative errors (Byte 1 - Byte 7): : 0xb1 0xb2 0xb3 0xb4 0xb5 0xb6 0xb7 Fatal errors (Oldest - Youngest) : : 0xb1 0xb2 0xb3 0xb4 0xb5 "Basic Engine returned error number
	0xerrornumber"
63302	"Parity error from Basic Engine to Serial"
63303	"Communication time-out error"
63304	"Unexpected response from Basic Engine"
63400	an .
63401	"Basic Engine returned error number Oxerrornumber"
63402	"Parity error from Basic Engine to Serial"
63403	"Communication time-out error"
63404	"Unexpected response from Basic Engine"
63500	ип
63501	"Basic Engine returned error number 0xerrornumber"
63502	"Parity error from Basic Engine to Serial"
63503	"Communication time-out error"
63504	"Unexpected response from Basic Engine"
63505	"errorstring
	The basic engine will reject all player commands'
63900	
63901	"Basic Engine returned error number
	0xerrornumber" "Parity error from Basic Engine to Serial"
60000	Europ orror from Hacia Engine to Carial*
63902	
63903	"Communication time-out error"
63903 63904	"Communication time-out error" "Unexpected response from Basic Engine"
63903 63904 70000	"Communication time-out error" "Unexpected response from Basic Engine" "Echo test OK"
63903 63904 70000	"Communication time-out error" "Unexpected response from Basic Engine"

Error Nr	Error String
70300	"SoftwareVersion"
70301	"Can not find segment in FLASH ROM on the An- alogue Board"
70302	"Communication with Analogue Board fails"
70400	"HardwareVersion"
70401	"Can not find segment in FLASH ROM on the An- alogue Board"
70402	"Communication with Analogue Board fails"
70500	"Clock adjusted OK"
70501	"Can not adjust the clock on the Analogue Board."
70502	"Wrong date/time text size."
70503	"Communication with Analogue Board fails"
70600	"Tuner accessibility test OK"
70601	"Can not access tuner on the Analogue Board."
70602	"Communication with Analogue Board fails"
70700	"Frequency download OK"
70701	"Wrong frequency table size."
70702	"Can not download the frequency table into the analogue NVRAM."
70703	"Can not download the frequency table into the analogue NVRAM."
70704	"Communication with Analogue Board fails"
70800	"Data slicer test OK"
70801	"Test of the Data slicer on the Analogue Board fails."
70802	"Communication with Analogue Board fails"
70900	"Sound Processor test OK"
70901	"Test of the Sound Processor on the Analogue
	Board fails."
70902	"Communication with Analogue Board fails"
71000	"AV Selector test OK"
71001	"Test of the AV Selector on the Analogue Board fails."
71002	"Communication with Analogue Board fails"
71100	"NVRAM test OK"
71101	"Test of the NVRAM on the Analogue Board fails."
71102	"Communication with Analogue Board fails"
71200	"Video routing on the Analogue Board OK"
71201	"Routing the video on the Analogue Board fails."
71202	"Invalid input."
71203	"Communication with Analogue Board fails"
71300	"Audio routing on the Analogue Board OK"
71301	"Routing the audio on the Analogue Board fails."
71302	and the second of the second o
	"Invalid input."
71303	"Communication with Analogue Board fails"
71303 71400	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK"
71303 71400 71401	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix."
71303 71400 71401 71402	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid."
71303 71400 71401 71402 71403	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails"
71303 71400 71401 71402 71403 71500	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" ""
71303 71400 71401 71402 71403 71500 71501	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" "" "Invalid slash version, default slash version is set."
71303 71400 71401 71402 71403 71500 71501 71502	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" "Invalid slash version, default slash version is set." "Setting the slash version on the Analogue Board fails."
71303 71400 71401 71402 71403 71500 71501 71502	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" "Invalid slash version, default slash version is set." "Setting the slash version on the Analogue Board fails." "Communication with Analogue Board fails."
71303 71400 71401 71402 71403 71500 71501 71502 71503 71600	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" "Invalid slash version, default slash version is set." "Setting the slash version on the Analogue Board fails." "Communication with Analogue Board fails." "Communication with Analogue Board fails" "ApplicationVersion"
71303 71400 71401 71402 71403 71500 71501 71502 71503 71600 71601	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" "Invalid slash version, default slash version is set." "Setting the slash version on the Analogue Board fails." "Communication with Analogue Board fails" "ApplicationVersion" "Can not find segment in FLASH ROM on the Analogue Board"
71303 71400 71401 71402 71403 71500 71501 71502 71503 71600 71601	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" "Invalid slash version, default slash version is set." "Setting the slash version on the Analogue Board fails." "Communication with Analogue Board fails." "ApplicationVersion" "Can not find segment in FLASH ROM on the Analogue Board" "Communication with Analogue Board fails."
71303 71400 71401 71402 71403 71500 71501 71502 71503 71600 71601 71602 71700	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" "Invalid slash version, default slash version is set." "Setting the slash version on the Analogue Board fails." "Communication with Analogue Board fails." "ApplicationVersion" "Can not find segment in FLASH ROM on the Analogue Board" "Communication with Analogue Board fails." "Communication with Analogue Board fails." "DiagnosticsVersion"
71303 71400 71401 71402 71403 71500 71501 71502 71503 71600 71601	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" "Invalid slash version, default slash version is set." "Setting the slash version on the Analogue Board fails." "Communication with Analogue Board fails" "ApplicationVersion" "Can not find segment in FLASH ROM on the Analogue Board" "Communication with Analogue Board fails" "DiagnosticsVersion" "Can not find segment in FLASH ROM on the Analogue Board"
71303 71400 71401 71402 71403 71500 71501 71502 71503 71600 71601 71602 71700	"Communication with Analogue Board fails" "Audio routing on the Analogue Board OK" "Can not access switching matrix." "CVBS signal is invalid." "Communication with Analogue Board fails" "Invalid slash version, default slash version is set." "Setting the slash version on the Analogue Board fails." "Communication with Analogue Board fails" "ApplicationVersion" "Can not find segment in FLASH ROM on the Analogue Board" "Communication with Analogue Board fails" "DiagnosticsVersion" "Can not find segment in FLASH ROM on the Analogue Board fails" "DiagnosticsVersion"

Error Nr	Error String
71801	"Can not find segment in FLASH ROM on the An- alogue Board"
71802	"Communication with Analogue Board fails"
72300	no n
72301	"Clearing the NVRAM on the Analogue Board fails"
72302	"Communication with Analogue Board fails"
72400	"segment checksum is : checksum which is correct" for every segment
72401	"segment could not be found" or "segment check- sum is : checksumC ,however it should be : check- sumE" for every segment
72402	"Communication with Analogue Board fails"
73000	nn
73001	"Storing the external presets on the Analogue Board fails"
73002	"Communication with Analogue Board fails"
80000	"The DVIO module is present in the system."
80001	"The DVIO module is not present in the system."
80100	"The DVIO module has been reset OK."
80101	"The DVIO module is not present in the system."
80102	"The DVIO module could not be reset."
80103	"Could not initialise I2C before Reset."
80200	"The accessibility of the DVIO module is OK."
80201	"The DVIO board is not present in this DVDR."
80202	"Could not initialise I2C."
80203	"Unable to reset the DVIO module."
80204	"Unable to receive the reset indication from the DVIO module."
80205	"Unable to send the configuration to the DVIO module."
80206	"Unable to download the chip IDto the DVIO mod- ule."
80207	"Unable to set the mode of the DVIO module to IDLE."
80208	"Software Error in function HandleStateAwaitingReply!!"
80209	"Maximal number of retries reached by HandleS- tateSending !!"
80210	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80211	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80212	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY innes !!"
80213	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80214	"VSM UART error timeout transmitting command"
80215	"VSM UART error timeout receivin g reply"
80216	"VSM UART frame error occurred receiving from DVIO board"
80217	"VSM UART parity error occurred receiving from DVIO board"
80218	"The confirmation/indication from the DVIO module is invalid."
80300	"The accessibility of the DVIO module is OK."
80301	"The DVIO board is not present in 1this DVDR."
80302	"Could not initialise I2C."
80303	"Unable to reset the DVIO modue."
80304	"Unable to receive the reset inication from the DVIO module."
80305	"Unable to send the configuration to the DVIO module."
80306	"Unable to download the chip ID $\mathfrak h$ 1he DVIO module."

Error Nr	Error String
80307	"Unable to set the mode of the DVIO module to
	IDLE."
80308	"Software Error in function HandleStateAwaitingReply!!"
80309	"Maximal number of retries reached by HandleS- tateSending !!"
80310	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80311	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80312	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80313	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80314	"VSM UART error timeout transmitting command"
80315	"VSM UART error timeout receiving reply"
80316	"VSM UART frame error occurred receiving from DVIO board"
80317	"VSM UART parity error occurred receiving from DVIO board"
80318	"The confirmation/indication from the DVIO mod- ule is invalid."
80400	"The accessibility of the DVIO module is OK."
80401	"The DVIO board is not present in this DVDR."
80402	"Could not initialise I2C."
80403	"Unable to reset the DVIO module."
80404	"Unable to receive the reset indication from the DVIO module."
80405	"Unable to send the configuration to the DVIO module."
80406	"Unable to download the chip ID to the DVIO mod- ule."
80407	"Unable to set the mode of the DVIO module to IDLE."
80408	"Software Error in function HandleStateAwaitingReply!!"
80409	"Maximal number of retries reached by HandleS- tateSending !!"
80410	"Maximal number of retries (NACKs) reached (HandleStateSending)"
80411	"We tried to receive a reply for DVIO_MAX_RETRIES_ACKREPLY times !!"
80412	"We tried to receive a reply for DVIO_MAX_RETRIES_REPLY times !!"
80413	"We tried to receive an Ack for DVIO_MAX_RETRIES_ACK times!!"
80414	"VSM UART error timeout transmitting command"
80415	"VSM UART error timeout receiving reply"
80416	"VSM UART frame error occurred receiving from DVIO board"
80417	"VSM UART parity error occurred receiving from DVIO board"
80418	"The confirmation/indication from the DVIO module is invalid."
90000	11 11
90001	"Error cannot initialise I2C"
90002	"Error cannot initialise VIP"
90003	"Error cannot clear ADC enable pin"
90004	"Error cannot set VSM audio clock"
90005	"Error cannot initialise audio encoder"
90006	"Error cannot initialise VSM audio in port"
90007	"Error cannot initialise VSM audio in DMA port"
90008	"Error cannot initialise VSM audio out DMA port"
90009	"Error cannot initialise host decoder audio in"
90010	"Error cannot initialise audio VSM out port"

Error Ni	Error String
90011	"Error digital loop audio cannot start audio encod-
	er" audio cannot start audio encod-
90012	"Error cannot start VSM audio in DMA port"
90013	"Error cannot start VSM audio in port"
90014	"Error transfer data from audio encoder to VSM"
90015	"Error cannot start VSM AV out DMA port"
90016	"Error cannot start VSM AV out port"
90017	"Error transfer data from VSM to host decoder"
90018	"Error digital loop audio data in host memory and VSM memory differ"
90019	"Error digital loop audio data is not a valid MPEG stream"
90020	"Error digital loop audio data is not a digital si- lence"
90100	HI
90101	"Error routing the audio back to the digital board."
90102	"Error cannot initialise I2C"
90103	"Error cannot initialise VIP"
90104	"Error cannot set ADC enable pin"
90105	"Error cannot set VSM audio clock"
90106	"Error preparing the 12kHz audio-sine"
90107	"Error cannot initialise audio encoder"
90108	"Error cannot initialise VSM audio in port"
90109	"Error cannot initialise VSM audio in DMA port"
90110	"Error cannot initialise VSM audio out DMA port"
90111	"Error cannot initialise audio VSM out port"
90112	"Error cannot initialise host decoder audio in"
90113	"Error loop audio user/dealer cannot start audio
	encoder"
90114	"Error cannot start VSM audio in DMA port"
90115	"Error starting the 12kHz audio-sine"
90116	"Error transfer data from audio encoder to VSM"
90117	"Error cannot start VSM AV out DMA port"
90118	"Error cannot start VSM AV out port"
90119	"Error transfer data from VSM to host decoder"
90120	"Error: audio data in host memory and VSM memory differ"
90121	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90122	"Error: audio data in host memory contains si- lence!"
90123	"There is no correct audio frame in the buffer"
90124	"The audio frame has an illegal version bit"
90125	"The audio frame has an illegal bitrate-index"
90126	"The audio frame has an illegal sampling rate"
90127	"The CRC of the audio frame is wrong"
90128	"The audio frame is not MPEG-I layer II!"
90129	"Error cannot de-mute DAC on analogue board"
90200	811
90201	"Initialisation of I2C failed"
90202	"Initialisation of VIP and EMPIRE failed"
90203	"Initialisation of PLL / Link failed."
90204	"Next descriptor address set wrong."
90205	"Turning on the colourbar failed"
90206	"No I2C communication possible to start video en-
	coder."
90207	"Starting the video encoder failed."
90208	"Transfer of data from video encoder to VSM
00000	failed."
90209	"Stopping the encoder failed."
90210	"Turning off the colourbar failed."
90211	"Cannot intialize hostdecoder parallel input"
90212	"Cannot initialise VSM AV-out DMA port"

Error Ni	Error String
90213	"Cannot initialise VSM AV-out port"
90214	"Cannot start VSM AV-out DMA port"
90215	"Cannot start VSM AV-out DMA port"
	· ·
90216	"Transfer of data from VSM to host decoder failed."
90217	"VSM and Hostdec memory do not match (compared after transfer)"
90218	"Decoding of the video data in the hostdecoder memory failed"
90219	"The data in the hostdecoder is not equal to a col- ourbar"
90220	"The video encoder did not return the Group Of Picture count."
90221	"The video encoder did not receive data from the VIP."
90223	"Initialisation of VIP and EMPRESS failed"
90224	"The video encoder did not return the current status."
90225	"The video encoder timed out in BUSY mode. (no VIP input)"
90226	"The video encoder did not return the current bi- trate."
90227	"The video encoder did not switch to ENCODING mode."
90228	"The video encoder could not start from STOP/IDLE mode."
90229	"The video encoder did not switch from IDLE to STOP mode."
90300	пн
90301	"Initialisation of I2C failed"
90302	"I2C communication to VIP failed"
90303	"Initialisation of VIP failed"
90304	"Generation of Close Caption data failed"
90305	"VIP not locked to video signal"
90306	"Initialisation of VBI Extractor failed
90307	"No CC data received"
90308	"Closed Caption data overrun"
90309	"Closed Caption data does not match"
90310	"Switch off ColourBar failed"
90400	nw .
90401	"Initialisation of I2C failed"
90402	"Initialisation of VIP and EMPIRE failed"
90403	"Initialisation of PLL / Link failed."
90404	"Next descriptor address set wrong."
90405	"Turning on the colourbar failed"
90406	"No I2C communication possible to start video encoder."
90407	"Starting the video encoder failed."
90408	"Transfer of data from video encoder to VSM failed."
90409	"Stopping the encoder failed."
90410	"Turning off the colourbar failed."
90411	"Cannot intialize hostdecoder parallel input"
90412	"Cannot initialise VSM AV-out DMA port"
90413	"Cannot initialise VSM AV-out port"
90414	"Cannot start VSM AV-out DMA port"
90415	"Cannot start VSM AV-out DMA port"
90416	"Transfer of data from VSM to host decoder
	failed."
90417	"VSM and Hostdec memory do not match (compared after transfer)"
90418	"Decoding of the video data in the hostdecoder memory failed"

Error Ni	Error String
90419	"The data in the hostdecoder is not equal to a col-
	ourbar"
90420	"The video encoder did not return the Group Of Picture count."
90421	"The video encoder did not receive data from the VIP."
90422	"Execution of the command on the analogue board failed."
90423	"Initialisation of VIP and EMPRESS failed"
90424	"The video encoder did not return the current sta-
	tus."
90425	"The video encoder timed out in BUSY mode. (no VIP input)"
90426	"The video encoder did not return the current bitrate."
90427	"The video encoder did not switch to ENCODING mode."
90428	"The video encoder could not start from STOP/IDLE mode."
90429	"The video encoder did not switch from IDLE to STOP mode."
90500	ан
90501	"Initialisation of I2C failed"
90502	"I2C communication to VIP failed"
90503	"Initialisation of VIP failed"
90504	"Generation of Close Caption data failed"
90505	"VIP not locked to video signal"
90506	"Initialisation of VBI Extractor falled
90507	"No CC data received"
90508	"Closed Caption data overrun"
90509	"Closed Caption data does not match"
90510	"Switch off ColourBar failed"
90511	"Execution of the command on the analogue board failed."
90600	
90601	"Initialisation of I2C failed"
90602	"Initialisation of VIP and EMPIRE failed"
90603	"Initialisation of PLL / Link failed."
90604	"Next descriptor address set wrong."
90605	"Turning on the colourbar failed'
90606	"No I2C communication possible to start video encoder."
90607	"Starting the video encoder failed."
90608	"Transfer of data from video encoder to VSM failed."
90609	"Stopping the encoder failed."
90610	"Turning off the colourbar failed."
90611	"Cannot intialize hostdecoder para llel input"
90612	"Cannot initialise VSM AV-out DNA port"
90613	"Cannot initialise VSM AV-out port"
90614	"Cannot start VSM AV-out DMAport"
90615	"Cannot start VSM AV-out port"
90616	"Transfer of data from VSM b host decoder failed."
90617	"VSM and Hostdec memory donot match (compared after transfer)"
90618	"Decoding of the video data in the hostdecoder memory failed"
90619	"The data in the hostdecoder is not equal to a col- ourbar"
90620	"The video encoder did not return the Group Of Picture count."
90621	"The video encoder did not receive data from the VIP."

	Error String
90622	"Execution of the command on the analogue board failed."
90623	"Initialisation of VIP and EMPRESS failed"
90624	"The video encoder did not return the current status."
90625	"The video encoder timed out in BUSY mode. (no VIP input)"
90626	"The video encoder did not return the current bitrate."
90627	"The video encoder did not switch to ENCODING mode."
90628	"The video encoder could not start from STOP/IDLE mode."
90629	"The video encoder did not switch from IDLE to STOP mode."
90700	MU
90701	"Initialisation of I2C failed"
90702	"I2C communication to VIP failed"
90703	"Initialisation of VIP failed"
90704	"Generation of Close Caption data failed"
90705	"VIP not locked to video signal"
90706	"Initialisation of VBI Extractor failed
90707	"No CC data received"
90708	"Closed Caption data overrun"
90709	"Closed Caption data does not match"
90710	"Switch off ColourBar failed"
90711	"Execution of the command on the analogue board failed."
90800	ив
90801	"Error routing the audio back to the digital board."
90802	"Error cannot initialise I2C"
90803	"Error cannot initialise VIP"
90804	"Error cannot set ADC enable pin"
90805	"Error cannot set VSM audio clock"
90806	"Error preparing the 12kHz audio-sine"
90807	"Error cannot initialise audio encoder"
90808	"Error cannot initialise VSM audio in port"
90809	"Error cannot initialise VSM audio in DMA port"
90810	"Error cannot initialise VSM audio out DMA port"
90811	"Error cannot initialise audio VSM out port"
90812	"Error cannot initialise host decoder audio in"
90813	"Error loop audio user/dealer cannot start audio encoder"
90814	"Error cannot start VSM audio in DMA port"
90815	"Error starting the 12kHz audio-sine"
90816	"Error transfer data from audio encoder to VSM"
90817	"Error cannot start VSM AV out DMA port"
90818	"Error cannot start VSM AV out port"
90819	"Error transfer data from VSM to host decoder"
90820	"Error: audio data in host memory and VSM mem- ory differ"
90821	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90822	"Error: audio data in host memory contains si- lence!"
90823	"There is no correct audio frame in the buffer"
90824	"The audio frame has an illegal version bit"
90825	"The audio frame has an illegal bitrate-index"
90826	"The audio frame has an illegal sampling rate"
90827	"The CRC of the audio frame is wrong"
90828	"The audio frame is not MPEG-I layer II!"
90829	"Error cannot de-mute DAC on analogue board"
90900	ии

Error Nr	Error String
90901	"Error routing the audio back to the digital board."
90902	"Error cannot initialise I2C"
90903	"Error cannot initialise VIP"
90904	"Error cannot set ADC enable pin"
90905	"Error cannot set VSM audio clock"
90906	"Error preparing the 12kHz audio-sine"
90907	"Error cannot initialise audio encoder"
90908	"Error cannot initialise VSM audio in port"
90909	"Error cannot initialise VSM audio in DMA port"
90910	"Error cannot initialise VSM audio out DMA port"
90911	"Error cannot initialise audio VSM out port"
90912	"Error cannot initialise host decoder audio in"
90913	"Error loop audio user/dealer cannot start audio encoder"
90914	"Error cannot start VSM audio in DMA port"
90915	"Error starting the 12kHz audio-sine"
90916	"Error transfer data from audio encoder to VSM"
90917	"Error cannot start VSM AV out DMA port"
90918	"Error cannot start VSM AV out port"
90919	"Error transfer data from VSM to host decoder"
90920	"Error: audio data in host memory and VSM memory differ"
90921	"Error: audio data in host memory contains wrong frequency: frequency Hz"
90922	"Error: audio data in host memory contains si- lence!"
90923	"There is no correct audio frame in the buffer"
90924	"The audio frame has an illegal version bit"
90925	"The audio frame has an illegal bitrate-index"
90926	"The audio frame has an illegal sampling rate"
90927	"The CRC of the audio frame is wrong"
90828	"The audio frame is not MPEG-I layer II !"
90929	"Error cannot de-mute DAC on analogue board"
140000	nn
140001	"I2C to Clock failed" or "I2C initialisation failed"
140100	411
140101	"I2C to Clock failed" or "I2C initialisation failed"

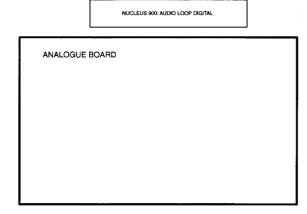
Loop Tests 5.5

The following loops can be distinguished:

- Loops performed on the digital board only
- User Dealer loops performed on the digital and analogue
- System loops performed via an external connection: outputs are looped back to the inputs.

5.5.1 Nucleus 900: Digital Audio Loop

This nucleus tests the audio path through the digital board



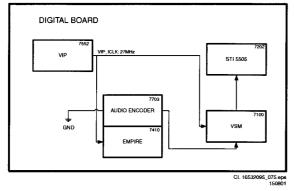


Figure 5-9

5.5.2 Nucleus 901: Audio User Dealer Loop

A PCM audio sine of 12kHz is generated in the Sti5505 for a while and sent to the analogue board. The signal coming from the analogue board is encoded again and sent to the memory of the host decoder for comparison. This nucleus tests the components on the audio signal path:

- Host decoder Sti5505
- Flex connection between connector 1602 (digital board) and connector 1900 (analogue board)
- Op-amp
- Scart switch STV6410
- ADC
- Audio Encoder
- VIP
- VSM

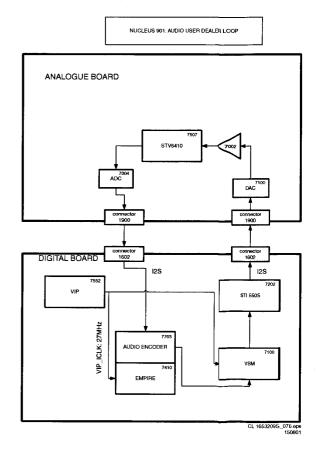
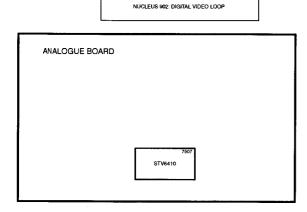


Figure 5-10

5.5.3 Nucleus 902: Digital Video Loop

A colourbar generated in the host decoder is looped through the VIP, Empire, and VSM and checked again in the host decoder. The following components are tested on the video signal path:

- VIP
- Empire
- VSM
- Host decoder



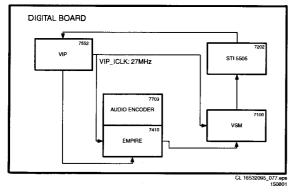


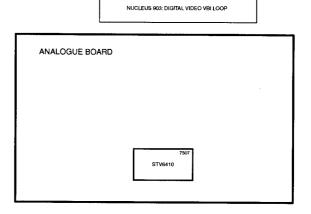
Figure 5-11

5.5.4 Nucleus 903: Digital Video VBI Loop

Nucleus for testing the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

This is done by using the internal test signal source (digital board only)



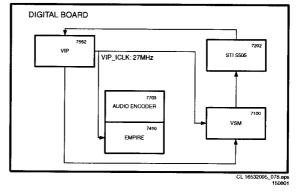


Figure 5-12

5.5.5 Nucleus 904: System Video Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board the video signal will be routed to the SCART (EUROPE) or CINCH (NAFTA). There it will be looped back externally by means of the proper cable

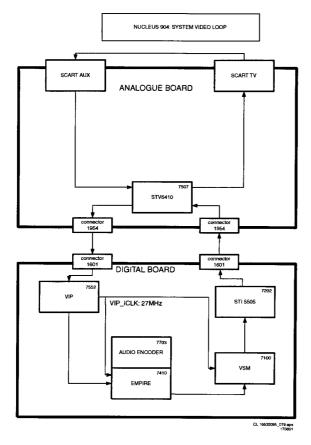


Figure 5-13

5.5.6 Nucleus 905: System Video VBI Loop

This nucleus tests the components on the video signal path:

- The VIP
- The VSM
- The Host Decoder

The video CVBS signal is routed to the output of the analogue board where it will be looped back by means of an external cable

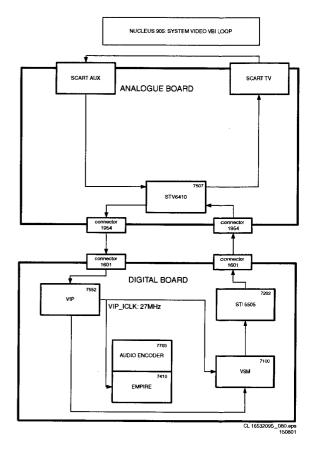


Figure 5-14

5.5.7 Nucleus 906: Video User Dealer Loop

Nucleus for testing the components on the video signal system path:

- The VIP
- The video encoder
- The VSM
- The host decoder
- The analogue board

On the analogue board, the video signal is internally routed back to the digital board.

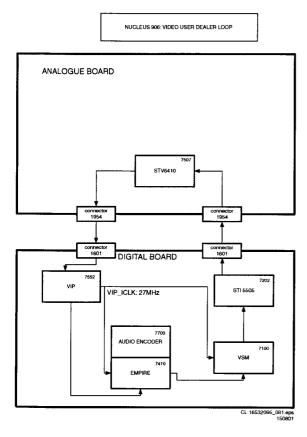


Figure 5-15

5.5.8 Nucleus 907: Video VBI User Dealer Loop

This nucleus tests the components on the video VBI signal path:

- The VIP
- The VSM
- The Host Decoder

The signal is routed back internally on the analogue board

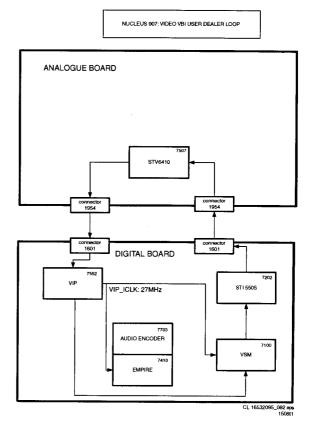


Figure 5-16

5.5.9 Nucleus 908: System Audio Loop Scart

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

On the analogue board, audio is passed to the SCART connector, where a SCART cable needs to be used to loop back the audio signal to the digital board

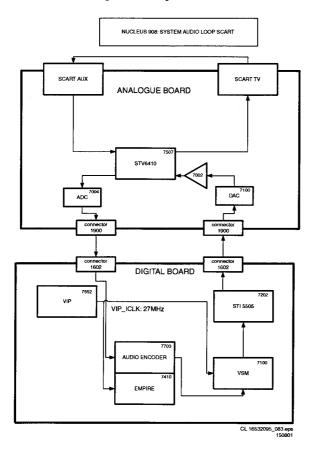


Figure 5-17

5.

5.5.10 Nucleus 909: System Audio Loop CINCH

Nucleus for testing the components on the audio signal path:

- The hostdecoder
- The analogue board
- The audio encoder
- The VSM

On the analogue board the audio is passed to the CINCH connector, where a CINCH cable needs to be used to loop back the audio signal to the digital board

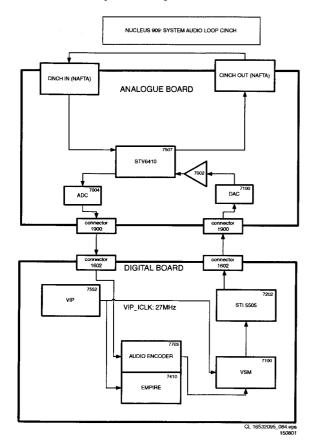
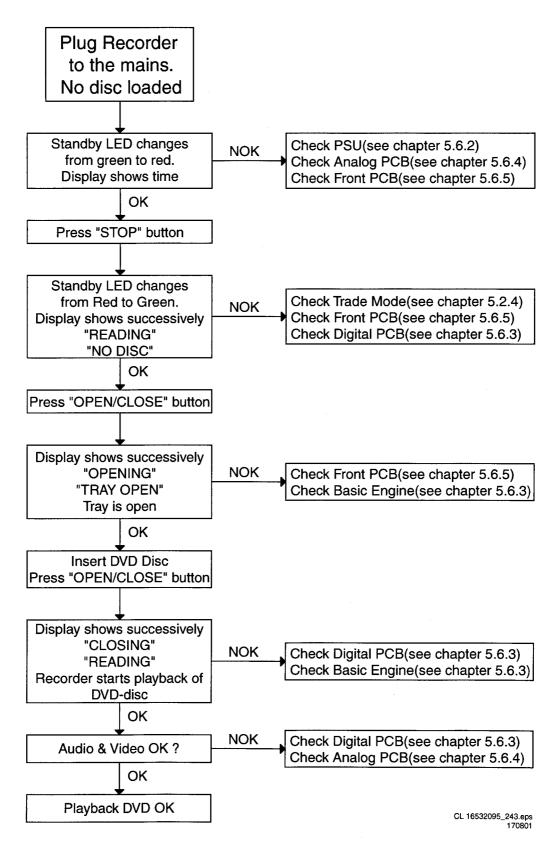


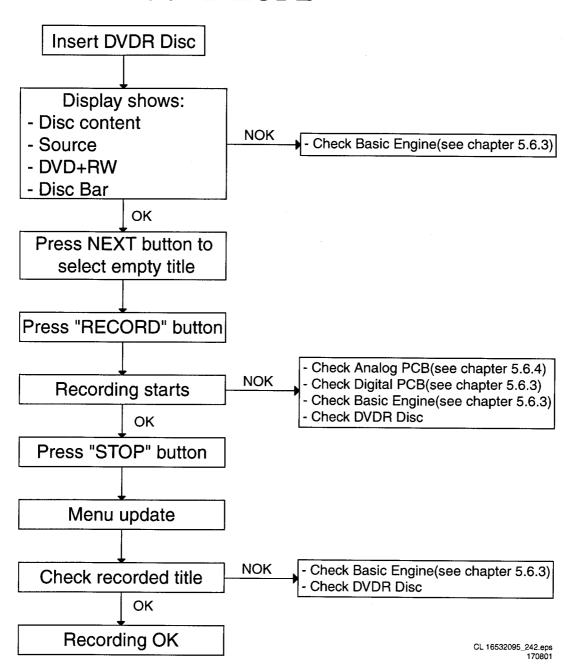
Figure 5-18

5.6.1 General

PLAYBACK MODE



RECORD MODE



5.6.2 Power Supply

Remove all the connectors from the PSU Check DC voltages on connector 0205: +12Vstby, +5V2stby, -5Nstby, -Vgnstby, +33Vstby +12Vstby and +5V2stby are oke. None of the voltages are present All voltages are present. Check +12Vreg circuit: Check +33Vstby circuit: Standby voltages are oke. Check DC - D6210, C2210, C2212 - D6200, C2200, R3200, D6201, R3201 voltages on connectors 0207 and 0209. Check +Vreg circuit: Check -5Nstby circuit: Connector 0207: D6240, C2240, C2242 D6220, C2220, IC7220, C2222, C2221 +3V3, +5V, -5V, +12V. Connector 0209: Check Prot 3V3 circuit: Check FLYB circuit: D6215, C2214, C2215, - D6221, T7241, R3220, R3221, R3222 +3V3, +12V, +5V, -5V, STBY_ctrl. R3520, R3521, D6520 R3223. Check -Vgnstby circuit: If not oke, check supply path of failed Connect PSU to a mains isolated variac. - D6230, C2230, R3230, D6231, R3233, supply voltages. R3234, C2235. Turn the input voltage up and measure voltage across C2125. Do not exceed max. mains voltage indicated on player. This voltage must be +/- 1.41 x Vin AC. Check if STBY_ctrl is LOW. - Check standby control path via digital board to analog board. Check primary circuit: - F1120, D6151, D6152, D6153, D6154, - R3120, L5120, L5520, C2125. Check +12V circuit: If fuse 1120 is defective, always check Q7125, D6145, T7140, Rsense (R3133, R3134, R3135, R3136 and R3137). must be present for the other voltages - Q7511, T7512, D6511, D6512, - R3511, R3513, R3514, L551, C2512. Check +3V3 circuit: Check with an oscilloscope Vds and Vg - Q7520, Q7521, L5520, C2521, F1520, of Q7125. - R3522, R3523, R3524, R3525, C2520. Check +5V circuit: - Q7501, Q7502, L5501, C2502, R3501 NO - R3502, R3503, R3504, C2540. Is PSU ticking? Check +3V3E circuit: - Q7505, Q7506, D6505, L5505, C2506, YES - R3505, R3506, R3507, R3508, C2502. Check -5V circuit: - Q7515, D6515, L5515, C2515, R3515. Check power switch circuit: Check start-up circuit: - Q7125, D6130, D3131, D6132 - R3125, R3126, R3141, R3132 - D6145, D6146, L5125 - Q7125, L5131, R3150, C2146 - C2136 - R3131, R3132, R3133, R3134 If oke, the power supply seems to be ok. Check the other boards in he player - R3135, R3136, R3137, R3146 for the cause of the overload. **Check Control circuit** - T7140, D6141, D6142, L5131, - C2144, C2145, C2147, C2151 - R3151, R3147, R3148, R3150 **Check Regulation circuit** - T7251, Q7200, R3250, R3253 - R3254, R3255, R3256, C2251 **Check Overvoltage circuit** - T7142, D6143, D6144, - R3149, R3144, C2152, C2142 **Check Overload circuit** - T7141, T7143, R3145, R3143, - R3142, C2143. CLi6532095_085.eps

5.6.3 Digital Board

Start-Up DSW

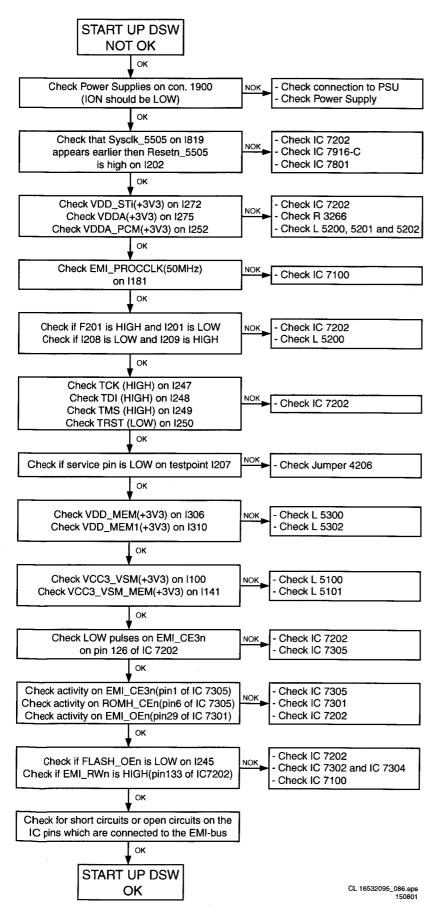
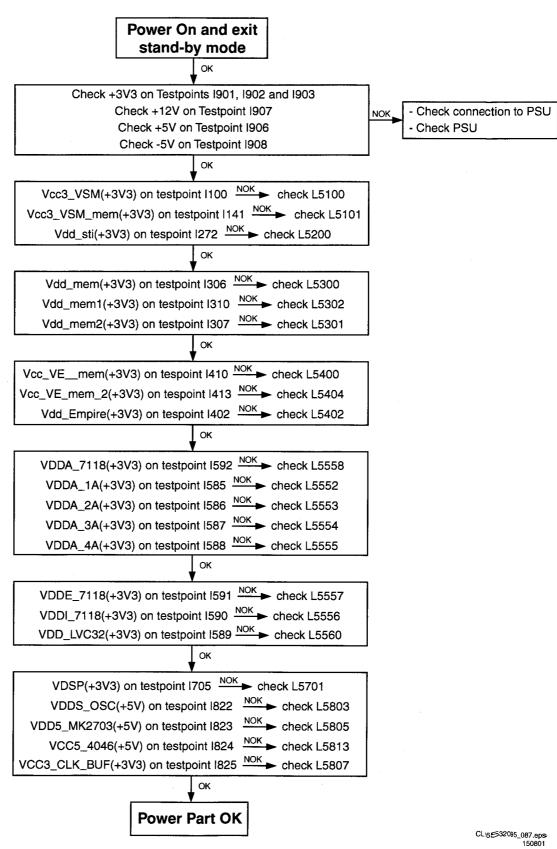


Figure 5-20

POWER PART CHECK DIGITAL BOARD

USE DIGITAL BOARD CIRCUIT DIAGRAMS 1 2, 3, 4, 5, 7 AND 8 AND DIGITAL BOARD BOTTOM VIEW TESTPOINTS



Reset and Clock Check

RESET & CLOCK CHECK DIGITAL BOARD

USE DIGITAL BOARD CIRCUIT DIAGRAMS 1,2,7 AND 8 AND DIGITAL BOARD BOTTOM VIEW TESTPOINTS

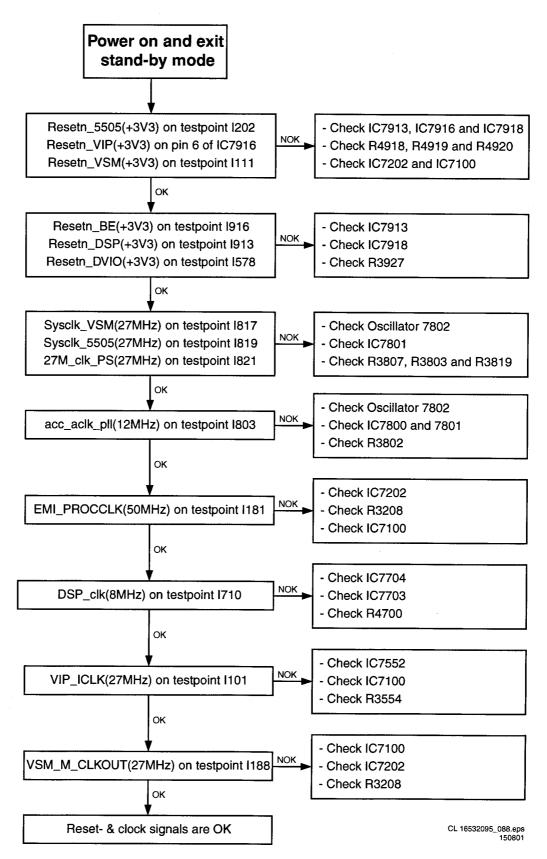


Figure 5-22

DSW MEMORY TESTS

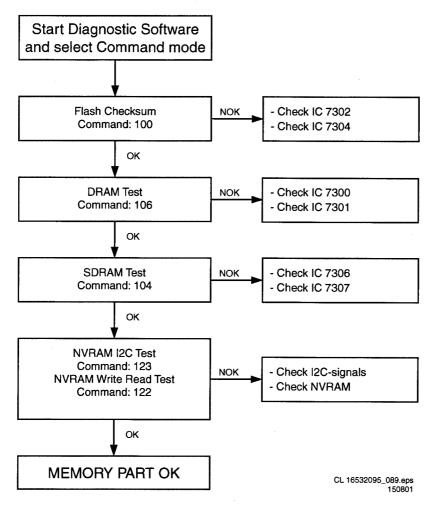


Figure 5-23

DSW VSM TESTS

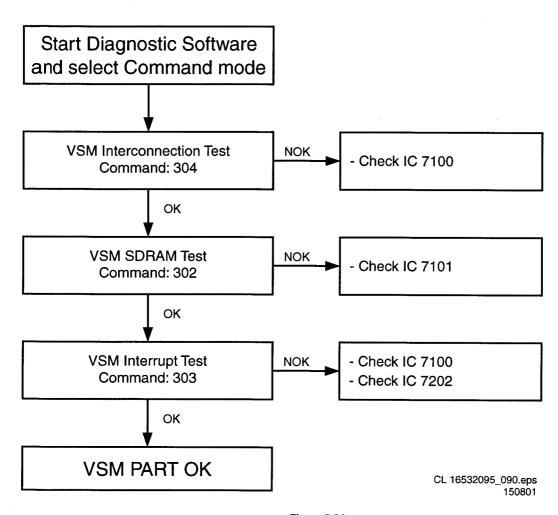


Figure 5-24

DSW Audio Video Encoder Tests

DSW AUDIO VIDEO ENCODER TESTS

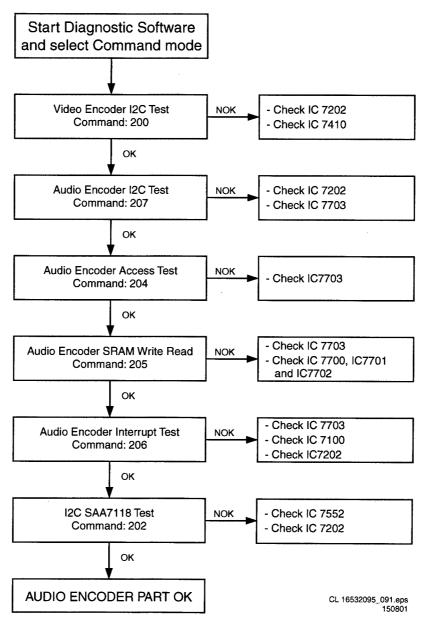


Figure 5-25

DSW Audio Part Check

DSW AUDIO PART CHECK

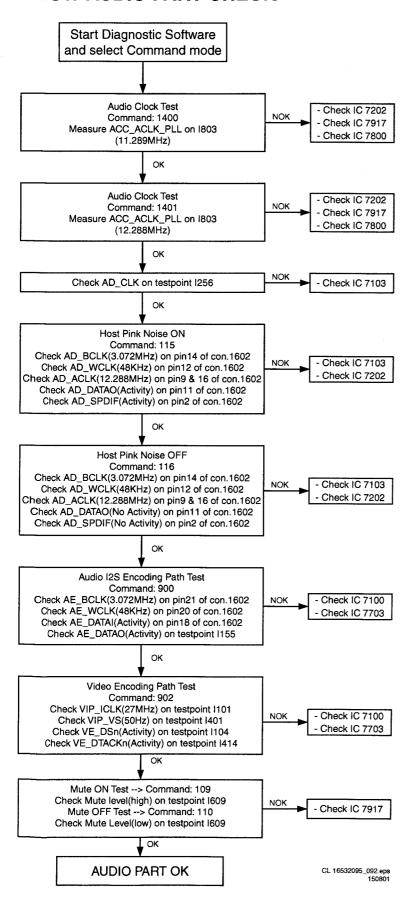


Figure 5-26

DSW Video Part Check

DSW VIDEO PART CHECK

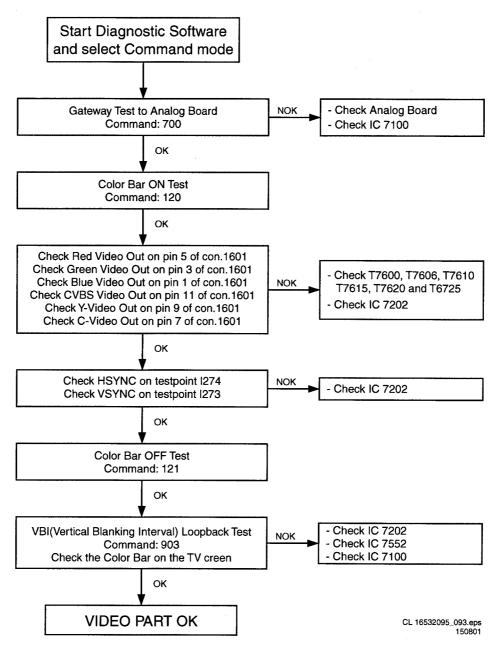


Figure 5-27

DSW Basic Engine Check

DSW BASIC ENGINE TESTS

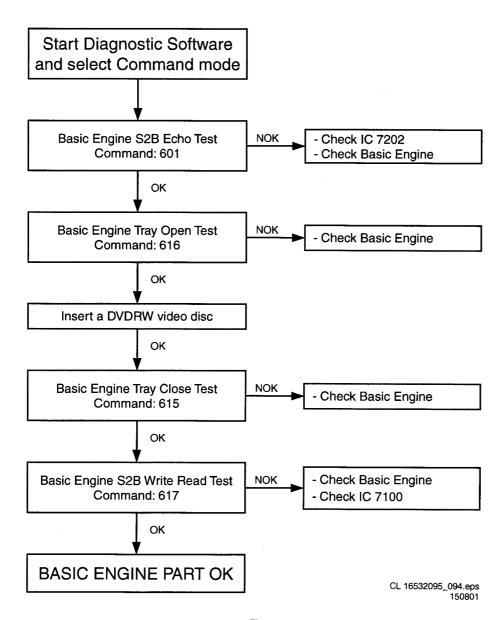
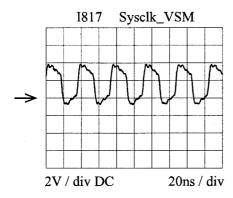
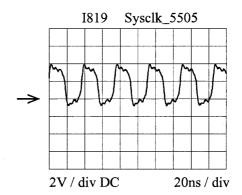
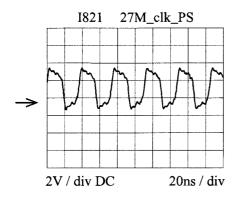


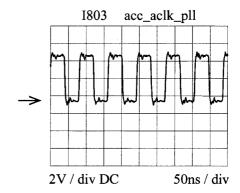
Figure 5-28

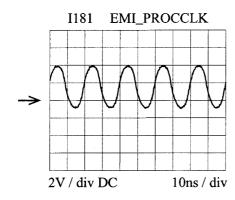
Waveforms Digital Board

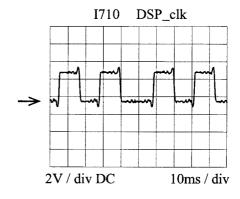


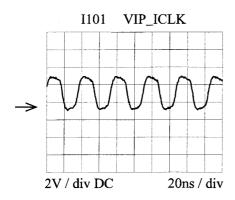


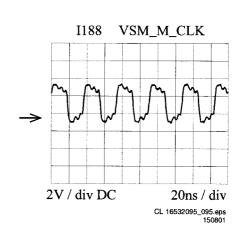




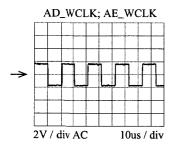


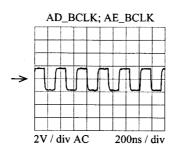


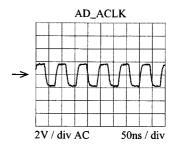


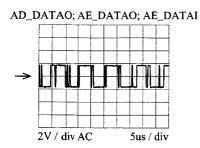


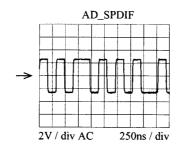
Waveforms Digital Board

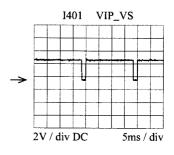


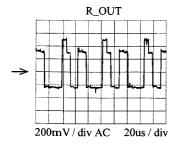


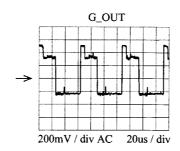


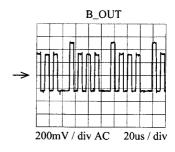


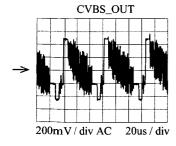


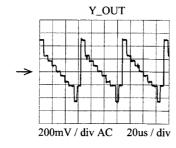


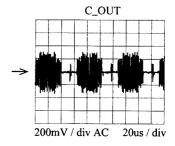


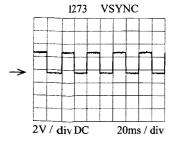


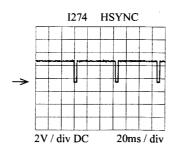












CL 16532095_096.eps 150801

Figure 5-30

Measurement Points Overview

E334 BCLK BCLK Low DIGI CLK II 1900 2 DAC E5		,					 	
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D D D D D D D D D D	CS	DAC	190014	CLK In	PCMCLK from DIGI	D_PCMCLK		P1001
Decoration D	CS	DAC	1900 12	nl stsO	A Data from DIGI	0ATAQ_Q		F0012
Post	DS	DVC	11 0061	CLK In	WCLK from DIGI	D_WCLK		F0011
Post	DS	DAG	6 0061	CTK III	BCLK from DIGI	D_BCLK		6000∃
Page	DS	DAC	1 0061	CTK IP	PCMCLK from DIGI	A_PCMCLK		2000∃
February Pack Pac	DS	DVG	1900 2	Data Out	IDIG ot ata A	TAQ_A		E0002
February February	DS	DAG	19003	CTK IP	WCLK from DIGI	A_WCLK		F0003
Mail	ES	DAC	1900 2	СГК I	BCLK from DIGI	∀ BCLK		F0002
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March Marc	91	101	1954 20	nl ni2	D_G f. DIGI	D_G		
MP X Name D_C N Nime Ni	91			ul nis			1	
March Marc	91	101	91 7961					
MP X Name D_CVBS D_CVBS f. DIGI V In 1954 19 In 1954 12 IO1 IB F5002 ALIN_SCS SCS A R IN W IF IN 1950 2B IO4 CO F5006 ALIN_SCS SCS A IN W IF IN 1950 8B IO4 CO F5006 ALIN_SCS SCS A IN SIN IN W IN IN	91	101	71 7961	UΙΛ			 	
MP X Name Description Type Part Name Coord.	SI	101	1624 15	UΙΛ	D_CVBS f. DIGI			
MP	Ы	101	1954 09			~		
MP X Name Description Type Part Name Coord.	bl	101	496t 07		A_C to DIGI	o_A_C		
MP X Name Description Type Part Name Coold F5002 ARIn, SC2 SC2 A R IW W F IM 1950 2B IO4 CQ F5006 ALIn, SC2 SC2 A IW W F IM 1950 2B IO4 CQ F5006 ALIN, SC2 SC2 Y IW SIn IM 1950 2B IO4 CQ F5020 ACVBSIN, SC2 SC2 Y IW SIn IM 1950 2B IO4 CQ F5030 ACVBSIN, SC2 SC2 Y IW SIn IM 1950 3B IO4 CQ F5031 BC, SC3 SC3 P IM SIn IM 1950 1AB IO1 F13 F5031 BC, SC3 SC3 P IM SIn IM 1950 1AB IO4 D9 F5031 BC, SC3 SC3 P IM SIn IM 1950 1AB IO4 E9 F5031 BC, SC3 SC3 P IM SIn IM 1950 1AB IO4 D9 F503 BC, CU SIN IM SIN IM IO4 D9 IO4 <td< td=""><td>Ы</td><td>101</td><td></td><td></td><td></td><td></td><td></td><td></td></td<>	Ы	101						
MP X Name Description Type Part Pack Pack Name Coord F5002 ARIn, SC2 SC2 A R IW W F IM 1960 SB 104 CQ F5006 ALIN, SC2 SC2 A IW W F IW 1950 SB 104 CQ F5006 ALIN, SC2 SC2 Y IW SIn IW 1950 AB 104 CQ F502 BC SC1 SC1 BC Sin IW 1950 AB 104 EQ F503 BC SC1 SC1 BC SIn IW 1950 AB 104 EQ F504 BC SC1 SC1 BC SIn IW 1950 AB 104 DQ F504 BC SC2 SC2 BIN C Out Sin IM 1950 AB 104 EQ F504 BC SC2 SC2 BIN C Out Sin IM 1950 AB 104 EQ F504 BC SC2 SC2 BIN C Out Sin IM 1950 AB 104 EQ F504 BC SC3 SC2 BIN C Out Sin IM 104 EQ 104 EQ	ÞΙ							
MP X Name Description Type Part Name Coord.	ÞΙ	101	1954 02	еир	GNDV to DIGI	CMDA	 1	
MP X Name Description Type Part Pact Pact Pact Pact Pact Pact Pact Pac	EI	POI	10 7961	Sin Out				
MP X Name Description Type Part Name Cood. F5002 ARIn_SC2 SC2 R II HF IN HF IN 1950 2B IO4 C9 F5006 ALLIN_SC2 SC2 R II HF IN HF IN HF IN HO COU 1950 8B IO4 C9 F5020 ACVBSIN_SC2 SC2 V IN Sin In 1950 10A F9 F9 F6 <								
MP X Name Description Type Part Name Name Description Type Part Name Description Type Part Name Description Part Name Description Part Name	63	†OI	1950 15B	al nis			 <u> </u>	
MP X Name Description Type Part Name Coord F5002 ARIn_SC2 SC2 A R IW WF IM 1950 SB IO4 C9 F5006 ALIn_SC2 SC2 A IW SIn IM 1950 SB IO4 C9 F5006 ALIn_SC2 SC2 V IW Sin IM 1950 SB IO4 C9 F502 BC_SC1 SC1 PB DC Out 1950 AB IO1 F13 F530 PG_SC1 SC1 PB DC Out 1950 AB IO1 F14 F531 BC_SC1 SC1 PB DC Out 1950 AB IO1 F14 F530 PG_SC1 SC1 PB DC Out 1950 AB IO1 F14 F527 PG_SC2 SC2 B IN C Out Sin In* 1950 AB IO1 F14 F500 PG_GC2 SC2 B IN C Out Sin In* 1950 AB IO1 H13 F501 PG_GC3 SC2 B IN C Out Sin In* IO1 H13 F502	6CI	†OI	811 0961	ul uis			-	
MP X Name Description Type Part Name Coord F5002 ARIn_SC2 SC2 A R IW WF IN 1950 SB IO4 C9 F5006 ALIn_SC2 SC2 A IW SIn D C Ur 1950 SB IO4 C9 F5020 ACVBSIN_SC2 SC2 Y IW Sin Du 1950 2B IO4 C9 F531 BC_SC1 SC1 P60 DC Out 1950 1AA IO1 F13 F532 BC_SC1 SC1 P60 DC Out 1950 1AA IO1 F14 F534 BC_SC1 SC1 P60 DC Out 1950 1AA IO1 F14 F524 BC_SC1 SC1 P60 DC Out 1950 1AA IO1 F14 F525 BC_SC2 SC2 B IN C Out Sin Out 1950 1AA IO1 F14 F530 BC_SC2 SC2 B IN C Out Sin Out 1950 1AA IO1 H13 F530 BC_SC3 SC2 B IN C Out Sin In* 1950 1AA IO1 H13 <td>6Q</td> <td>‡OI</td> <td>1950 88</td> <td>DC OT</td> <td>•</td> <td></td> <td></td> <td></td>	6Q	‡OI	1950 88	DC OT	•			
MP X Name Description Type Part Name Coord F5002 ARIn_SC2 SC2 A IN HF IN 1950 2B IO4 C9 F5006 ARIn_SC2 SC2 A IN HF IN 1950 2B IO4 C9 F5006 ACVBSIN_SC2 SC2 Y IN Sin_Out* 1950 2B IO4 C9 F502 ACVBSIN_SC2 SC2 Y IN Sin_Out* 1950 2B IO4 F9 F536 BC_SC1 SC1 BC Sin_Out* 1950 10A IO1 F13 F545 BC_SC1 SC1 P50 DC Out 1950 10A IO1 F14 F524 Goul_SC1 SC1 P50 DC Out 1950 10A IO1 F14 F527 RC2 SC1 P50 SC1 P50 SC1 P50 IO1 F14 F530 RC3 SC2 SC3 SC3 SC3 SC4 IO1 G14 F530 RC4 SC3 SC3 SC4 SC4 IO2 <	6G	†OI	8Z 0961		SCZ B IN C OU	BC_SCS	 <u> </u>	
MP X Name Description Type Part Name Coord F5002 Achin_SC2 SC2 A IN HF IN 1950 2B IO4 C9 F5006 Achin_SC2 SC2 A IN HF IN 1950 2B IO4 C9 F5026 AcvBSIN_SC2 SC2 Y IN Sin Out* 1950 2B IO4 F9 F536 BC_SC1 SC1 BC Sin Out* 1950 2B IO4 F9 F537 BC_SC1 SC1 P50 DC Out 1950 10A IO1 F14 F524 BC_SC1 SC1 P50 DC Out 1950 10A IO1 F14 F524 BCQUL_SC1 SC1 P50 DC Out 1950 10A IO1 F14 F524 BCQUL_SC1 SC1 P50 DC Out 1950 10A IO1 F14 F524 BCQUL_SC1 SC1 P50 Sin Out 1950 10A IO1 F13 F527 BCQUL_SC1 SC1 P50 Sin Out 1950 1A IO1 G14 <td>H13</td> <td>IOI</td> <td>A81 0361</td> <td>DC Out</td> <td></td> <td></td> <td>1</td> <td></td>	H13	IOI	A81 0361	DC Out			1	
MP X Name Description Type Part Name Coord F5002 ARIn_SC2 SC2 A R IN WF IN 1950 2B IO4 C9 F5006 ARIn_SC2 SC2 Y IN SIn Du 1950 6B IO4 C9 F5020 YCVBSIN_SC2 SC2 Y IN Sin Du 1 1950 2B IO4 C9 F525 BC_SC7 SC1 BC Sin Du 1 1950 2B IO4 C9 F521 BC_SC7 SC1 Pin B DC Out 1950 2B IO1 F13 F524 BC_SC7 SC1 Pin B DC Out 1950 10A IO1 F14 F524 BC_SC7 SC1 P50 DC Out 1950 10A IO1 F14 F524 BC_SC7 SC1 P50 DC Out 1950 10A IO1 F14 F524 BC_SC7 SC1 P50 DC Out 1950 10A IO1 F14							 	
MP X Name Description Type Part Name Cood. F5002 ARIn_SC2 SC2 A R IW WF IM 1950 2B IO4 C9 F5006 ACVBSIN_SC2 SC2 Y IW Sin Out* 1950 2B IO4 C9 F5020 YCVBSIN_SC2 SC2 Y IW Sin Out* 1950 2B IO4 F9 F513 BC_SC1 SC1 BC Sin Out* 1950 R IO1 E13 F514 BC2C1 SC1 Pin B DC Out 1950 AB IO1 F14 F515 BC3C1 SC1 Pin B DC Out 1950 AB IO1 F14 F516 BC3C1 SC1 Pin B DC Out 1950 AB IO1 F14 F516 BC3C1 SC1 Pin B DC Out 1950 AB IO1 F14	F13	101	A11 0361	JuO ni2		VIII.		
Wb X N game Describtion Type Part Name Describtion Type Part Name Doc Ort 1960 8P 101 F13 F5005 ACVBSIN_SCS SCS A IN Sin IN 1960 2B 104 E9 F5006 ACVBSIN_SCS SCS A IN NF IN 1960 2B 104 E9 F5007 ABIN_SCS SCS A IN NF IN 1960 5B 104 C9 F5008 ABIN_SCS SCS A IN NF IN 1960 5B 104 C9 F501 ABIN_SCS SCS A IN NF IN 1960 5B 104 C9 F502 ABIN_SCS SCS A IN NF IN 1960 5B 104 C9 F503 ABIN_SCS SCS A IN NF IN 1960 5B 104 C9 F504 ABIN_SCS SCS A IN NF IN 1960 5B 104 C9 F505 ABIN_SCS SCS A IN NF IN 1960 5B 104 C9 F506								
E230 BC_SC1 SC1 BC Sin Ont*, 1360 VA 104 E3 E2005 ACABSIN_SCS SCS A IN NE IN 1360 SB IO4 E3 E2006 AFIL_SCS SCS A IN NE IN 1360 SB IO4 E3 E2007 AFIL_SCS SCS A IN NE IN 1360 SB IO4 E3 BC_SC1 SCS A IN NE IN 1360 SB IO4 C3 C3 BC_SC3 SCS A IN NE IN 1360 SB IO4 C3 C3 BC_SC3 SCS A IN NE IN 1360 SB IO4 C3 C3 BC_SC3 SCS A IN NE IN 1360 SB IO4 C3 C3 BC_SC3 SCS A IN NE IN 1360 SB IO4 C4 C3 BC_SC3 SCS A IN NE IN 1360 SB IO4 C4 C3 BC_SC3 SCS A IN NE IN 1360 SB IO4 C4 C3							 1	
Wb X A Ngme Describition Type Part Name Coord. Wb X Y Name Describition Type Part Name Coord.								
MP X Y Name Description Type Part Name Coord. F5002 ARIO ARIO ARIO 1950 SB 104 C9 F5006 ARIO ARIO ARIO 1950 GB 104 C9 F5006 ARIO ARIO ARIO 1950 GB 104 C9							 †	
MP X Y Name Description Type Part Name Coord. F5002 ARIN NFIN 1950 2B IO4 C9							· · · · · · · · · · · · · · · · · · ·	
MP X Y Name Description Type Part Name Coord.								
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Measurement Point Overview for EURO

- OLG	101	V01 005:	\no. •	1 100 / 100	I			
G13	101	AE 0361 Aer 0361	NF Out	SC1 Y Out	ACABROON CO.		ļ	F531
Eld			+	SC1 A L Out	ALOutsc1		<u> </u>	8127
60	101	Ar 0561	NF Out	NO HA LOS	TOG_JUORA	}	}) 0107
60	104	1950 218 1950 218	GND V Out	SCS GND A	CMDA		<u> </u>	F5021
60	104	1950 48		SC2 Y Out	YCVBSOut_SC2		<u> </u>	61037
			GND	SCS GND A	GNDA		ļ	F5004
60 60	104	81 0391 8E 0391	NF Out	SC2 A L Out	ALOutSC2		<u> </u>	E2003
H14		A1S 0361	1uO ∃N	SC2 A R Out	AROut_SC2		<u> </u>	F5001
EH1	101		GND	SCI GND A	GNDA			F525
113	101	A3 0361 A0S 0361	NI A	SC1 Y IN	YCVBSIN_SC1			F534
E13	101	AS 0391	NE IN	SC1 A L IN	ALIn_SC1			6197
			NE IN	SC1 A R IN	rDS_niAA			7127
E14	101	47 096L	DC IN	SC1 GND A	GNDA			F513
H13	FOIA	1 5861	DC IN	IDIO OT	INESET_DIG			F8201
	rolA	01 1861	DC IN	OU OT	DH.			60187
F13	FOIA	6 1861	DC IN	00 OT				80187
EtH	FOIA	1985 2	DC IN	15 DIGI	YOR_O		ļ	F8205
H13	roiA	1982 4	DC IN	15IG oT	YQA_A		ļ	F8204
E1H	FOIA	1985 3	DC IN	To DIGI	ATAQ_Q		ļ	F8203
H13	FOIA	1982 2	DC IN	To DIGI	ATAQ_A			F8202
€13	FOIA	E 1861	GND	VGN to DC	VGNSTBY			F8102
<u> </u>	101	1953 6	DC Out	TNORT of W2 8	W28			90537
F13	FOIA	11 1861	DC Out	2 A 40 DC	8T22			P8110
D13	FOIA	1981 2	DC Out	12 V to DC	12STBY			F8101
E13	FOIA	3 1861	TUO DO	POR to DC	IAO9I			F8104
6∀	TOIA	3802	OI OII	IICS	PAGS			F811
6A	FOIA	3804	OI OII	IICS	SCL1		L	F810
E13	FOIA	8 1861	OI OII	IICI	2CF			70187
E13	FOIA	9 1861	OI OII	IICI	AGS			F8105
98	Sd	5351	DC Out	W28	WS8			9€66∃
018	UT	12 6077	DC Out	MS9	WSS			F303
7 1∃	rola	St 786t	DC Out	TotoM V &	MS			FFF111
DS	SOIA	311 6087	→ tuo ⊃a	Inverse Reset	feseAl			E905
D3	SOIA	7803 12	DC Out	OIA V3	SYBT2			006∃
SH	FOIA	71187	Count Out	Clock Adjust	INT Clock			E083
13	DAG	10 0061	еир	Ground Digital	GNDD			F0001
18	DAG	71 0061	NI Sd	3V3 Supply	3AD			₹100 ∃
ra	Sd	1932 7	СИD	Ground Analogue	GNDA			F3207
IG	Sd	1932 6	DC Gen	Controls PS	FLYB			F3206
Ia	Sd	1932 5	NI Sd	33 V Supply	YATSEE			F3205
LO_	Sq	1932 4	NI Sd	Supply GND	VGNSTBY			F3204
LO.	Sd	1932 3	NI Sd	δ Λ Supply	YBTSN3			F3203
l)	_Sd	1932 2	NI Sd	5 V Supply	ΛS			F3202
LO.	Sd	1932 1	NI Sd	12 V Supply	12V			F3201
C10	FOIA	FOIA	Condition	Fact. Mode	L_MODE		ļ	008∃
	9msN	Part	θάχΤ	Description	Mame	Х	X	ЧM
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			Signal	Signal	Signal		Scher	natics
MP	Х	Υ	Name	Description	Type	Part	Name	Coord.
F5101			ARCRI	A L Rear Cinch In	NF In	1958 1A	102	D2
F5103			ARCLI	A R Rear Cinch In	NF In	1958 2A	102	E2
F5202			RCVBSIn	V Rear Cinch In	V in	1959 2A	102	C2
F5503			RSVHSYIn	Y Rear SVHS In	V In	1955 3B	102	B2
F5504			RSVHSCIn	C Rear SVHS in	Sin In	1955 4B	102	B2.
F338			RSVHSYOut	Y Rear SVHS Out	V Out	1955 3A	103	A9
F337			RSVHSCOut	C Rear SVHS Out	Sin Out	1955 4A	IO3	A9
F6001			DVAR	A R from DIGI	Sin In	1960 1	AP	D1
F6002			GNDA	GNDA	GND	1960 2	AP	D1
F6004			DVAL	A L from DIGI	Sin In	1960 4	AP	D1
F700			IF	IF Out	DC Out	1705 11	TU	СЗ
F701			IF In	IF In	Sin In	1705 11	ΤU	СЗ
F702			GNDFV	GND FV	GND	1705 12	TU	C2
F703			GNDFV	GND FV	GND	1700 3	TU	В6
F704			40.4	40.4 Trap	Sin Out	1700 1	ΤU	B5
F705			AGC	AGC	DC Out	3701	TU	A4
F812			SYNC	SYNC from Sepa.	Freq Out	7803 33	AIO1	F6
F4202			DIG OUT L	Digital Out Low	GND	1954 2	DIGI	B4
F4203			DIG OUT H	Digital Out High	Sin Out	1945 3	DIGI	A4
F4204			OPT OUT	Optical Out	DC Out	1943 1	DIGI	D3
F806			FAN OUT	FAN Out	DC Out	1984 1	FACO	C5
F807			FAN IN	FAN In	DC In	1985 1	FACO	F1
F8206			ION	ION_FAN	DC Out	1982 6	AIO1	H13
F8208			BE_FAN	BE_FAN	DC Out	1982 8	AIO1	l13
F8209			FB	FBIN SC2	DC Out	1982 9	AIO1	113
F8210			GNDD	GNDD	GNDD	1982 10	AlO1	113

Remark: Indicator * means more than one signal type

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MD	v	,	Signal	Signal	Signal		Scher	
MP	Х	Y	Name	Description	Type	Part		Coord.
F800 F3201		+	F_MODE 12V	Fact. Mode 12 V Supply	Condition PS IN	AIO1 1932 1	AIO1 PS	C10
F3202			5V	5 V Supply	PSIN	1932 1	PS	C1
F3203			5NSTBY	5 V Supply	PS IN	1932 2	PS	C1
F3204			VGNSTBY	Supply GND	PSIN	1932 3	PS	C1
F3205	•		33STBY	33 V Supply	PS IN	1932 5	PS	D1
F3206			FLYB	Controls PS	DC Gen	1932 6	PS	D1
F3207			GNDA	Ground Analogue	GND	1932 7	PS	D1
F0017			3VD	3V3 Supply	PS IN	1900 17	DAC	B1
F0001		<u> </u>	GNDD	Ground Digital	GND	1900 01	DAC	E1
F803			INT Clock	Clock Adjust	Count Out	7811 7	AIQ1	H5
F900		<u> </u>	5STBY2	5V AIO	DC Out	7803 12	AlO2	D3
F902			IReset	inverse Reset	DC Out *	7803 115	AIO2	D2
F8111			5M	5 V Motor	DC Out	1987 12	AIO1	F14
F303			5SW	5SW	DC Out	7703 21	TU	B10
F9336			8SW	8SW	DC Out	2321	PS	В6
F8105			SDA	IIC1	IIC IO	1981 6	AIQ1	E13
F8107			SCL	IIC1	IIC IO	1981 8	AlO1	E13
F810			SCL1	IIC2	IIC IO	3804	AIO1	A9
F811			SDA1	IIC2	IIC IO	3805	AlO1	A9
F8104			IPOR1	IPOR to DC	DC OUT	1981 5	AIQ1	E13
F8101			12STBY	12 V to DC	DC Out	1981 2	AIQ1	D13
F8110			5STB	5 V to DC	DC Out	1981 11	AIO1	F13
F5306			8SW	8 SW to FRONT	DC Out	1953 6	101	11
F8102			VGNSTBY	VGN to DC	GND	1981 3	AIO1	E13
F8202			A_DATA	To DIGI	DC_In	1982 2	AIO1	H13
F8203			D_DATA	To DIGI	DC_In	1982 3	AIO1	H13
F8204			A_RDY	To DIGI	DC_In	1982 4	AIO1	H13
F8205			D_RDY	To DIGI	DC_In	1982 5	AIO1	H13
F8108			INT	TO DC	DC_In	1981 9	AIO1	F13
F8109			RC	TO DC	DC_In	1981 10	AlO1	F13
F8201		ļ	IRESET_DIG	TO DIGI	DC_In	1982 1	AIO1	H13
F5103			ARIn_2	ARIN2	NF IN	1958 3A	IO3	E13
F5101			ALIn_2	ALIN2	NF IN	1958 1A	IO3	E14
F5906		ļ	GNDV	GND V	GND	1957 6A	101	H12
F5806			GNDV	GND V	GND	1956 6A	101	18
F510			ARout_1	A R Out 1	NF Out	1959 5B	101	E13
F509			ALout_1	A L Out 1	NF Out	1959 4B	101	D13
F5201		<u> </u>	RCVBSOut2	SC1 Y Out	V Out	1997 1B	103	A8
F5105		ļ	ARIn_1	ARIN1	NF IN	1959 1A	102	E2
F5104			ALIn_1	ALIN1	NF IN	1959 4A	102	E2
F5202		-	RCVBSin	YIN	Sin IN	1997 2A	102	C2
F5905		ļ	Y_OUT	Y Out	Sin Out*	1957 5A	101	112
F5801		 	U_IN	UIN	Sin In*	1956 1B	101	110
F5805			Y_IN	Y IN	Sin In	1956 5A	101	19
F5802			V_IN	VIN	Sin In	1956 2B	101	110

Measurement Point Overview for NAFTA

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l l			Signal	Signal	Signal		Scher	natics
MP	X	Y	Name	Description	Туре	Part		Coord.
F5401			A_V	A_V to DIGI	Sin Out	1954 01	101	13
F5402			GNDV	GNDV to DIGI	GND	1954 02	101	14
F5403			A_U	A_U to DIGI	Sin Out	1954 03	101	14
F5405			A_Y	A_Y to DIGI	V Out	1954 05	101	14
F5407			A_C	A_C to DIGI	Sin Out	1954 07	101	14
F5409			A_YCVBS	AYCVBS to DIGI	V Out	1954 09	101	14
F5412			D_CVBS	D_CVBS f. DIGI	V In	1954 12	101	15
F5414			D_Y	D_Y f. DIGI	V In	1954 14	101	15
F5416			D_C	D_C f. DIGI	Sin In	1954 16	101	15
F5418		<u> </u>	D_R	D_T f. DIGI	Sin In	1954 18	101	16
F5420			D_G	D_G f. DIGI	Sin In	1954 20	101	16
F5422			D_B	D_B f. DIGI	Sin In	1954 22	101	16
F5301			AFCRI	A R from FC	NF In	1953 1	101	1
F5303			AFCLI	A L from FC	NF In	1953 3	101	11
F5304		1	CVBSFIN	CVBS from FC	V In	1953 4	101	11
F5307			CFIN	C from FC	Sin In	1953 7	101	12
F5309			YFIN	Y from FC	V In	1953 9	101	12
F012			DAINOPT	A D Opt to DIGI		1900 20	DAC	A1
F013			DAINCOAX	A D Coax to DIGI		1900 21	DAC	A1
F014			DAOUT	A D from DIGI		1900 20	DAC	A1
F0002			A_BCLK	BCLK from DIGI	CLK In	1900 2	DAC	E2
F0003			A_WCLK	WCLK from DIGI	CLK in	1900 3	DAC	D2
F0005			A DAT	A Data to DIGI	Data Out	1900 5	DAC	D2
F0007			A_PCMCLK	PCMCLK from DIGI	CLK In	1900 7	DAC	D2
F0009			D BCLK	BCLK from DIGI	CLK In	1900 9	DAC	D2
F0011			D WCLK	WCLK from DIGI	CLK In	1900 11	DAC	D2
F0012		<u> </u>	D DATA0	A Data from DIGI	Data In	1900 12	DAC	C2
F0014	-	1	D_PCMCLK	PCMCLK from DIGI	CLK In	1900 14	DAC	C2
F0016			D_KILL	A Kill from DIGI	DC In	1900 16	DAC	C2
F010	-,		ARDAC	A R from DAC	NF Out	7002 1	DAC	C9
F011			ALDAC	A L from DAC	NF Out	7002 7	DAC	E9
F513			ALOut 2	A L Rear Out 2	NF Out	1958 4B	101	B13
F512		l —	AROut 2	A R Rear Out 2	NF Out	1958 5B	101	C13
F5205		 	RCVBSOut1	V Rear Cinch Out1	V Out	1997 5C	103	A8
F5503			RSVHSYIn	Y Rear SVHS In	V In	1955 3B	103	B2
F5504			RSVHSCIn	C Rear SVHS In	Sin In	1955 4B	102	B2
F338		 	RSVHSYOut	Y Rear SVHS Out	V Out	1955 3A	103	A9
F337			RSVHSCOut	C Rear SVHS Out	Sin Out	1955 3A	103	A9
F6001			DVAR	A R from DIGI	Sin In	1960 1	AP	D1
F6002			GNDA	GNDA	GND		AP	-
F6004		-	DVAL	A L from DIGI	Sin In	1960 2		D1
F700			IF UVAL	IF Out		1960 4	AP	D1
F701			IF In	IF Out	DC Out	1705 11	TU	C3
F701	**				Sin In	1705 11	TU	C3
F702			GNDFV	GND FV	GND	1705 12	TU	C2
F705			GNDFV	GND FV	GND	1700 3	Z	В6
F812	ALV L		AGC SYNC	AGC	DC Out	3701	TU	A4
F330		\'		SYNC from Sopa.	Freq Out	7003 33	AIO1	F6
r330		L	RC IN	Remote Control In	DC Out	1993 2	103	E2

			Signal	Signal	Signal		Scher	natics
MP	Х	Υ	Name	Description	Туре	Part	Name	Coord.
F4202			DIG OUT L	Digital Out Low	GND	1954 2	DIGI	B4
F4203			DIG OUT H	Digital Out High	Sin Out	1945 3	DIGI	A4
F4204			OPT OUT	Optical Out	DC Out	1943 1	DIGI	D3
F806			FAN OUT	FAN Out	DC Out	1984 1	FACO	C5
F807			FAN IN	FAN In	DC In	1985	FACO	F1
F8206			ION	ION_FAN	DC Out	1982 6	AlO1	H13
F8208			BE_FAN	BE_FAN	DC Out	1982 8	AIO1	113
F8209			FB	FBIN SC2	DC Out	1982 9	AIO1	113
F8210			GNDD	GNDD	GNDD	1982 10	AIO1	113

Remark: Indicator * means more than one signal type Power Part Check

RESET AND CLOCK CHECK ANALOG BOARD

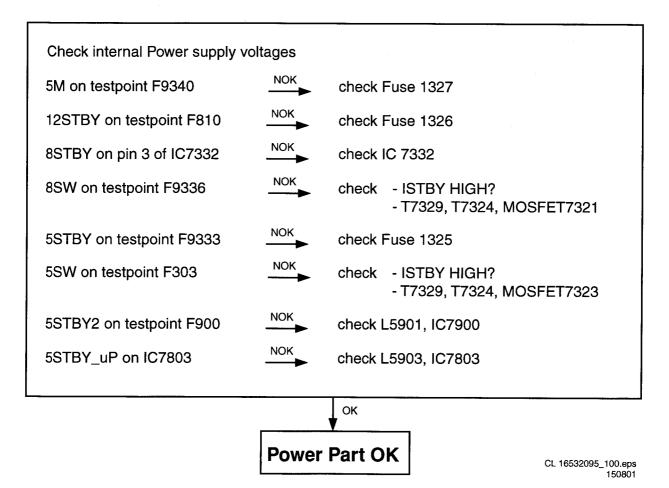


Figure 5-34

DSW CHECK ANALOGUE BOARD

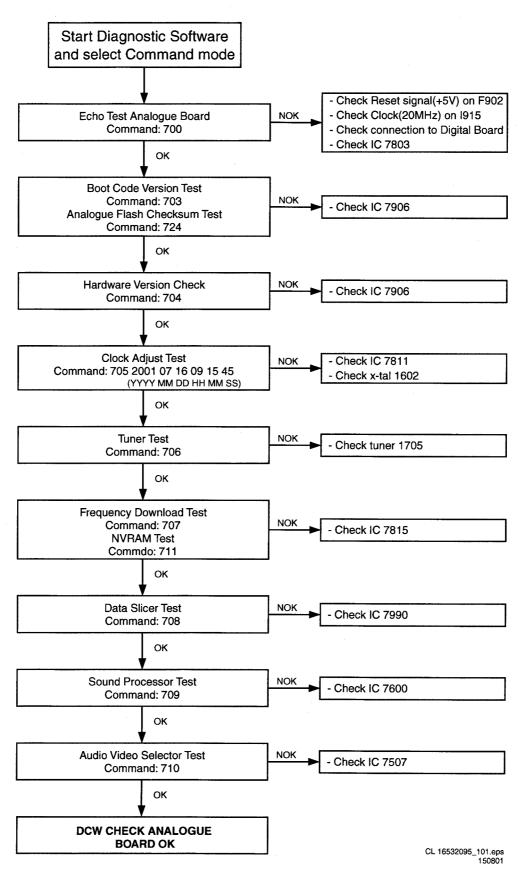


Figure 5-35

Routing Audio and Video

Route Video Nucleus Number: 712 Description

This nucleus routes the video signals on the analogue board to the destination determined by the input parameters The paths that are available for video routing and their description(Europe version)

PATH ID	DESCRIPTION
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
03	Input signal is from FRONT S-VIDEO(Y/C) and will be routed to the digital board.
04	Input signal is from REAR S-VIDEO(Y/C) and will be routed to the digital board.
05	Input signal is CVBS from SCART1 and will be routed to the digital board.
06	Input signal is CVBS from SCART2 and will be routed to the digital board.
07	No routing.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to SCART1.
09	Input signal is VIDEO(CVBS) from SCART1 and will be routed to SCART2.
10	Input signal is VIDEO(CVBS) from SCART2 and will be routed to SCART1.
11	No routing.
12	Input signal is from REAR VIDEO(CVBS) IN and will be routed to SCART1 and SCART2.
13	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to SCART1.
14	Input signals VIDEO(CVBS and Y/C) from SCART 1 will be routed to SCART2.
15	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to SCART2.
16	Input signal is from FRONT S-VIDEO(Y/C) IN and will be routed to SCART2.
17	No routing
18	No routing
19	Input signals VIDEO(RGB and FAST BLANKING) from SCART2 will be routed to the corresponding pins of SCART1.

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The paths that are available for video routing and their description (Nafta region)

Path ID	Description
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to the digital board.
02	Input signal is from REAR VIDEO(CVBS) IN and will be routed to the digital board.
03	Input signal is from FRONT S-VIDEO(Y/C) IN and the signal received will be routed to the digital board.
04	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to the digital board.
05	Input signal is from YUV IN and will be routed to the digital board.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) from ANTENNA IN and will be routed to VIDEO(CVBS) OUT and .
09	Input signal is from YUV IN and will be routed to YUV OUT.
10	No routing.
11	No routing.
12	Input signal is from REAR VIDEO(CVBS) IN and will be routed to REAR VIDEO(CVBS) OUT.
13	Input signal is from FRONT VIDEO(CVBS) IN and will be routed to REAR VIDEO(CVBS) OUT.
14	Input signal is from REAR S-VIDEO(Y/C) IN and will be routed to REAR S-VIDEO(Y/C) OUT.
15	Input signal is from FRONT S-VIDEO(Y/C) IN and will be routed to REAR S-VIDEO(Y/C) OUT.

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Route Audio Nucleus Number: 713 Description

This nucleus routes the audio on the analogue board to the destination determined by the input parameters

The paths that are available for audio routing and their description (Europe version)

Path ID	Description				
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.				
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.				
02	Input signal is from REAR AUDIO IN and will be routed to the digital board.				
03	Input signal is AUDIO from SCART1 and will be routed to the digital board.				
04	Input signal is AUDIO from SCART2 and will be routed to the digital board.				
05	No routing.				
06	No routing.				
07	No routing.				
08	Input signal is VIDEO(CVBS) and AUDIO from ANTENNA IN and will be routed to SCART1.				
09	Input signal is VIDEO(CVBS) and AUDIO from SCART1 and will be routed to SCART2.				
10	Input signal is VIDEO(CVBS) and AUDIO from SCART2 and will be routed to SCART1.				
11	Input signal is AUDIO from dvio board and will be routed to SCART1.				
12	No routing.				
13	No routing.				
14	No routing.				
15	No routing.				
16	No routing.				
17	Input signal is from REAR AUDIO IN and will be routed to SCART1.				
18	Input signal is from FRONT AUDIO IN and will be routed to SCART1.				

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The paths that are available for audio routing and their description (Nafta region)

Path ID	Description
00	Input signal is VIDEO(CVBS) from digital board and will be re-routed back to the digital board.
01	Input signal is from FRONT AUDIO IN and will be routed to the digital board.
02	Input signal is from REAR AUDIO IN 1 and will be routed to the digital board.
03	Input signal is from REAR AUDIO IN 2 and will be routed to the digital board.
04	No routing.
05	No routing.
06	No routing.
07	No routing.
08	Input signal is VIDEO(CVBS) and AUDIO from ANTENNA IN and will be routed to VIDEO(CVBS) OUT and REAR CINCH OUT 2.
09	No routing.
10	Input signal is from REAR AUDIO CINCH IN 1 and will be routed to REAR AUDIO CINCH OUT 2.
11	Input signal is from FRONT AUDIO CINCH IN and will be routed to REAR AUDIO CINCH OUT 2.
12	No routing.
13	No routing.
14	No routing.
15	No routing.
16	Input signal is AUDIO from dvio board and will be routed to AUDIO CINCH OUT 2.

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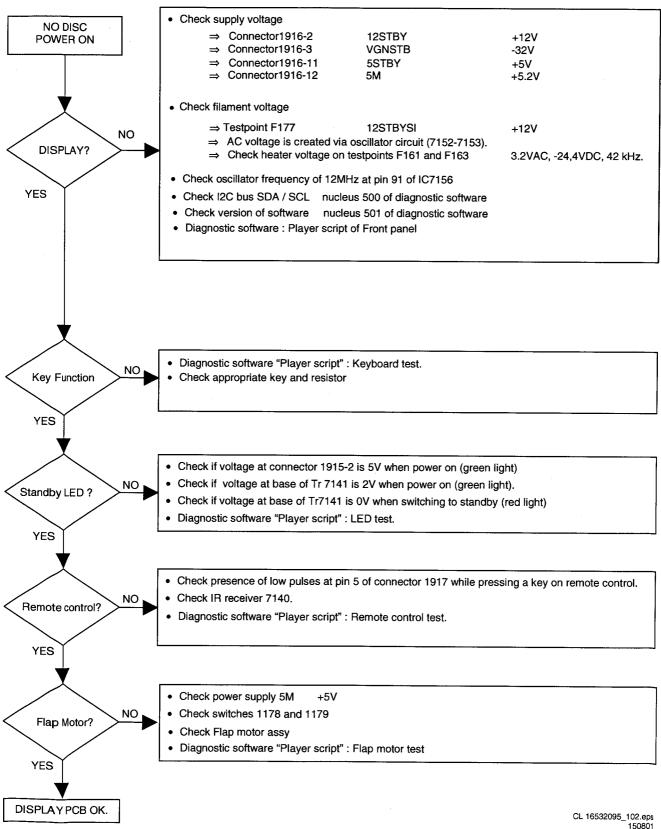
EXAMPLE DD:> 713 00

71300: Audio routing on the Analogue Board OK.

Test OK @

Display Board

TROUBLESHOOTING DISPLAY BOARD



Power Part Check

POWER PART CHECK DVIO

USE DVIO BOARD CIRCUIT DIAGRAMS 1 2, 3, 4 AND 5 AND DVIO TOP VIEW TESTPOINTS

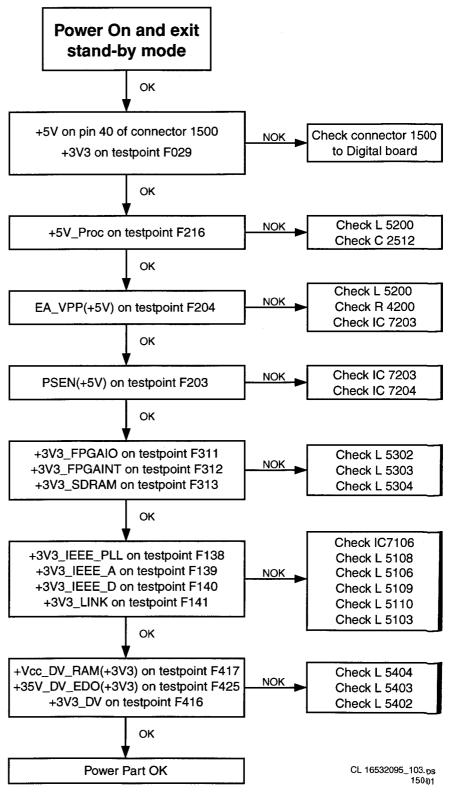


Figure 5-37

Reset and Clock Check

RESET & CLOCK CHECK DVIO

USE DVIO BOARD CIRCUIT DIAGRAMS 2, 3, 4 AND 5 AND DVIO TOP VIEW TESTPOINTS

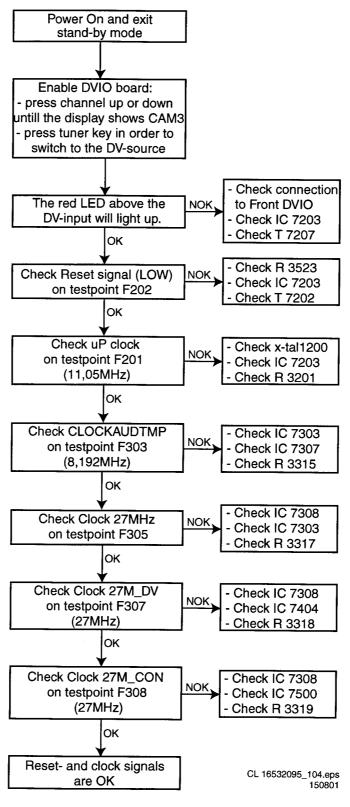


Figure 5-38

DSW DVIO TESTS

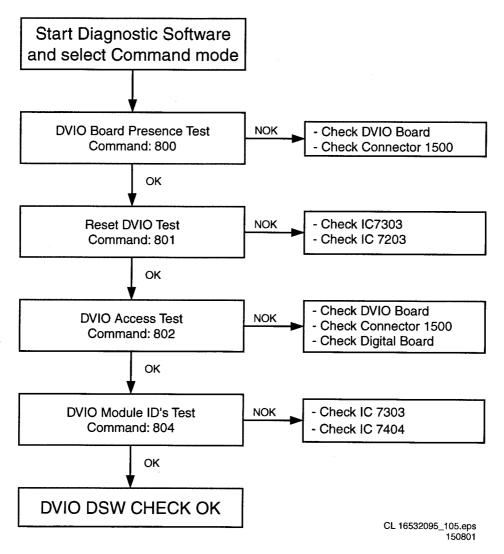


Figure 5-39

Functional Test

FUNCTIONAL TEST VIDEO PICTURE DVIO BOARD

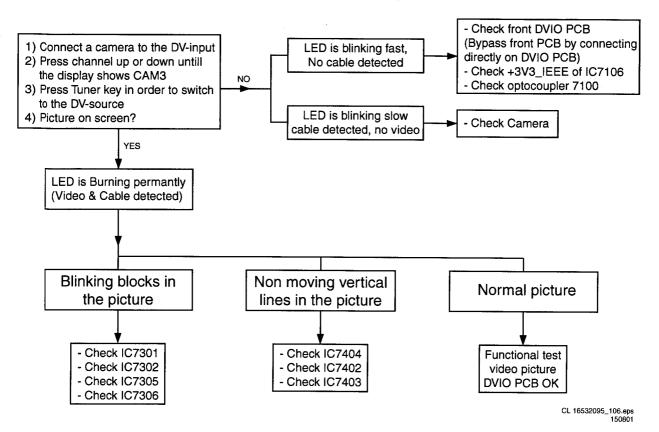
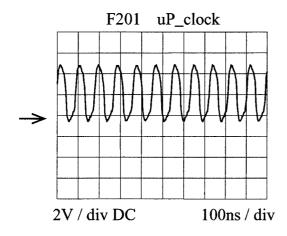
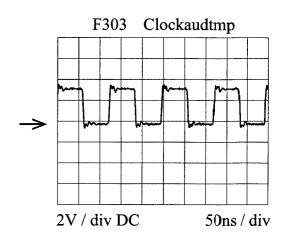


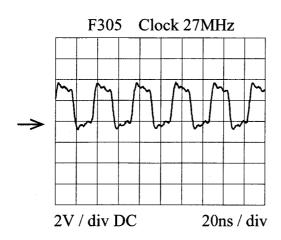
Figure 5-40

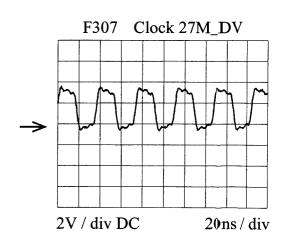
Waveforms

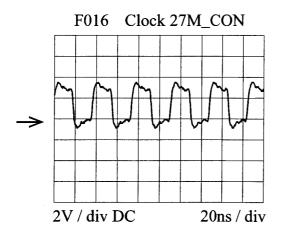
Waveforms DVIO











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.6.7 Progressive Scan

Video Part Check

VIDEO PART CHECK PROGRESSIVE SCAN

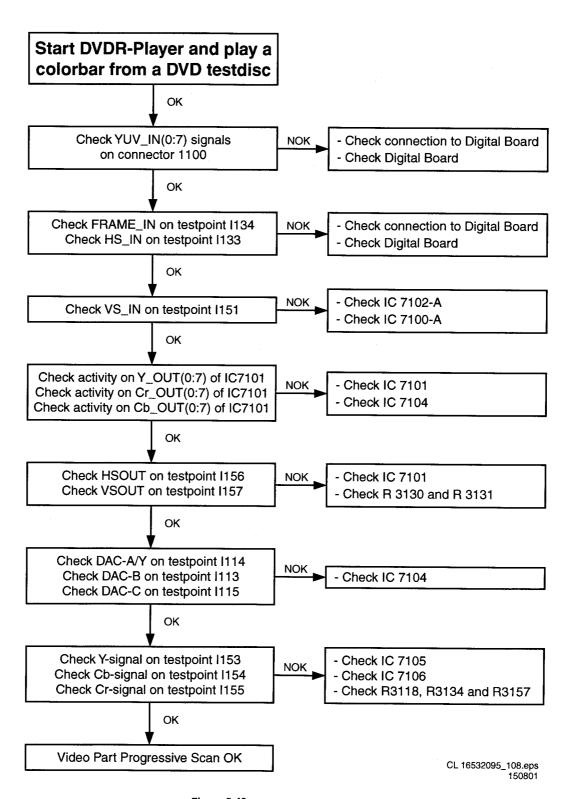
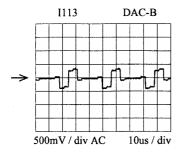
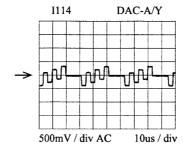


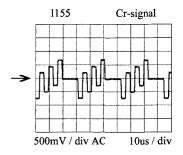
Figure 5-42

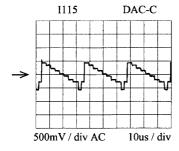
Waveforms

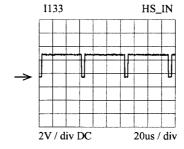
Waveforms Progressive Scan

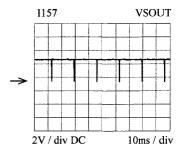


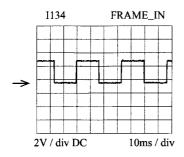


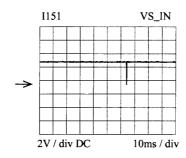


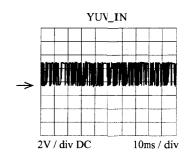


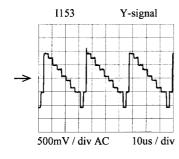


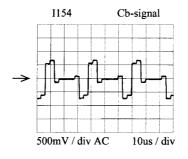


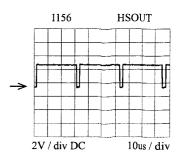


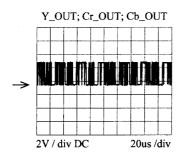












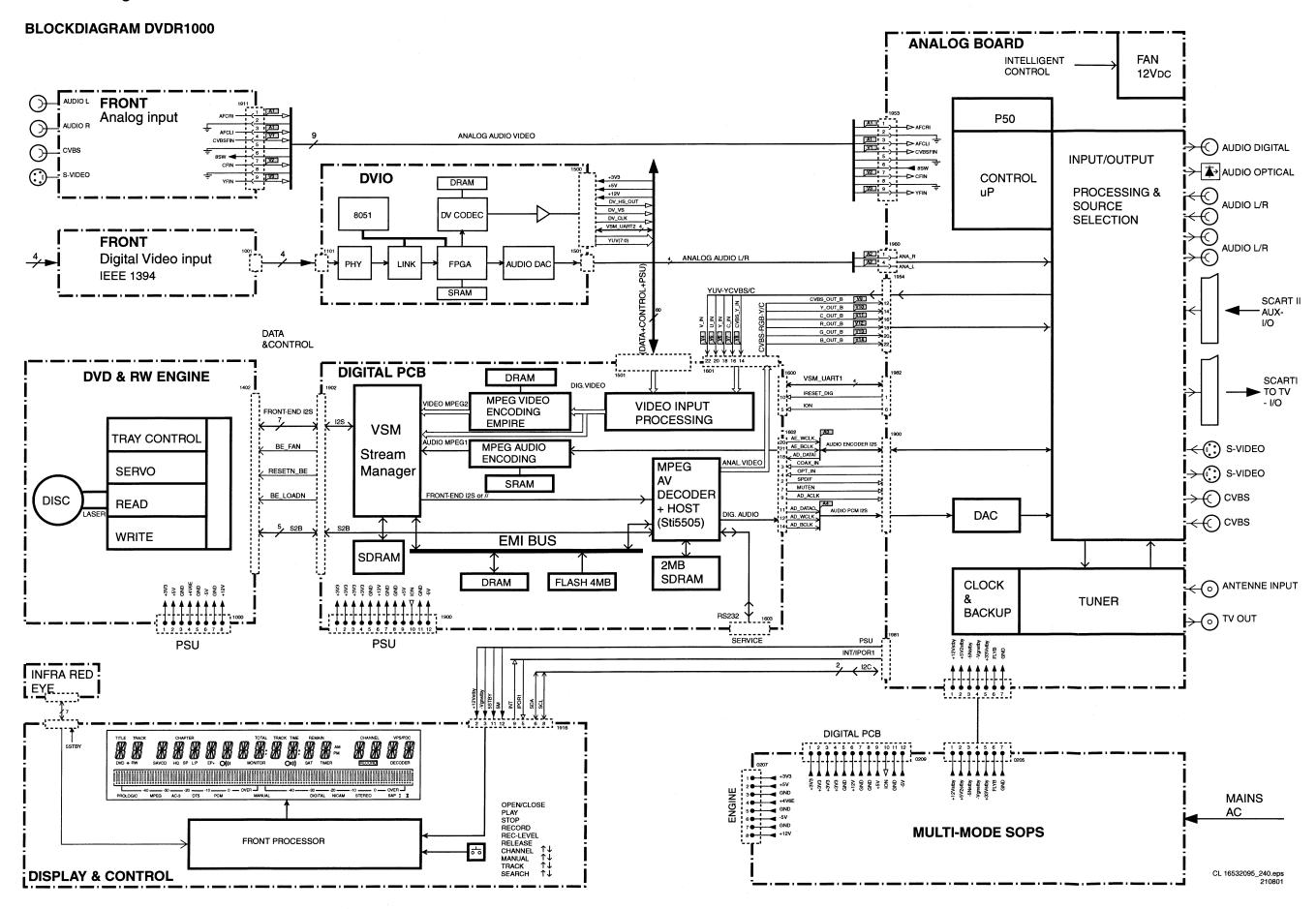
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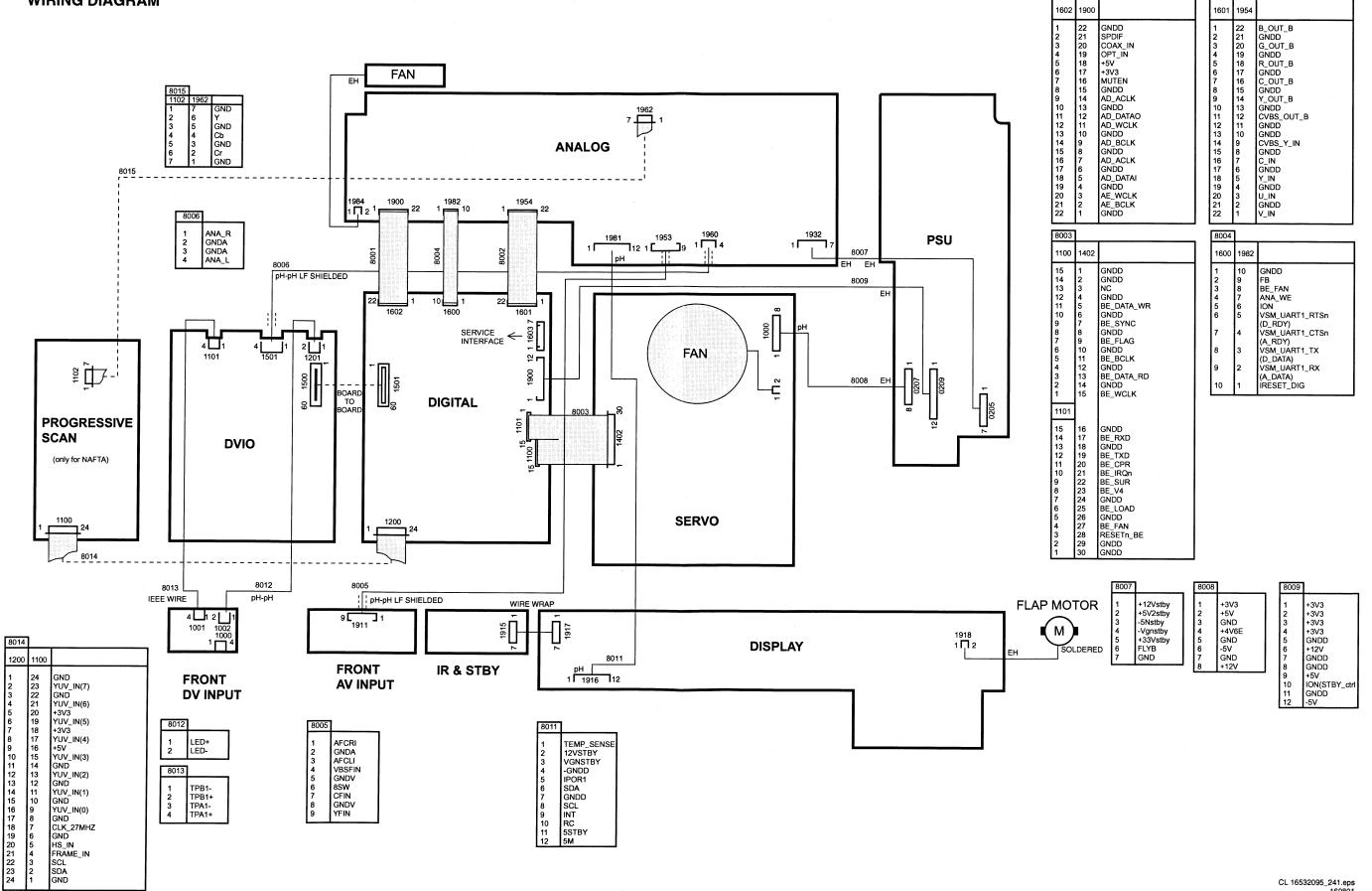
6. Block and Wiring Diagram.

Blockdiagram DVDR1000

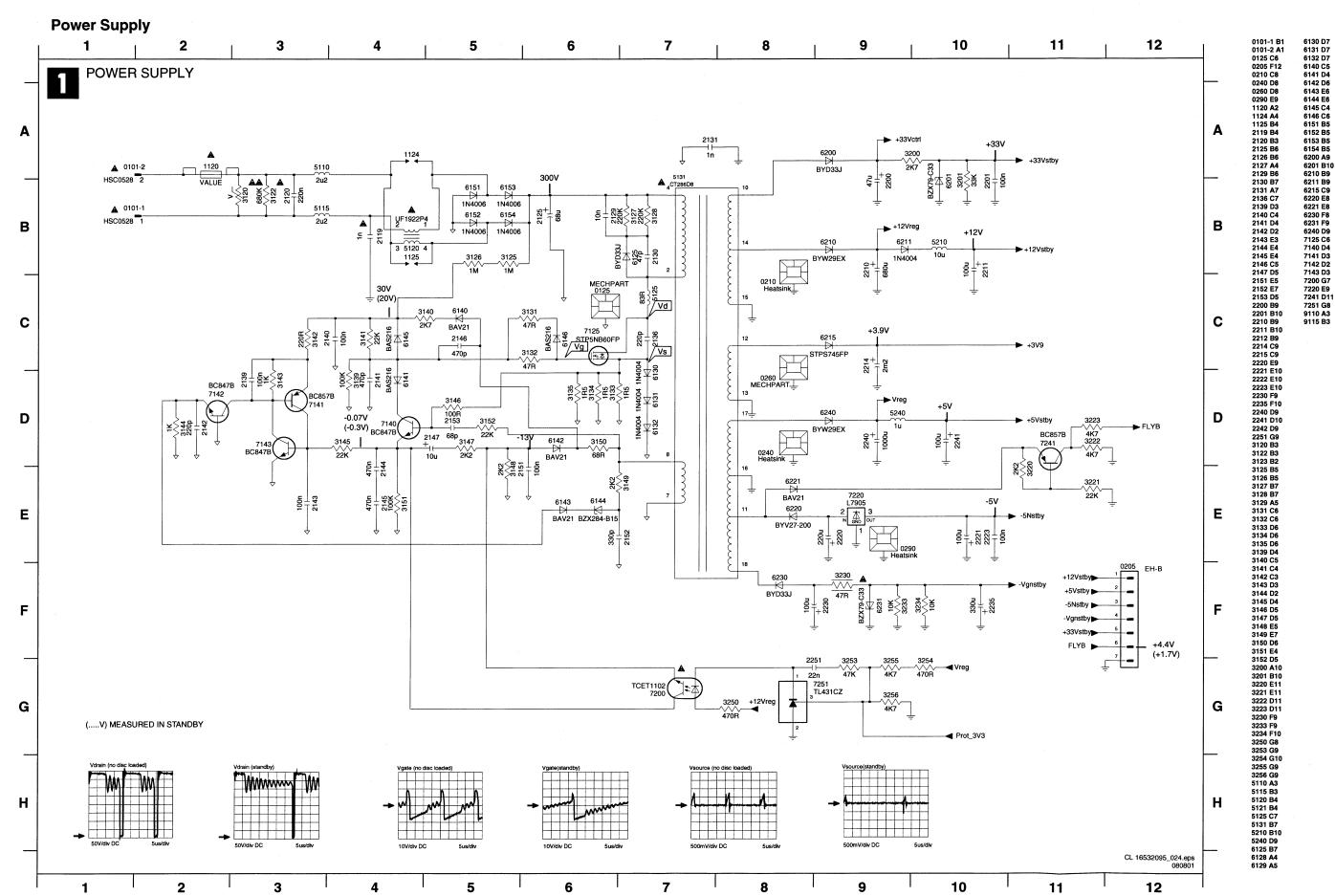


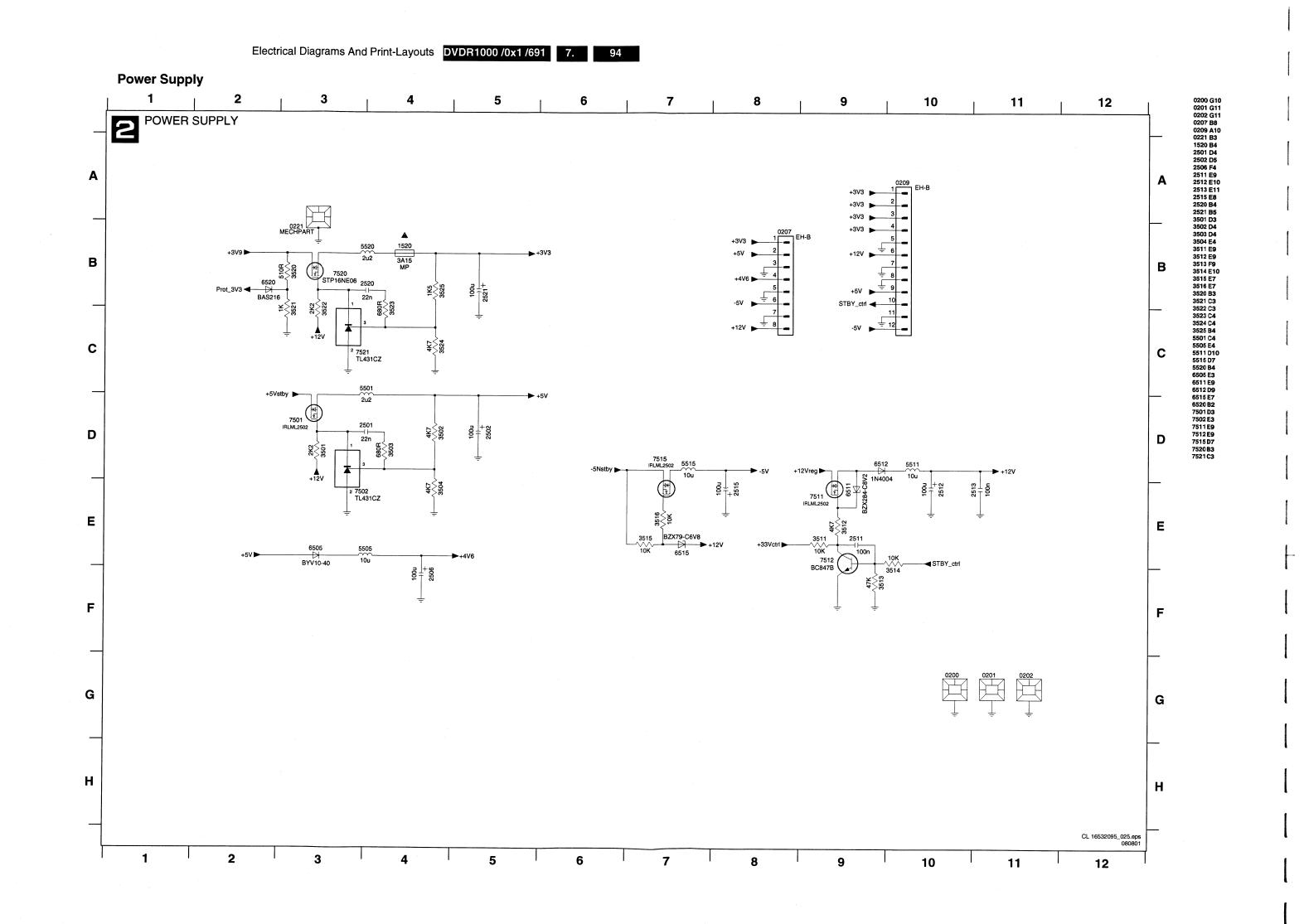
Wiring Diagram

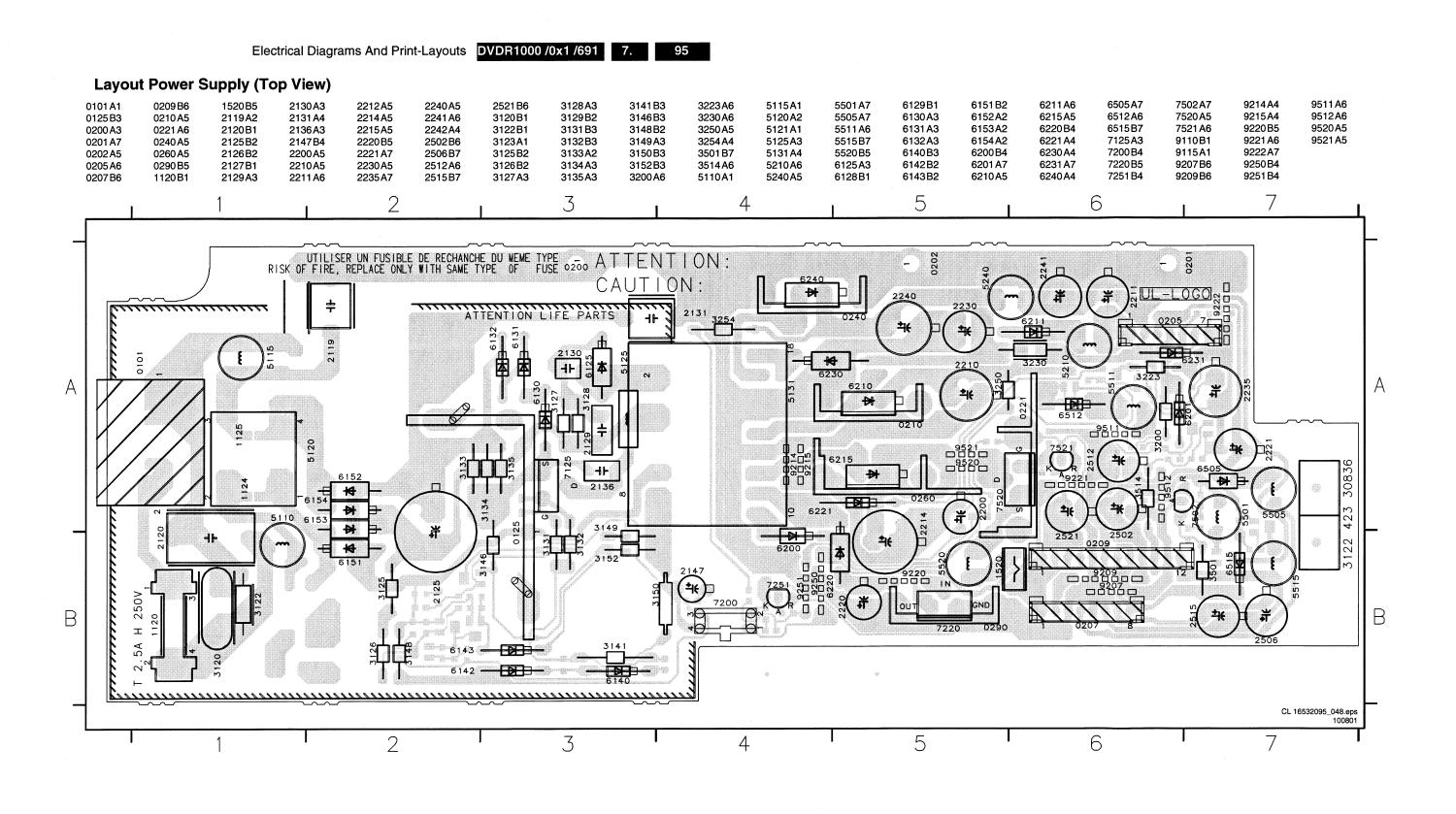
WIRING DIAGRAM

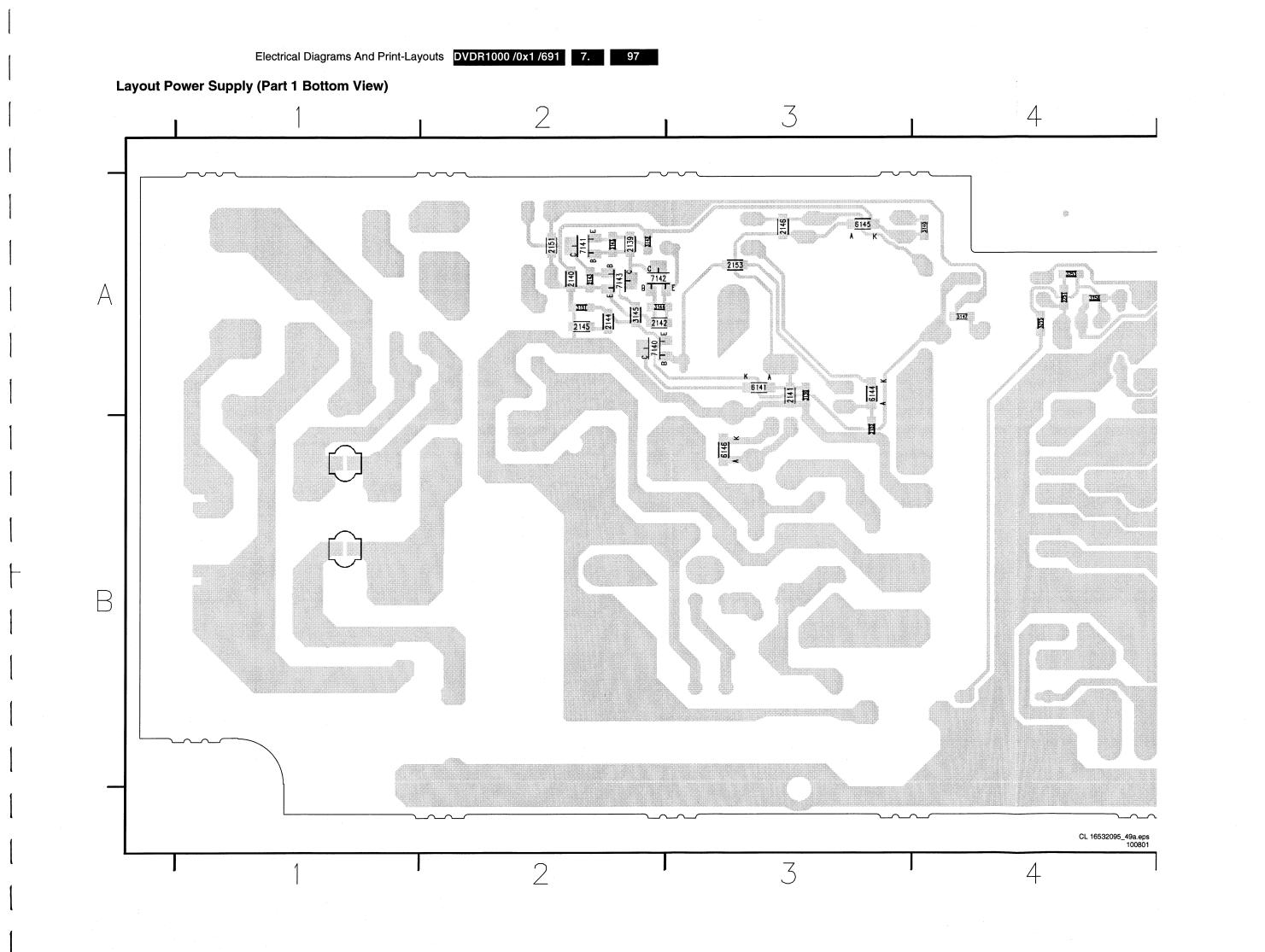


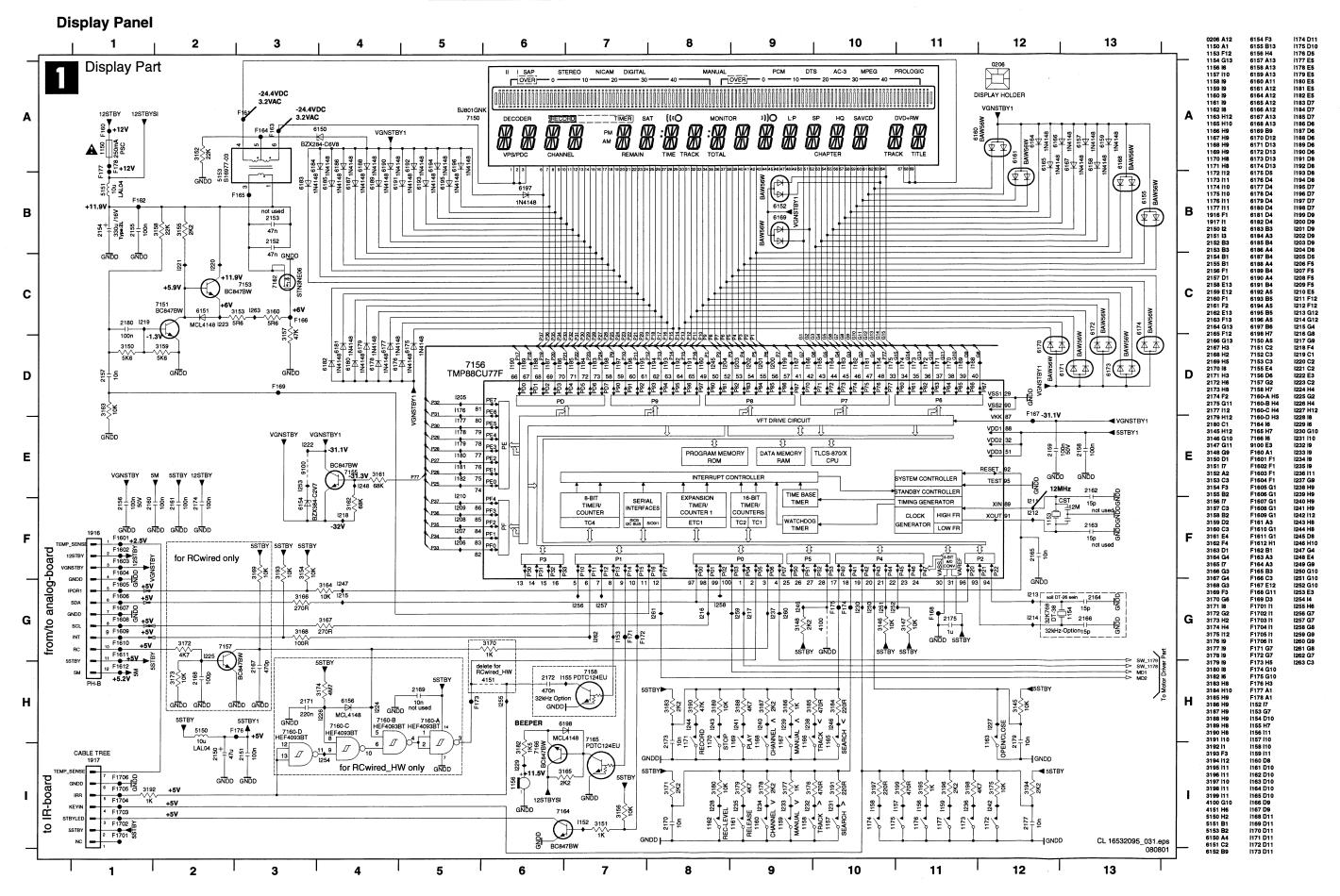
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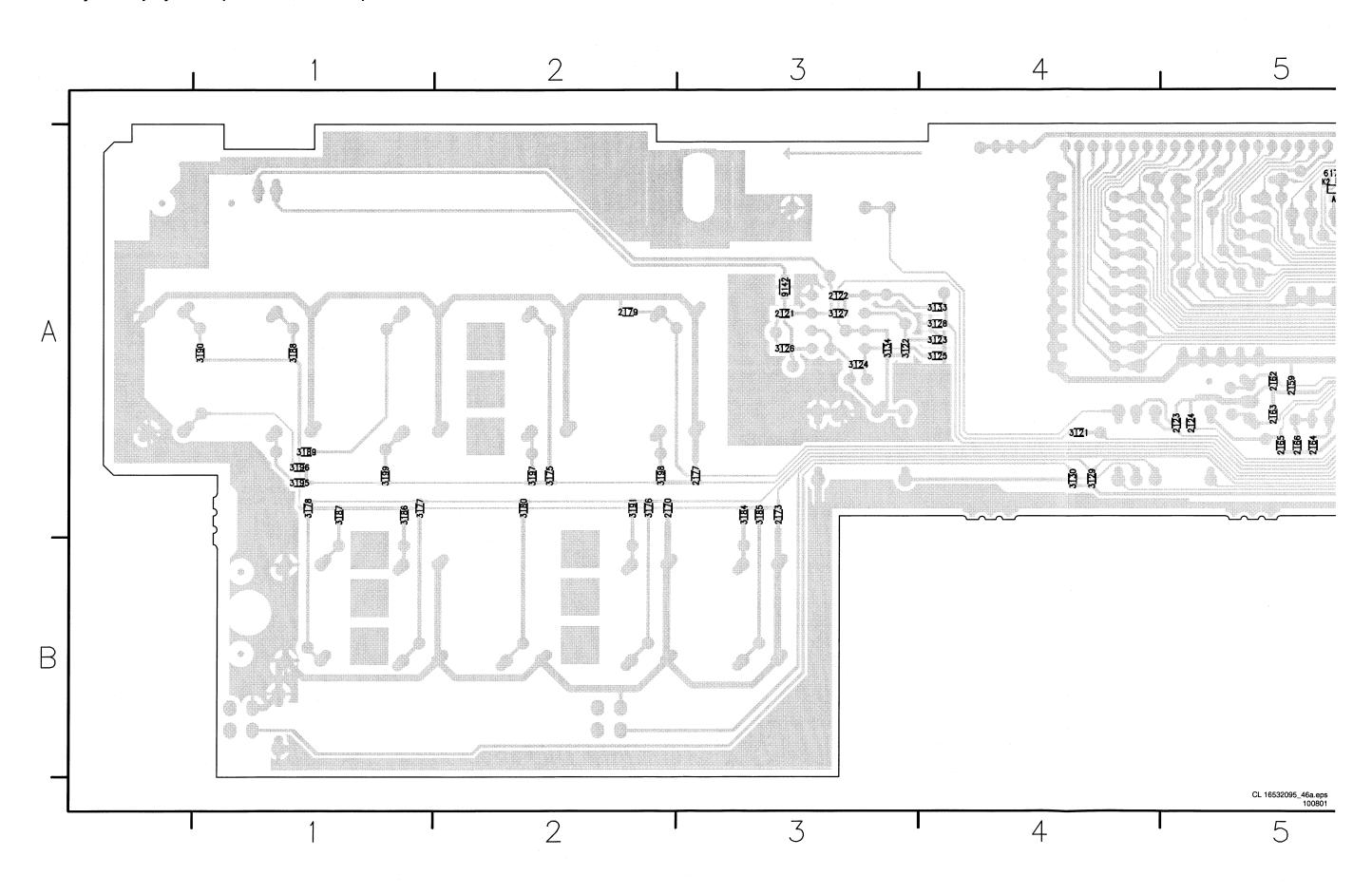




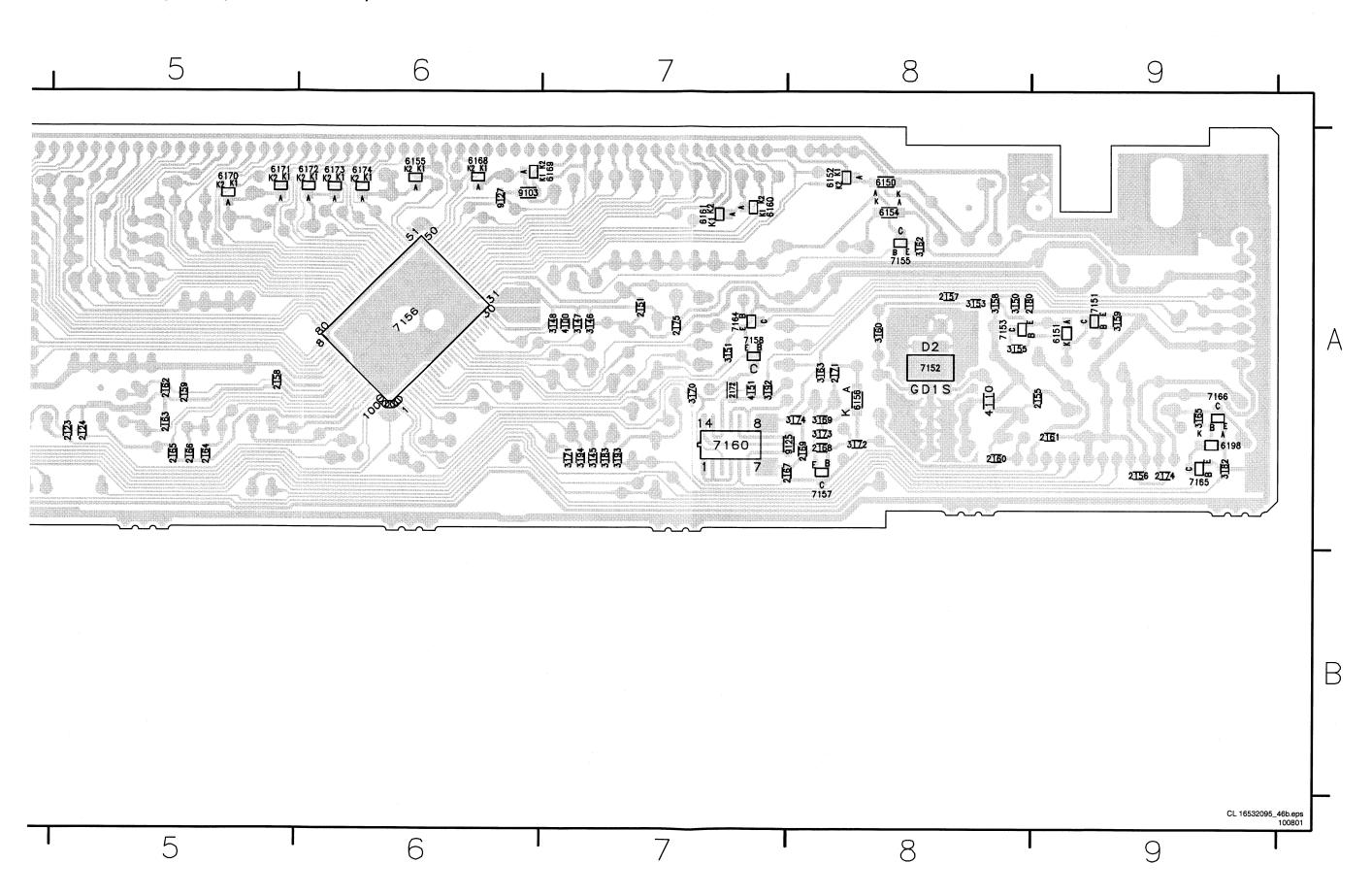


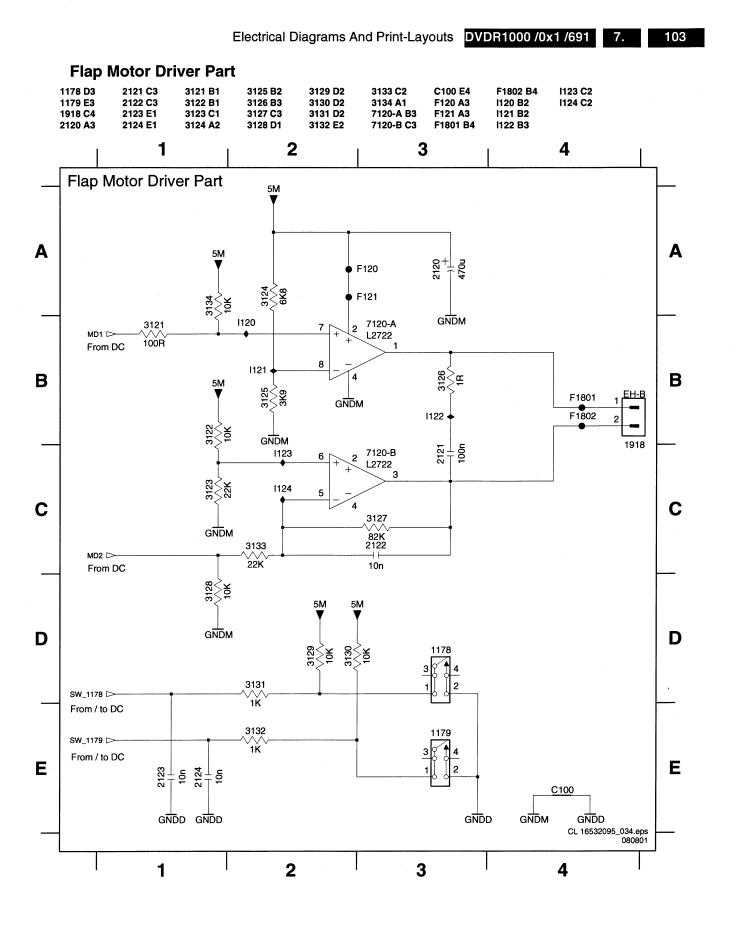


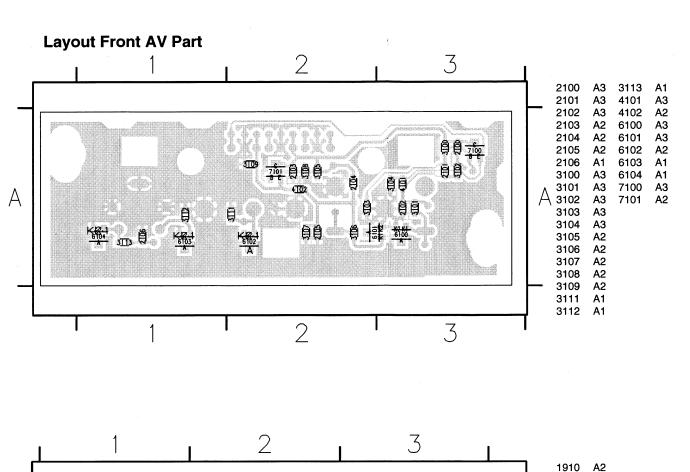
Layout Display Panel (Part 1 Bottom View)



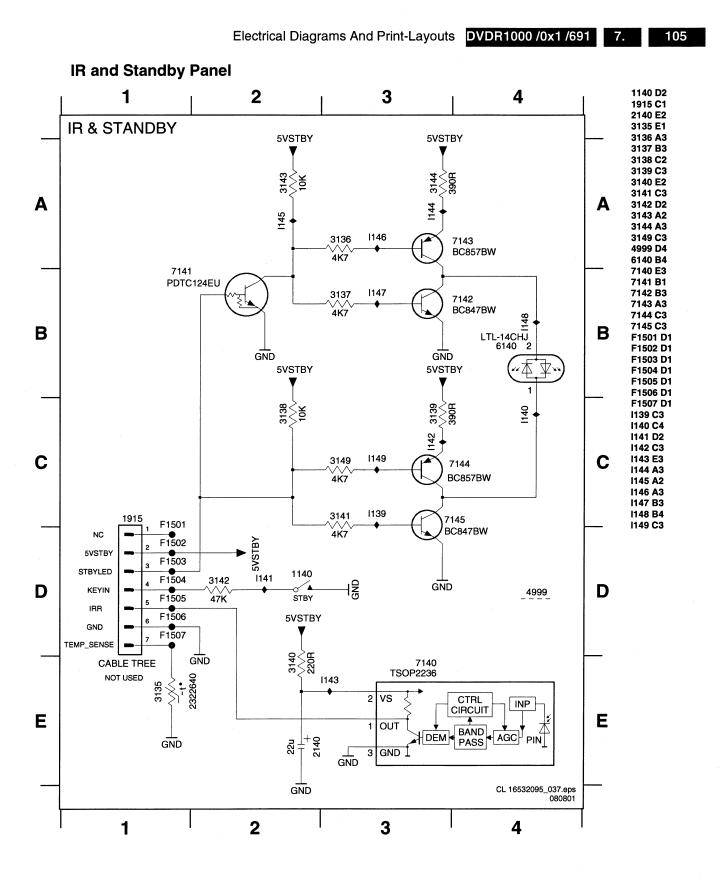
Layout Display Panel (Part 2 Bottom View)

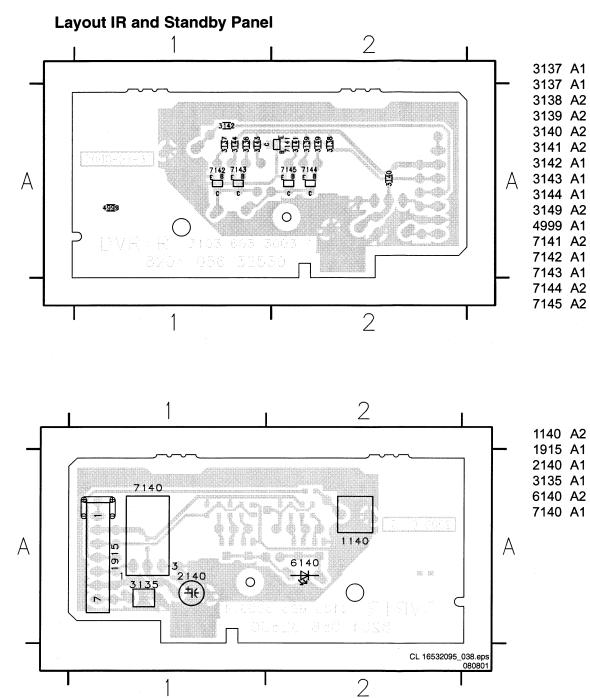






1911 A2





Electrical Diagrams And Print-Layouts DVDR1000 /0x1 /691

1950-1 E14
1950-2 A14
1951-2 A14
1951-2 A14
1952-2 C14
1952-2 C14
1953-1 I1
1954 I3
2500 A5
2501 A6
2502 A8
2502 A8
2503 A8
2503 A8
2504 B13
2506 C5
2507 C1
2501 C11
2511 E2
2513 E19
2514 E9
2515 E12
2514 E9
2514 E1
2514 E1
2524 F8
2525 F7
2526 F7
2526 F6
2537 F1
2528 F8
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21A Ε F GNDV G 534 1535 GNDV F531 GNDV 2530 L001-SC2 ARIN_SC2 GNDV 2531 151 1510 Н 2535 → (10u 16 F5416 ADN ADN A 6754 B 184 B 2000 B 184 B 2000 B 184 B 2000 <u>GND</u>V GNDV A_G P from YUV_CON A_B P from YUV_CON from YUV_CON 3554 75R C570 CTYC_H D
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KILL_DC D
from IO4
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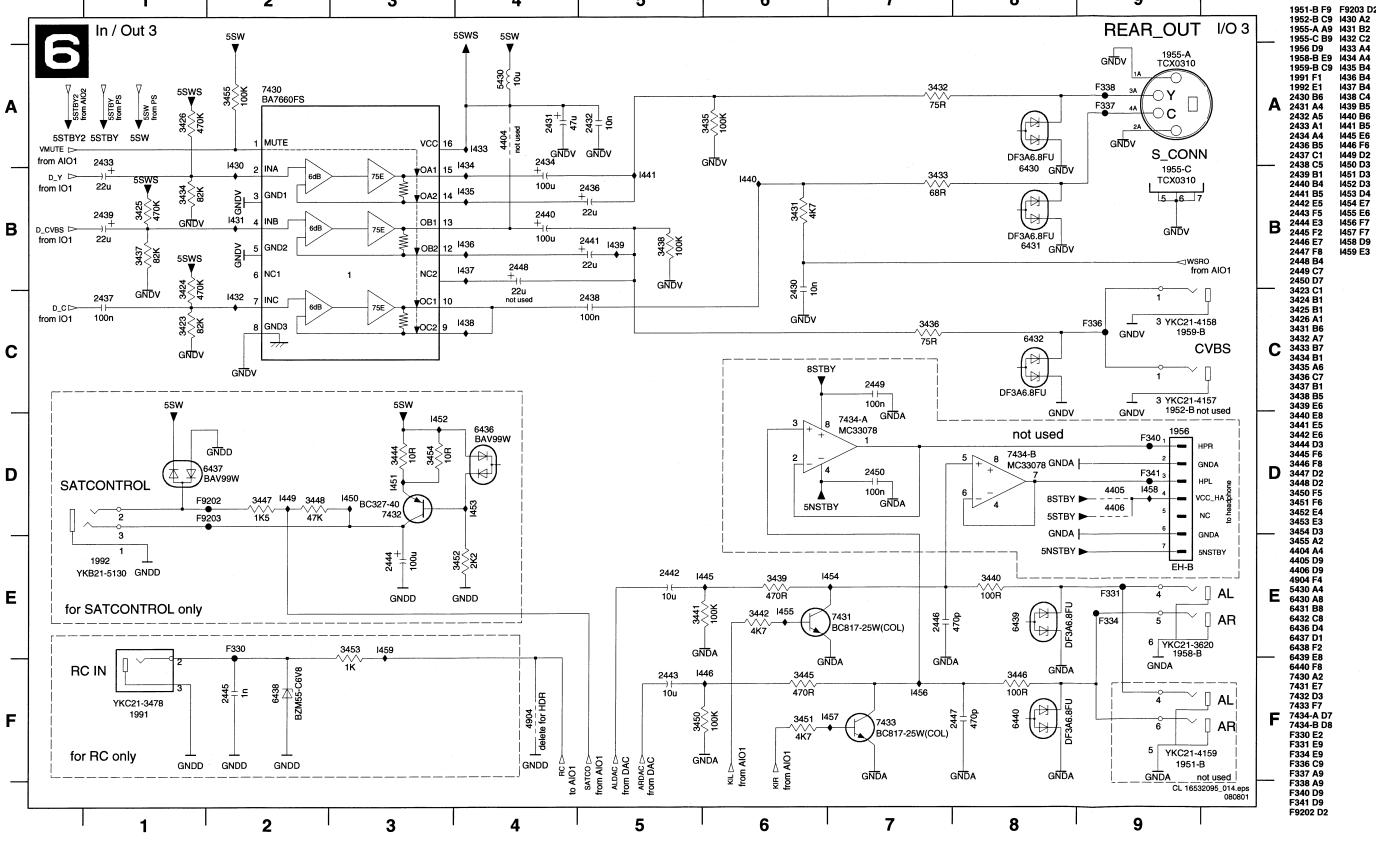
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GNDV 100n

3482 1477

GNDV

8464 S BZM55-C6V8 3481 758 6463

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GNDV GNDV GNDV

3457 390R not used 3480 75R

BC847BW

3485

1K

6

GNDV

GNDV

GNDA

GNDV

BC817-25W(COL)

BIN_SC2 to 101

GIN_SC2 .

8_SC2 to lO1

RCIN_SC2 .

FBIN_SC2 -

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GNDV

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6468 MCL4148 2469

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15B 16B

17B 18B

19B ___20B

21B

F5015

F5019 F5020

DF3A6.8FU 6466 99

1476 3484 75R

GNDV

8

F5021 GNDV

9

GNDV

GNDV

FBIN

GNDV

GNDV

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YCVBSOUT

6463 E7

6464 E7

6465 F7 6466 F9

6468 E1

7460 A7

7461 B7

7462 C2

7463 E3 7464 F6 7466 D1 F5001 C9

F5002 C9

F5003 C9

F5004 C9

F5006 C8 F5007 D9

F5008 D9 F5010 D9

F5011 D9

F5015 E9 F5016 E9

F5019 E9 F5020 E9

F5021 F9 1460 D2 1461 D3

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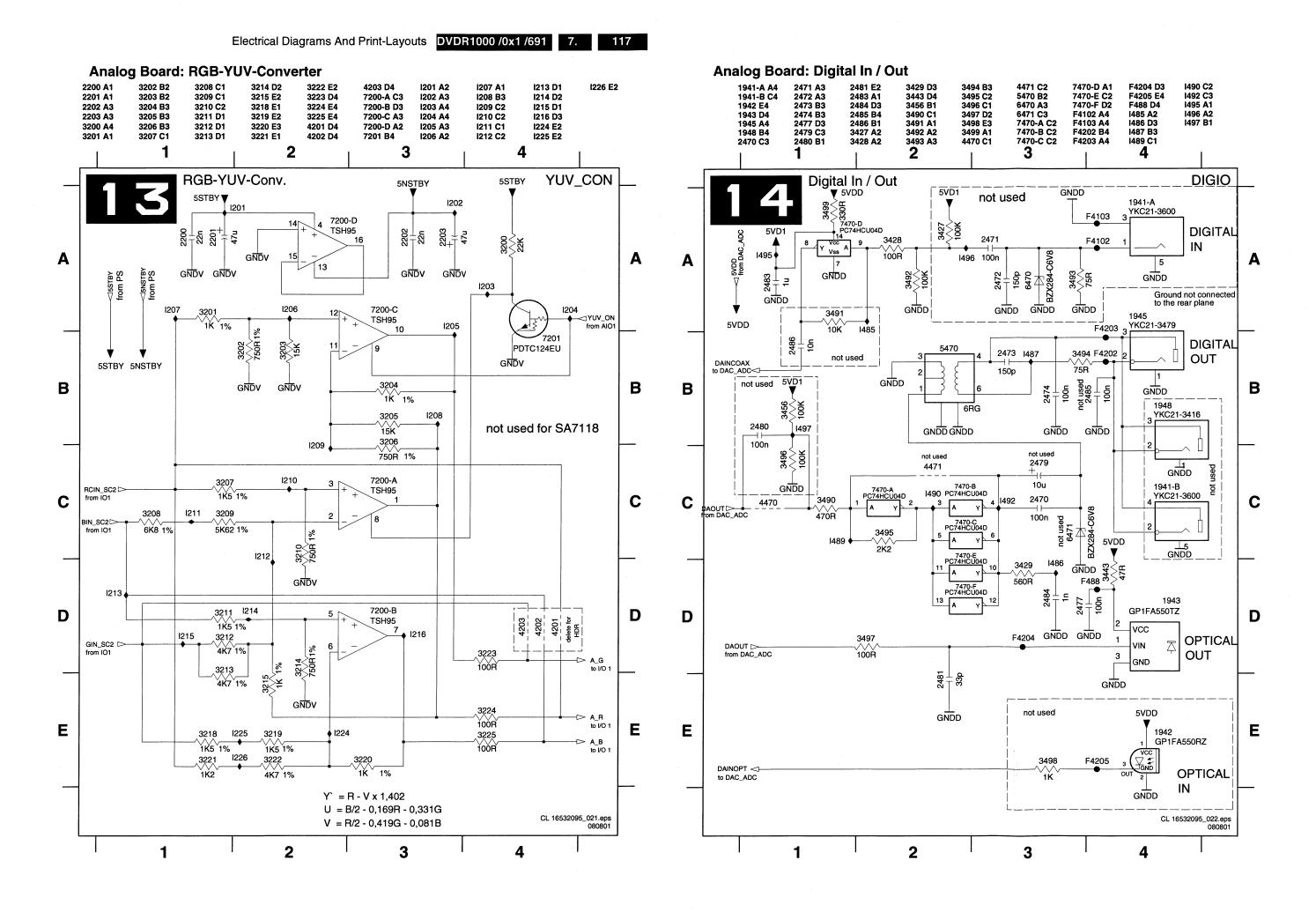
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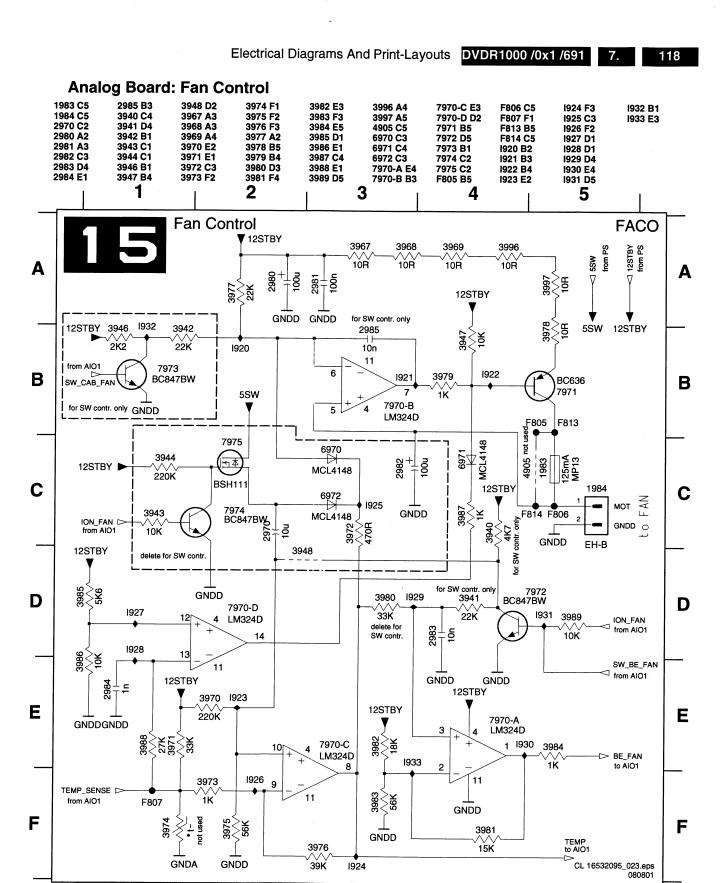
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Audio F0005 D2 Converter F0007 D2 F0009 D2 F0011 C2 F0012 C2 F0014 C2 Α F012 MCL4148 F0016 C2 F0017 B1 DAINOPT > F013 DAINCOAX From DIGIO F014 DAOUT <>→ to DIGIO GNDD 1900 FMN GNDD -DAOUT В DAINCOAX DAINOPT 5VD 18 F0017 5004 ЗVD D_IKILL GNDD D_PCMCLK C GNDD D_DATA0 D_WCLK GNDD D_BCLK 2028 ↓ †+ 10u 2027 100n QUD F0007 3008 C6 1034 A4 220p GNDD 3009 C8 1035 A4 GNDA GNDA GNDA GNDA 1026 1011 3011 3010 C6 3011 D7 1036 B4 A_PCMCLK GNDD GNDD GNDD 1037 E3 4K7 1% D 2023 ⊤ ⊤ 47p D 3012 D7 3013 F2 GNDD 1038 E1 not used 5 F0005 1012 3012 1039 F1 8STBY A_DAT 3014 D2 4K7 1% OND F0003 3V3DD 3V3DD 3V3DD 3015 E2 GNDD GNDD 2008 330p 330p 4K7 3014 2009 1013 A_WCLK F0002 3015 22R 100n 2019 3018 E6 7004 GNDA UDA1360TS A_BCLK 3019 E6 2 F0001 22R 16 9 100n 3018 3019 1R5 3019 3020 E2 GNDD GNDD GNDA 3021 F2 1015 1037 VDDA VDDD GNDA GNDA 3022 F8 ᅙ 7002-B 5 3023 E3 Ε MC33078 F011 14 FSEL CLOCK VREFP E 5001 Bead 2001 3024 E3 GNDD CONTROL 3024 7 PWON VREFN GNDD -1027 ^∕^\ 47K + 1001 1001 1001 1016 3026 A2 VREF VINL ADC 3027 B2 ΣΔ 3028 F5 2013 2014 1038 3020 3029 C8 3030 C3 1022 100n 12K 1% VINR 47u DC-CANCEL GNDA GNDA GNDA 3032 F8 2015 GNDA 1039 3021 FILTER 1019 5000 B3 5NSTBY 11 BÇK ARADCI> 5001 E1 DIGITAL DATAO 13 12K 1% 47u 12 WŞ 5002 B3 3022 3032 5003 B1 F 5K1 1% 3013 22R 22B 2020 47p 47p 47p 47p 6 SFOR 5004 B1 VSSD VSSA 6000 A1 10 15 2018 7000 A6 ♦1023 7001 A4 пot 7002-A B8 220p GNDD GNDD GNDA GNDA GNDD GNDD GNDA 7002-B E8 1020 7004 E4 CL 16532095_020.eps 7005 C3 F0001 E1 1 2 3 5 4 6 7 8 9

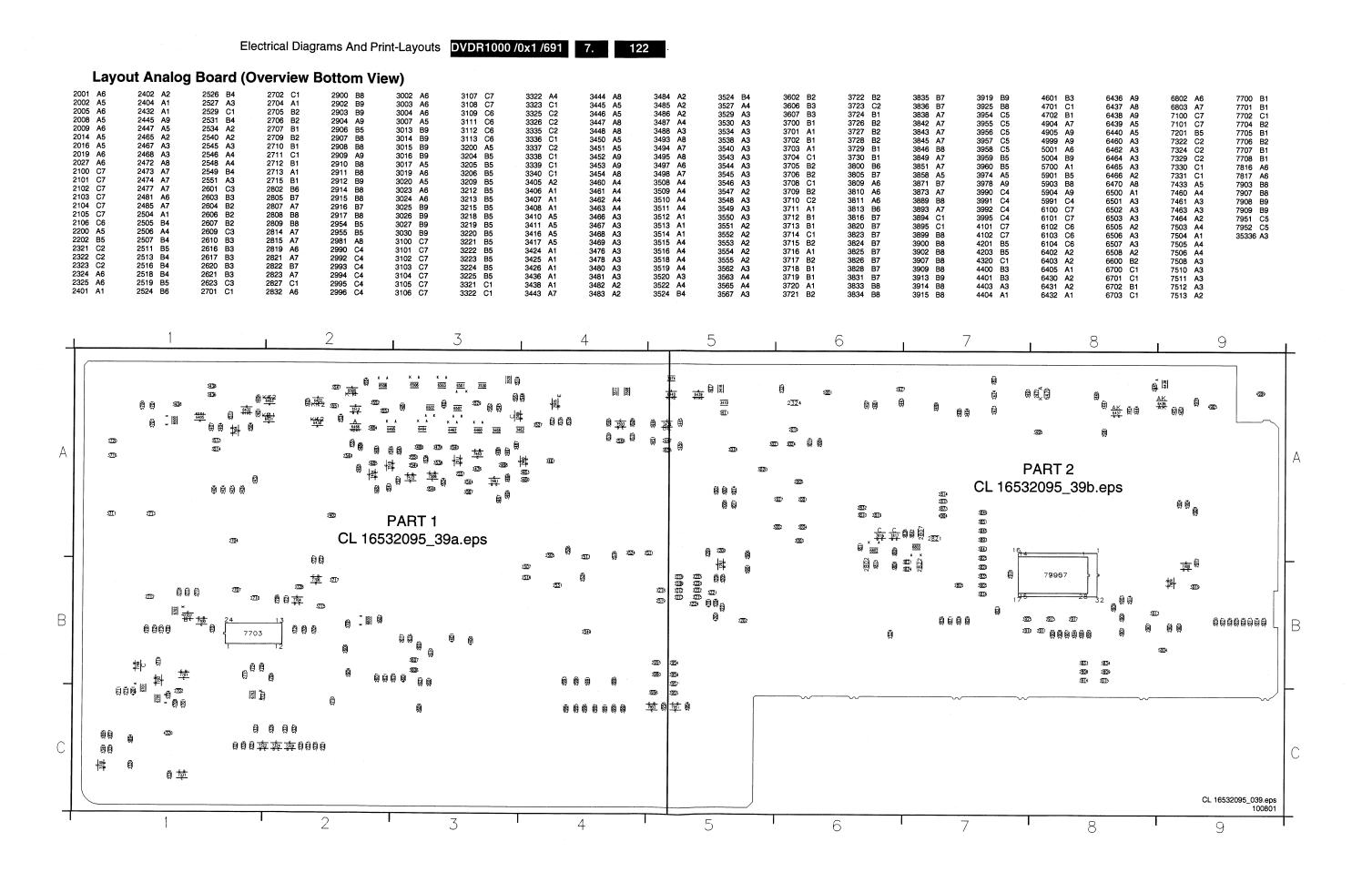


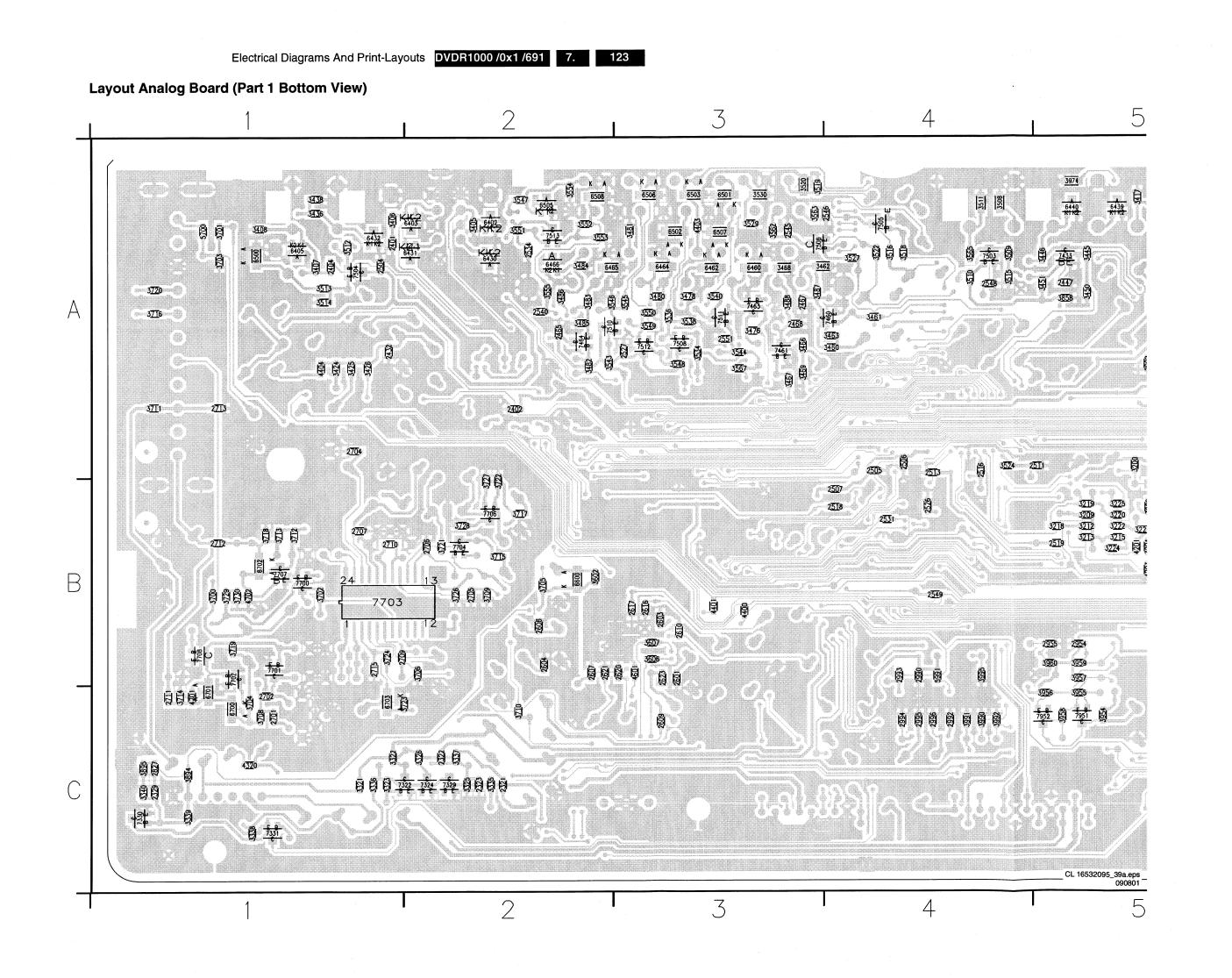


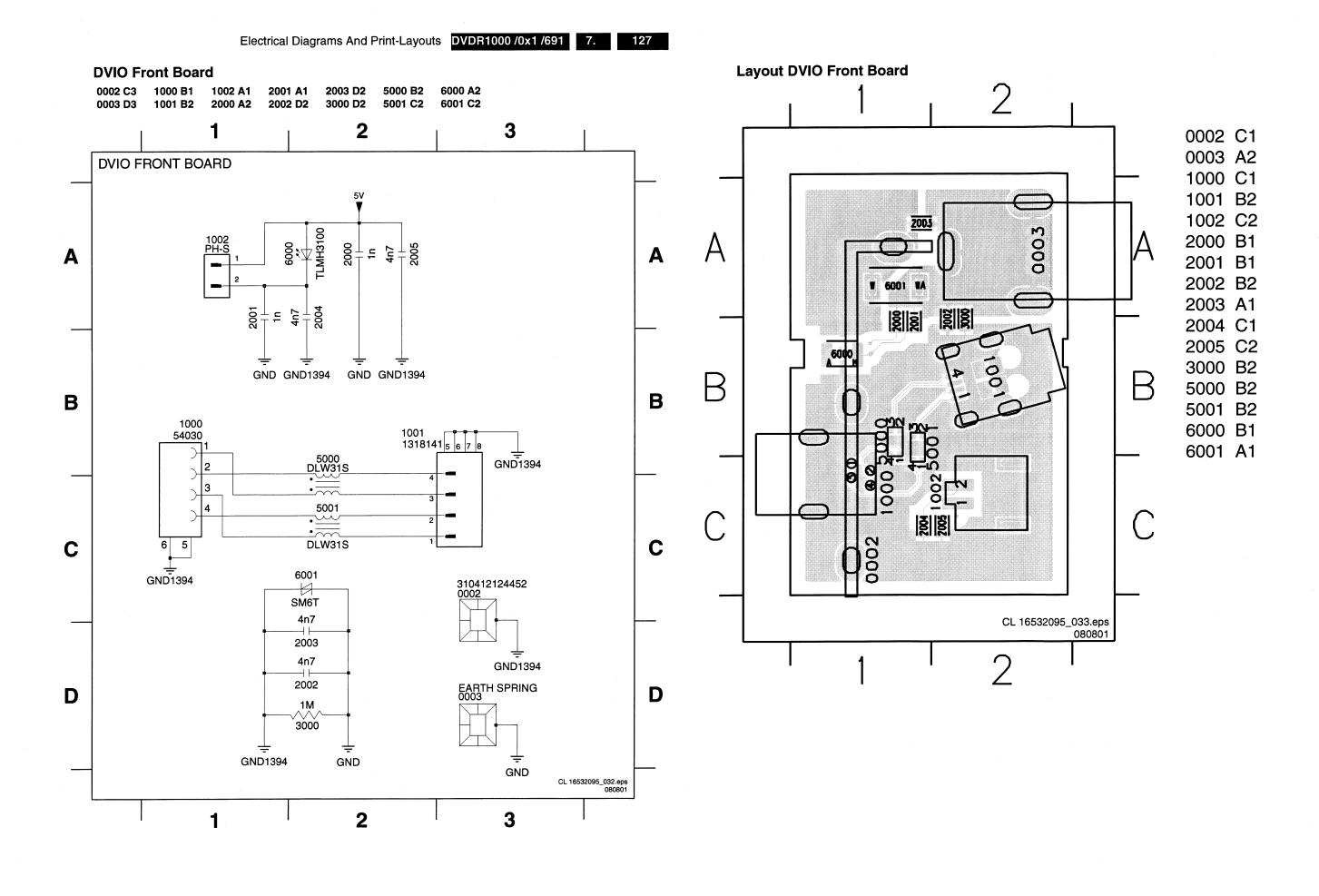
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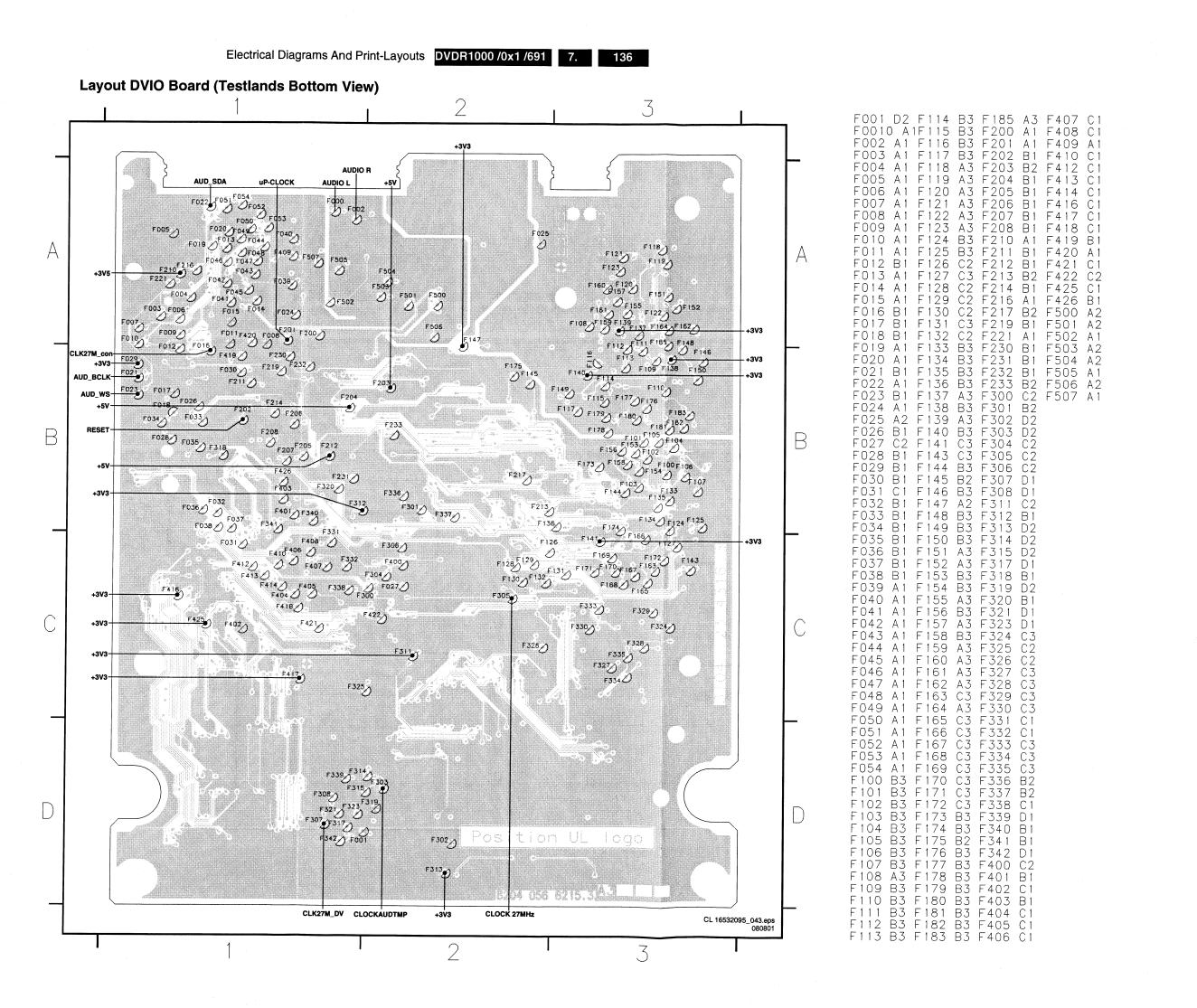
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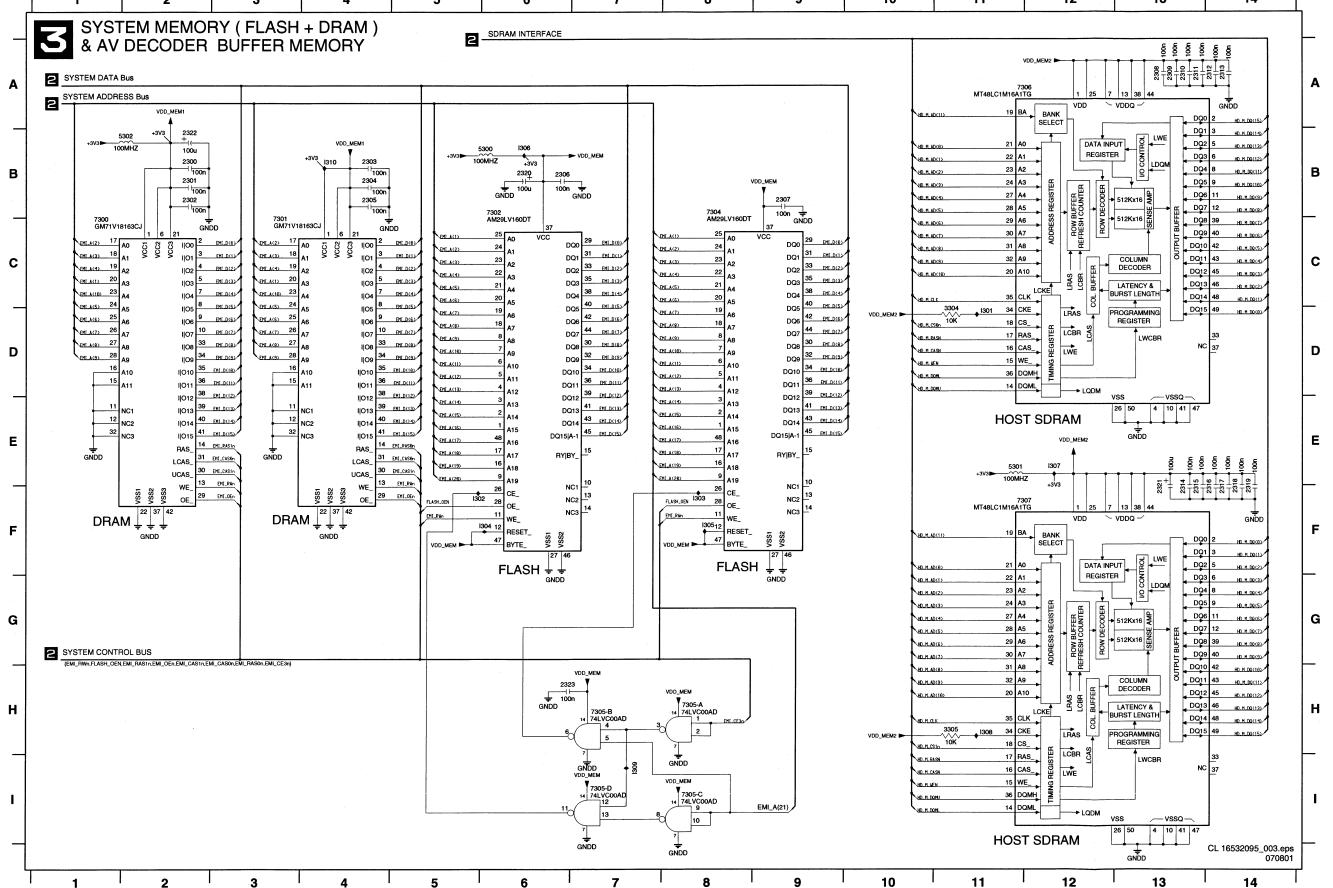




2312 A14 2313 A14

2315 F13

2316 F14 2317 F14 2318 F14 2318 F14 2320 B6 2321 F13 2322 B2 2322 B2 2323 H6 3305 H11 5300 B6 5301 E11 5302 B2 7300 C1 7301 C3 7302 B8 7305-A H8 7305-A H8 7305-C I8 7305-C I8 7305 F12 2307 F12 2307 F12 1307 F12



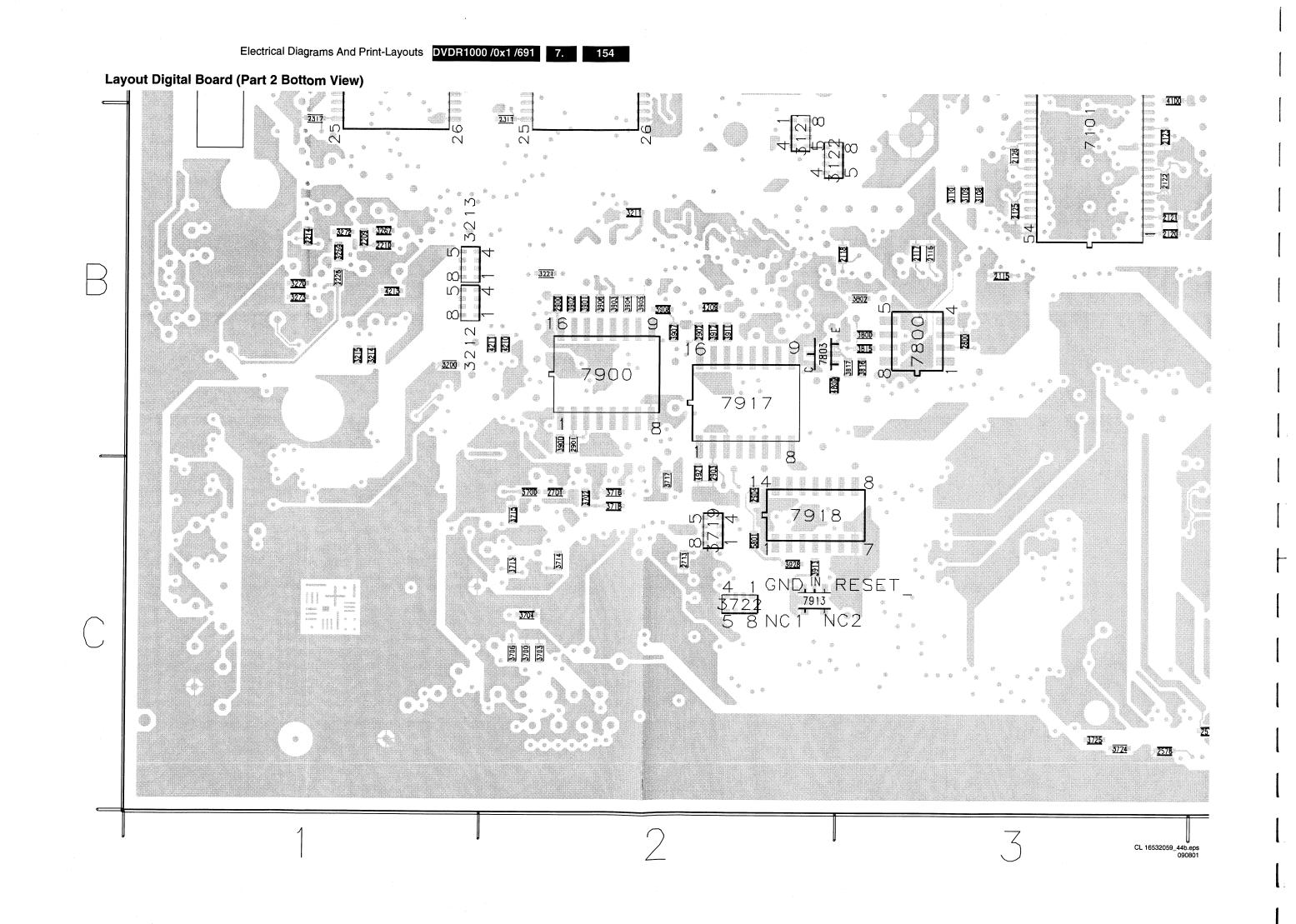
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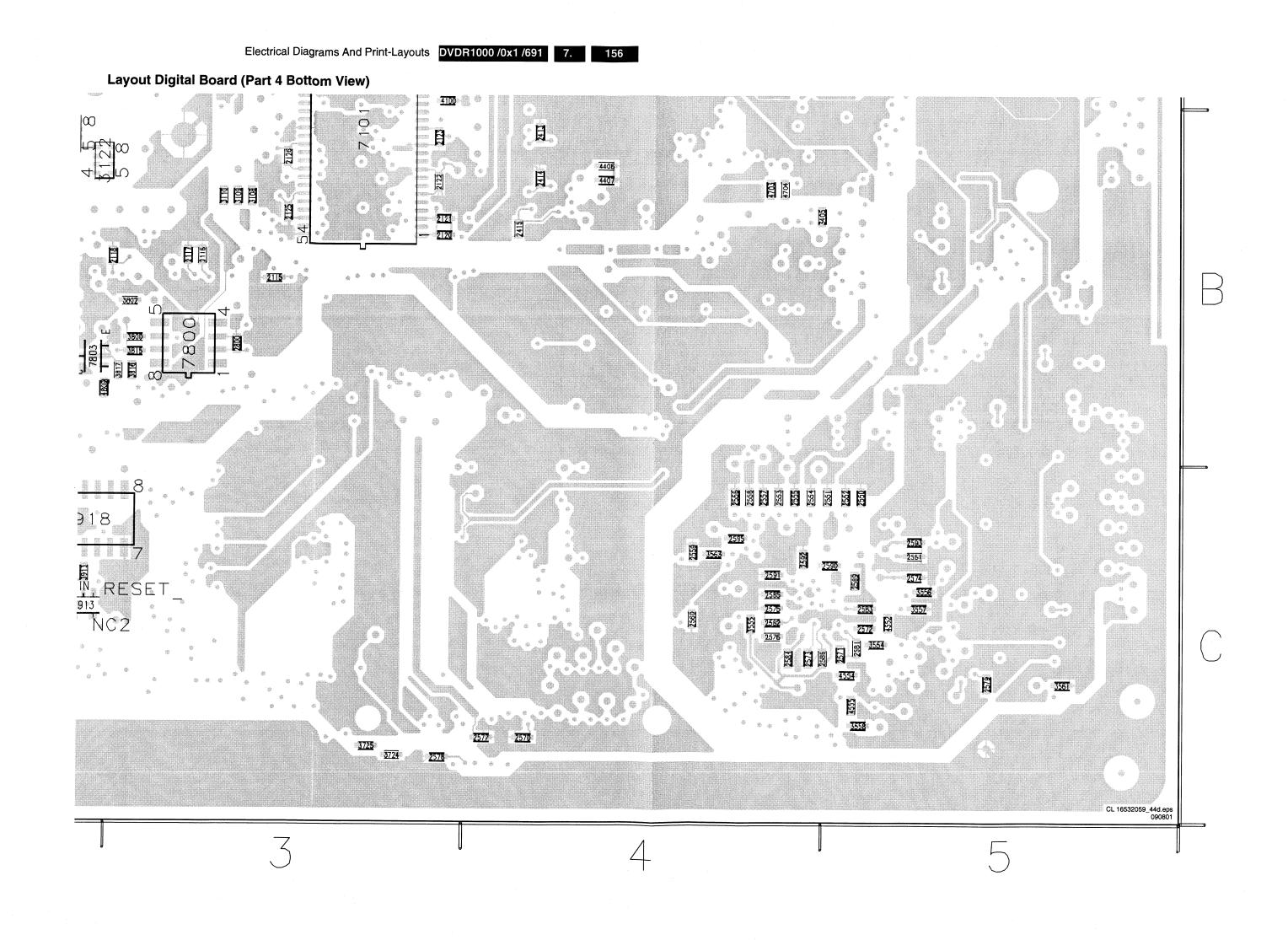
11

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GNDD CL 16532095_008.eps 070801





Alignments

ADJUSTMENT INSTRUCTIONS ANALOGUE BOARD

Test equipment:

1. Dual-trace oscilloscope

Voltage range Frequency

Probe

: 0.001 ~ 50 V/div : DC ~ 50 MHz

: 10:1, 1:1

2. DVM (Digital voltmeter)

3. Frequency counter

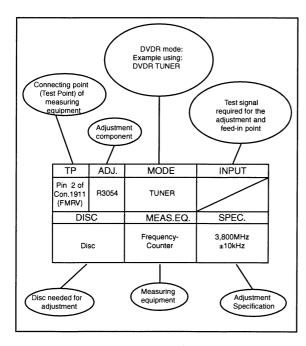
4. Sinus generator

Sinus

: 0 ~ 50 MHz

5. Test pattern generator

How to read the adjustment procedures:



Front End (FV)

Service tasks after replacement of IC 7703, coil L5702 and L5703:

1 AFC Adjustment:

Purpose: Correct adjustment of demodulator AFC - circuit

Symptom, if incorrectly set:

Bad or disturbed TV channel reception.

PAL - AFC adjustment [5703]:

	_		
TP	ADJ.	MODE	INPUT
IC 7703 Pin 17 (I976)	L5703	TUNER	38,9MHz 500mV _{pp} at Tuner 1705, Pin 11 (F700, IF-out)
DIS	SC	MEAS.EQ.	SPEC.
		DC Voltmeter Frequ. Generator	2,5V ±0,2V

2 HF - AGC adjustment [3707]:

Service tasks after replacement of IC 7703:

Purpose: Set amplifier control.

Symptom, if incorrectly set:

Picture jitter if input level is too low and picture distortion if input level is too high.

TP	ADJ.	MODE	INPUT
Tuner 1705 Pin 11 (F700, IF-out)	R3707	Set tuned to channel 27	4,5mV(74dBµV) on aerial input PAL white picture, audio IF on, no modulation
DIS	SC	MEAS.EQ.	SPEC.
		Oscilloscope Video Pattern Generator	550mV _{pp} +/-50mV (use a 10:1 probe)

3 Attenuating the 40.4 MHz [5702]: (SECAM only)

Service tasks after replacement of coil 5702:

Purpose: To attenuate the band I carrier rests.

Symptom, if incorrectly set:

Bad picture quality when the filter attenuates the picture carrier (38.9MHz).

TP	ADJ.	MODE	INPUT
OFW 1700 Pin 1 (F704)	L5702	TUNER	40.4 MHz, 300mV _{ms} at Tuner 1705, Pin 11 (F700, IF-out)
DIS	SC	MEAS.EQ.	SPEC.
		Oscilloscope, Sinus Generator, Counter	adjus t minimum amplitude

If the adjustment is correct the signal at pin 1 of OFW [1 700] must be smaller than the input signal amplitude by at least 5 dB.

9. Circuit-, IC Descriptions and List of Abbreviations

9.1 Multi-Mode SOPS 50PS203

Why Multi-Mode SOPS? 9.1.1

Using ordinary SOPS results in a decrease of the efficiency at low output loads due to the increase of the switching frequency.

The Multi-Mode SOPS will reduce the switching frequency at low loads but still preserves valley switching.

9.1.2 Block Diagram

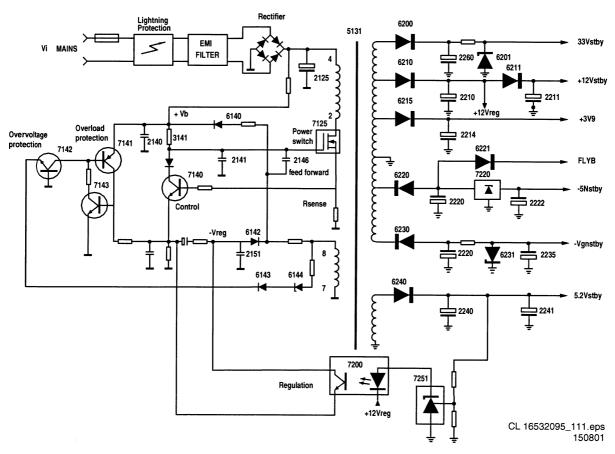


Figure 9-1

Circuit Description

Input Circuit

The input circuit consists of a lightning protection circuit and

The lightning protection comprises R3120, sparkgaps 1124 and 1125. D6128, 6129, C2127 and R3129 are optional. L5110, L5115, C2120 and L5120 form the EMI filter. It prevents inflow of noises into the mains.

Primary Rectifier/smoothing Circuit

The AC input is rectified by diodes 6151,6152, 6153, 6154 and smoothed into C2125. The voltage over C2125 is approximately 300V. It can vary from 200V to 390V.

This circuit is formed by R3125, 3126, R3141, C2140 and R3132.

When the power plug is connected to the mains voltage, the MOSFET 7125 will start conducting as soon as the gate voltage reaches a treshold value. A current starts to flow in primary winding 2-4. The MOSFET will be fed forward via winding 7-8, R3150 and C2146.

+Vb Supply and Negative Regulation Voltage

The positive part of the voltage over winding 7-8 will be rectified via R3150, D6140 and charged via R3140 into C2140. The voltage over C2140 has a value of +30 till +40V. This value depends on the value of the mains voltage Vi and

The negative part of the voltage over winding 7-8 will be rectified via R3150, D6142 and charged into C2151. The voltage over C2151 has a value of -15V and is used as regulation voltage.

Control Circuit

The control circuit exists of T7140, D6141, C2144 and 2145, C2147, R3147 and 3148.

This circuit is fed by supply voltage +Vb via R 3141. This circuit controls the conduction time and the switching frequency of the power switch circuit. It switches off the MOSFET as soon as the voltage over Rsense reaches a certain value. This value depends on the error voltage at the emittor of T7140, which can be positive or negative (+/-0,66V). The voltage fed back by the regulation circuit defines this error voltage.

Power Switch Circuit

This circuit comprises MOSFET 7125, Rsense formed by R3133, 3134, 3135, 3136 and 3137, R3131, R3132, D6146. Diodes 6130, 6131 and 6132 protect the control circuit in case of failure of the MOSFET.

Regulation Circuit

The regulation circuit comprises opto-coupler 7200, which isolates the base voltage of transistor 7140 at the primary side from a reference component 7251 at the secondary side. The TL431(7251) can be represented by two components:

- a very stable and accurate reference diode
- a high gain amplifier

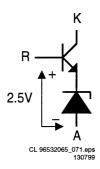


Figure 9-2

TL431 will conduct from cathode to anode when the reference is higher than the internal reference voltage of about 2.5V. If the reference voltage is lower, the cathode current is almost zero.

The cathode current flows through the LED of the optocoupler. The collector current of the opto-coupler will adjust the feedback level of the error voltage at the emittor of T7140.

Overload Protection Circuit

This circuit consists of R3145, C2143, a thyristor circuit formed by T7141 and T7143, R3143 and R3142. When the output is shortened, the thyristor circuit will start to conduct and switch off the supply voltage over C2140. This results in a switching of f of the drain current of the MOSFET 7125 and the output will be disabled. The start circuit will try to start up the power supply again. If the circuit is still shortened, the complete start and stop sequence will repeat. The power supply comes in a hiccup mode (is ticking).

Overvoltage Protection Circuit

This circuit consists of R3149, D6144, 6143, R3144, C2142

When the regulation circuit is interrupted due to an error in the control loop, the regulated output voltage will increase (overvoltage). This overvoltage is sensed on the primary

When an overvoltage is detected, the circuit will start up the thyristor circuit T7141-7143. The power supply will come in a hiccup mode as long as the error in the control loop is present.

Secondary Rectifier/Smoothing Circuit

There are 6 rectifier/smoothing circuits on the secondary side. Each voltage depends on the number of windings of the transformer.

From these circuits a lot of voltages are derived and fed to 3 connectors. The following voltages are present at the output:

Functional use: to Digital board + Dvio board

- 1. +3V3(for dig pcb + DVio)
- 2. +3V3(for dig pcb + DVio)
- +3V3(for dig pcb + DVio)
- 4. +3V3(for dig pcb + DVio)
- 5. GND(for dig pcb + DVio)
- 6. +12V(for dig pcb + DVio)
- 7. GND(for dig pcb + DVio)
- 8. GND(for dig pcb + DVio)
- 9. +5V(for dig pcb + DVio)
- 10. STBY control(for dig pcb + DVio)
- 11. GND(for dig pcb + DVio)
- 12. -5V(for dig pcb + DVio)

The +12V is switched off by the STBY_ctrl signal.

When the +12V is switched off, also the +3V3, +5V and -5V are switched off. All these voltages are low drop regulated. Connector 0205

Functional use: to analogue board + display board + flap motor

'STBY' indicates that the voltage will not be switched off in the standby situation.

- 1. +12VSTBY(= +12V Standby, for display heating, 8Vstby)
- 2. +5VSTBY(= +5V Standby; general use)
- 3. -5NSTBY(= -5V Standby; neg. voltage for drivers)
- 4. VGNSTBY(= -32V Standby; for display grids)
- 5. +33STBY(= +33V Standby; for tuner)
- 6. FLYB(flyback pulse for power fail + measurement)
- 7. GNDA(Ground for the analogue board)

Connector 0207 Functional use: to engine

- 1. +3V3(for engine servo board)
- 2. +5V(for engine servo board)
- 3. GND(for engine servo board)
- 4. +4V6E(for engine analog part)
- 5. GND(for engine servo board)
- 6. -5V(for engine servo board) 7. GND(for engine motor currents)
- 8. +12V(for engine motor currents)

9.2 **Display Board**

9.2.1 Operation Unit DC (DC Part)

The core element of the operation unit DCis the microcontroller TMP88CU77ZF [7156]. The TMP88CU77ZF is an 8 bit microcontroller fitted with 96kB RO M and 3kB RAM and is responsible for following functions:

- Integrated VFD driver
- Timer
- Evaluation of the keyboard matrix
- Decoding the remote control commands from the infrared receiver pos. 6170
- Activation of the display
- Motor driver

The system clock is generated with the 12/1 Hz quartz (Pos. 1153).

9.2.2 **Evaluation of the Keyboard Matrix**

There are 15 different keys on the display oard. A resistor network is used to generate a specific dire;t voltage value, depending on the key pressed, via the resit ors 3145, 3171, 3183 and 3194 on the analog/digital (A/D) ports (7156 Pin 17, 18, 19, 20). Pressing keys simultaneously n ay lead to undesired functions!

9.2.3 IR Receiver and Signal Evaluation

The IR receiver [7140] contains a selectively controlled amplifier as well as a photo-diode. The photo-diode changes the received transmission (approx. 940nm) in electrical pulses, which are then amplified and demodulated. On the output of the IR receiver [7140], a pulse sequence with TTLlevel, which corresponds to the envelope curve of the received IR remote control command, can be measured. This pulse sequence is input into the controller for further signal evaluation via input IRR [7156, pin 2].

9.2.4 **Motor Driver Flap**

The flap-motor is controlled via the 2 Port-Pins (MD1, MD2) of the P (7156, Pin 12, Pin 100). The motor driver part is constructed as a bridged dual power operational amplifier. Between the IC outputs (7120, Pin1, Pin3) and a Boucherot circuit (2121, 3126) suppresses a spurious 3MHz oscillation from the output stage. The two ports-pins (MD1, MD2) of the P are PWM-outputs and are controlled in the following way:

Flap Motor:

	MD1	MD2
off	Н	L
open	Н	PWM(H)
close	L	PWM(L)

Duty Cycle 50% for OPEN and CLOSE

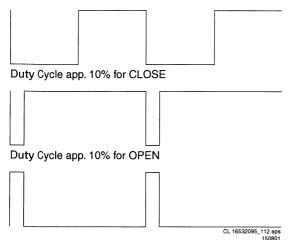


Figure 9-3

For the detection of the end-positions of the flap there are two switches (1178, 1179) installed and the information is evaluated from the P via the signals SW_1178 and SW_1179.

Flap Switches:

	SW1	SW2
open	L	Н
closed	Н	L
moving	Н	Н
error	L	L

9.2.5 Bi-Color LED (Standby and ON)

The STBY-LED is a red/green bi-color-LED and is controlled via the STBYLED-signal of the P (7156 Pin 10) in the following way:

Colour of STBY LED	Status of the Set
red	STBY
green	ON

9.3 **Analogue Board Europe**

9.3.1 Microprocessor TMP93C071F

The microcontroller "AIO" TMP93C071F is a 16bit microcontroller with internal ROM and 8kB RAM. It includes the following functions:

- A/D converters
- composite sync input
- I²C bus interface

Following connection to the mains, a positive pulse on the reset input on the P is generated by the reset-IC TL7705 (Pos.7900). The system clock is generated with the 20MHz quartz (Pos. 1994).

9.3.2 Bus Systems

The communication between the P and the other functional groups is via the I2C-bus (SDA, SCL). The clock rate is approx. 95kHz.

Functional groups on the I²C bus:

- E²PROM ST24E16 (Pos. 7815)
- Tuner (Pos. 1705)
- Matrix-switch STV6410 (Pos. 7507)
- Audio IC / MSP (Pos. 7600)
- Display board (Pos. 1987)
- VPS-IC (Pos. 7990).

9.3.3 E²PROM

The E²PROM ST24E16 (Pos. 7815) is an electric erasable and programmable, non-volatile memory. The E²PROM stores data specific to the device, such as the AFC-reference value, clock-correction-factor, etc. The data is accessed by the P via the I²C-bus.

VPS, PDC, Teletext (Europe Only)

The STV5348 (Pos. 7990) is a VPS, PDC, and Teletext Decoder with an external 13,875Mhz quartz.

The following data formats are identified:

- VPS (Timer data and station name)
- PDC Format 2 (Timer data and station name)
- PDC Format 1 (station name and time)
- TXT header line (time for "time download")

9.3.5 FOME

The FOME-circuit compares the video signal coming from the tuner and the one coming from the Scart-plug 1. If the video-signals are identical the output of the FOME-circuit is low.

9.3.6 Fan Control

The fan control circuit is necessary to control the speed of the cabinet fan (Pos. 1984) according to the requirements in temperature and noise. The temperature is measured via an NTC on the display board (Pos. 3145). When the temperature is lower than 25°C the fan-voltage is approx. 5V

and will reach approx. 10V at a temperature of 40°C. It is also possible to switch off the fan via the control line ION_FAN. The circuit generates also two control-signals: TEMP goes to the P and BE_FAN is the control-line for the basic engine fan.

9.3.7 **Power Supply**

The 5SW and 8SW supply are switched off in case of standby from the P via the ISTBY-line. This is possible for powersave. The ISTBY-line must be low in case of STBY. There is also a "power fail" circuit on the PS-schematic which is necessary to mute AUDIO when IPFAIL is low.

9.3.8 Front End (TU, AP Part)

The Front End Comprises the Following Parts:

- Tuner [1705]
- IF amplifier & video demodulator IC TDA 9818 [7703]
- Sound processor MSP3415G [7600]

IF Selection

The IF frequency of the video carrier is 38.9 MHz for all systems except SECAM L' (33.9 MHz).

A quasi-split audio system is used. Separate surface-wave filters (SAW) are required. [1700], [1701] for video, [1702] for audio. [1700] Is switched into the signal path for DK/I-SECAM L/L' reception, if the signal SAWS is "high". In this case the switches [7701], [7702] are open and the diode [6700] is conducting. [1701] Is switched into the signal path for BG reception, if the signal SAWS is "low". Then the switch [7708] is open and the diode [6701] is conducting. For DK/I-SECAM L/L' reception, an additional circuit for suppressing the adjacent channel audio carrier is provided, which is set using coil [5702] to maximum suppression at 40.4MHz.

IF Demodulator

TDA 9818

The IF signal from the tuner is processed by the demodulator IC TDA 9818 [7703]. The signal PSS to pin3 switches between demodulation of positive SECAM or negative PAL modulated video carriers. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. The audio-IF carrier is selected in the audio SAW filter [1702]. This filter is switched for SECAM L'. If the signal SB1 is "high", the switch [7707] is closed and the diode [6702] is not conducting. For all other standards the diode [6702] is conducting and the switch [7707] is open. The output signal from this SAW filter is first processed in the TDA 9818. Audio carriers are converted from the tuner IF level into the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5703] on the TDA 9818 is adjusted so that when a frequency of 38.90 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of the TDA 9818 is 2.5V. The setting of the picture carrier frequency for SECAM L in the TDA 9818 is achieved by connecting pin 7 of the IC via a resistor [3702] to earth. The switch [7700] and the signal SB1 "high" do this. The HF-AGC is set using the AGC controller [3707] so that, with a sufficiently large antenna input signal (74 dBV), the voltage at the IF output of the tuner [1705] pin 11 is 500 mVpp. This setting must be carried out, when the audio carrier is switched off. The demodulated video signal appears on pin 16 [7703]. The demodulator AGC voltage at pin4 is used to determine the antenna signal strength after a buffer [7705] with the signal AGC_MUTE. In the opposite direction this line may be used to mute the demodulator to avoid cross talk in all cases. where the tuner signal is not needed. In this case a "high" signal is sent via AGC MUTE and the conducting diode [6703] to pin4. The video trap [1703] reduces adjacent channel video and sound carrier remainders in the video for BG standards. For all other standards the switch [7704] and signal TS "low" bypass this trap. In this cases the selectivity

of the SAW filter [1700] is sufficient. A frequency response correction is achieved by the inductance [5009] for not BG standards. This correction is not preferred for SECAM L' and therefore shorts circuited by [7709], if the signal SB1 is "high". The demodulated video signal VFV is available after the buffer and limiting stage for noise peaks [7706]. The FM-PLL demodulator function of TDA 9818 is not used and deactivated by the resistor [3726].

Audio Demodulator

Sound processor MSP 3415G

The MSP 3415G [7600] is a multistandard sound processor which can demodulate FM Mono/Stereo, NICAM and AM signals. The incoming signal is first controlled and then digitised. The digital signal is then demodulated in 2 separate channels. In the first MSP channel, FM and NICAM (B/G/I/D/ K) are demodulated, whereas in the second MSP channel, FM and are demodulated again (NICAM L corresponds to NICAM B/G). These demodulated signals are selected digitally in the I/O and switched to the D/A converter on the outputs. Amplitude and bandwidth of the demodulated audio signals can be determined in the MSP using the corresponding commands via the I2C bus. The audio signal from the tuner is available at the pins 30 AFER and 31 AFEL.

Input/Output Video-Routing (Europe-Version)

General Description:

The complete Video- I/O-switching is basically realised by the I/O switch STV6410A. It is controlled via IIC-Bus-0 (SDA/ SCL) by the all in one C on the analogue board. The STV 6410 has three YCVBS switches, three chroma switches and one RGB switch. All switches have 6-dB amplification on the outputs. The YCVBS inputs have bottom clamp, the chroma inputs have average clamp, and the RGB inputs have bottom clamp circuits at the inputs. The R/C inputs can be switched to average clamp for chroma signals via I2C bus. The IC has also one slow blanking monitor and one fast blanking switch for fast RGB insertion (see detailed description in chapter 1.5). Two pre-selectors BA 7652 are additionally used: One for switching between Rear CVBS, Y-Rear and Front, the second for switching between Chroma-Rear and Front signal. Both pre-selectors are controlled via IS1 and IS2 from the analogue board C.

CVBS Signals:

There are four CVBS input connection possibilities: Front chinch (E6), Rear Chinch (E4), Scart 1 (E1) and Scart 2 (E2). Rear Chinch In is routed via the pre selector BA 7652; the other signals are connected direct to the STV 6410. The selected CVBS signal is routed to Rear Chinch Out (via BA 7660, 6dB amplification, 75 Ohm driver) and to Scart 1. Independent of the input signal quality (CVBS, S-Video or RGB) the digital board supplies also S-Video and RGB signals to the corresponding socket.

S-Video Signals:

There are also four S-Video input connection possibilities: Front In (E5), Rear In (E3), Scart 1 and Scart 2. For S-Video from Scart this option has to be switched on in the OSD menu. The pre-selectors and the STV 6410 do the signal selection (for detailed routing see overview). Also the video quality will be S-Video, the digital board supplies also CVBS to the corresponding sockets. The S-Video signal that is coming from the digital board is routed via ₽A 7660 (6-dB amplification and 75-Ohm driver) to the S-Video Rear Out socket.

RGB Signals:

The Scart 2 RGB input signal (Decoder sock⊜t) is connected to the RGB switch of STV 6410 and to the digital board in parallel. The RGB from Scart 2 is routed to Scart 1 in low

power standby mode. The direct connection (not via STV 6410) is for loop through and REC. The RGB signal, which is coming from the digital board, is connected to the RGB encoder input of the STV 6410 and is routed to Scart 1 in all

As the Scart-connection can carry either RGB- or Y/C-signals it is necessary to define the available and selected signalproperty. While Pin15 of Scart (Red or Chroma-upstream) is fully handled via STV6410A the Pin7 (Blue or Chromadownstream) has to be extra set.

- Scart1: Pin42 of C (SC1YC H-line):
 - Low (Blue-Out on SC1
 - High (Chroma-In on SC1
- Scart2: Pin41 of C (SC2RGB_H-line):
 - Low (Chroma-Out on SC2
 - High (Blue-In on SC2

Detection of Status-Information

Pin-8 (Slow-Blank):

Level-detection of Pin-8 (Scart-1 and -2) is realised by using STV6410A. It can be readout via IIC-Bus by the CC-C. To obtain the status of Scart1-Pin8, Bit 0 & 1 of register 06h must be set to 0 (Input-mode). The corresponding bits for verification of Scart2-Pin8-status are set to input-mode as

Meaning of Read-Register-Bits:

- Bit 7 & 6: not used
- Bit 5 & 4: Status Scart-2/Pin8:
 - 0 1 Low-level
 - 1 0 Medium-level (16:9)
 - 1 1 High-level (4:3)
- Bit 3 &2: not used
- Bit 1 & 0: Status Scart-1/Pin8:
 - 0.1 Low-level
 - 1 0 Medium-level (16:9)
 - 1 1 High-level (4:3)

Pin-16 (Fast Blank):

Only the status/level of Scart-2/Pin16 must be detected; this is realised by using PortC3/AIN14 (Pin25) of the CC-C as an Analogue-input.

- ADC-value lower or equal 24h (Pin16 low (no RGB-
- ADC-value greater 24h (Pin16 high (RGB present on

To avoid misdetection a "software-integration" (result is first valid if it was 3-times the same) must be implemented, determination has to be done approx. every 47msec (no multiple of V-sync).

WSS on Y/C-Plug:

Picture-Ratio-Information (16:9 or 4:3) on SVHS-connections is coded via the average DC-level of the Chroma-signal-line, detection is realised by using an analogue-input-port of the CC-C

- ADC- value lower or equal 40h (4:3-picture-ratio delivered
- ADC-value greater 40h (16:9-picture-ratio available on

Y/C-Rear is determined via Port40/AIN3 (Pin14) of CC (WSRI-line) and Port41/AIN4 (Pin15) is used for Y/C-Front (WSFI-line).

Generation of Status-Information

Pin-8 (Slow Blank):

Only on Scart-1 the Slow-Blank-Status (Level of Pin8) must be created, which is done via IIC-Bus-register 06h (Bits 0 & 1) of the STV6410A.

Pin-16 (Fast Blank):

Only the status/level of Pin16-Scart1 must be controlled; this is realised by using the FB-switch-capabilities of the STV6410A, which are set via IIC-Bus-register 04h (bits 4 &

WSS on Y/C-Plug:

The appropriate DC-level on Chroma-signal-line for Y/C-Rear-Out is produced via Port57 (Pin10) of the CC-C (WSRO-line).

- 4:3 Picture-ratio supported on Y/C-Plug: Port57 set to 0
- 16:9 Picture-ratio supported on Y/C-Plug: Port57 set to

9.3.10 Audio Routing Analogue board (Europe / Nafta)

General Description:

The Audio- I/O switching is realised by the STV6410 I/O

By I²C Bus (SDA-0/SCL-0) it is possible to control all the Audio in- and outputs (for detailed Information we refer to the STV6410 routing overview).

Analog audio coming from DV-Board and second rear Cinch input is routed via MSP3415 to the STV 6410. After selecting the audio source via STV 6410, the signal must be transformed into the digital domain. For this, the UDA 1360TS (ADC) is responsible. An input-voltage of up to 2Vrms can be handled from the IC's. For further processing, the UDA 1360TS (ADC) delivers the data-in I^2S format to the digital-board. After a certain delay the (processed) data come back from the digital board to the UDA 1328 (DAC). The UDA 1328 (DAC) transforms the I²S data back into the analog domain and feeds the signals direct to the MC33078 (OPV). From the MC33078 (OPV) the signals are delivered back to the STV 6410 and also direct to the 2nd rear out Cinch. The other outputs (Scart, Cinch) are supported by the STV 6410.

Detailed Description STV 6410:

The STV 6410 is an I²C bus controlled audio and video switch matrix, which is able to handle audio input signals up to 2 Vrms. The used outputs are equipped with internal level adjustment possibility. Low distortion and very good channel separation is a typical peculiarity of this IC. The output resistance is very low and the frequency bandwidth is up to 50 kHz.

Detailed Description UDA 1360:

The UDA 1360TS is a stereo Analog-to-Digital Converter employing bitstream conversion techniques.

The UDA supports the I²S-bus data format and the MSBjustified data format with word lengths of up to 20 bits. The IC supports also 2Vrms input signals and is designed for 3V3 supply voltage.

The device is able to handle system clocks of 256fs and

Typical THD+N at 0dB is -85dB and a S/N performance up to 97dB is possible.

Detailed Description UDA 1328:

The UDA1328 is a 6 channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.

The UDA 1328 supports the I²S-bus data format with word lengths of up to 24 bits.

Digital sound features can be controlled with the L3 interface. System clock can be set to 256fs or 384fs.

The Device also provides 2 high quality differential outputs. Typical THD+N at 0dB is -95dB and a S/N of up to 106dB is possible.

Supply voltage is 3V3.

Circuit-, IC Descriptions and List of Abbreviations DVDR1000 /0x1 /691

GB 163

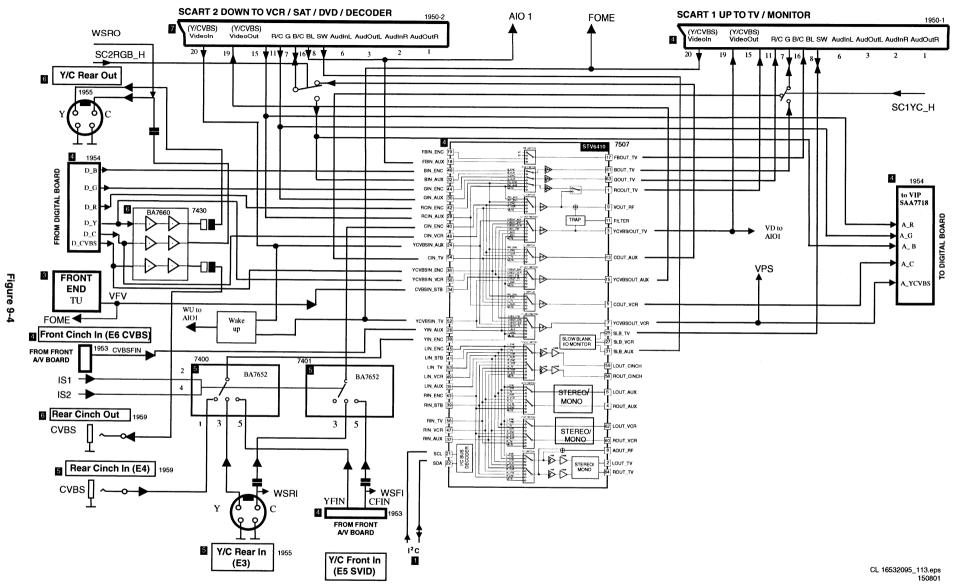
Detailed Description MC 33078:

The MC33078 is a dual operational amplifier for audio applications.

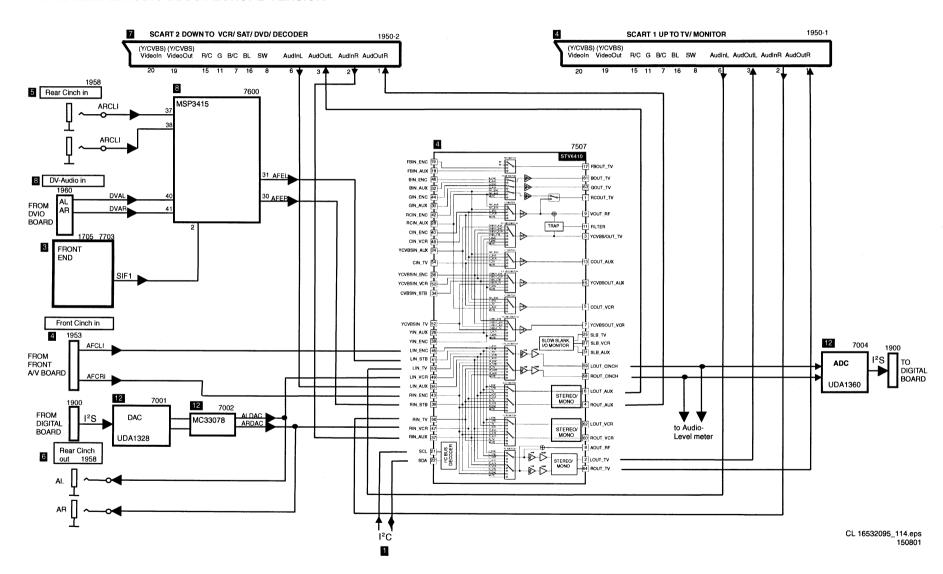
It offers low voltage noise (4,5nV/ $\sqrt{\text{Hz}}$) and high frequency performances (15MHz Gain Bandwidth product, 7V/s slew rate).

In addition the MC33078 has a very low distortion (0,002%).

BLOCK DIAGRAM VIDEO IN/OUT EUROPE-VERSION (Y/CVBS) (Y/CVBS) WSRO



BLOCK DIAGRAM AUDIO IN/OUT EUROPE-VERSION



Analog Board Nafta version

9.4.1 Microprocessor TMP93C071F

The microcontroller "AIO" TMP93C071F is a 16bit microcontroller with internal ROM and 8kB RAM. It includes the following functions:

- A/D converters
- composite sync input
- I²C bus interface

The following connection to the mains, a positive pulse on the reset input on the P is generated by the reset-IC TL7705

The system clock is generated with the 20MHz quartz (Pos. 1994).

9.4.2 Bus Systems

The communication between the P and the other functional groups is via the I²C-bus (SDA, SCL). The clock rate is approx. 95kHz.

Functional groups on the I²C bus:

- E²PROM ST24E16 (Pos. 7815)
- Tuner (Pos. 1705)
- Matrix-switch STV6410 (Pos. 7507)
- Audio IC / MSP (Pos. 7600)
- Display board (Pos. 1987)

9.4.3 E²PROM

The E²PROM ST24E16 (Pos. 7815) is an electric erasable and writeable, non-volatile memory. The E²PROM stores data specific to the device, such as the AFC-reference value. clock-correction-factor, etc. The data is accessed by the P via the I2C-bus.

9.4.4 FOME

The FOME (Follow Me) -circuit compares the video signal coming from the tuner and the one coming from the Scartplug 1. If the video-signals are identical the output of the FOME-circuit is low.

9.4.5 Fan Control

The fan control circuit is necessary to control the speed of the cabinet fan (Pos. 1984) according to the requirements in temperature and noise. The temperature is measured via an NTC on the display board (Pos. 3145). When the temperature is lower than 25°C the fan-voltage is approx. 5V and will reach approx. 10V at a temperature of 40°C. It is also possible to switch off the fan via the control line ION_FAN. The circuit generates also two control-signals: TEMP goes to the P and BE_FAN is the control-line for the basic engine fan.

9.4.6 **Power Supply**

The 5SW and 8SW supply are switched off in case of Stby from the P via the ISTBY-line. This is possible for powersave. The ISTBY-line must be low in case of STBY. There is also a "power fail" circuit on the PS-schematic which is necessary to mute AUDIO when IPFAIL is low.

9.4.7 Front End (TU, AP Part)

The front end comprises the following parts:

- Tuner [1705]
- IF amplifier & video demodulator IC TDA 9817 [7703]
- Sound processor MSP3445G [7600]

IF Selection

The IF frequency of the video carrier is 45.75 MHz. A guasisplit audio system is used. Separate surface-wave filters (SAW) are required. [1701] for video, [1702] for audio.

IF Demodulator

TDA 9817

The IF signal from the tuner is processed by the demodulator IC TDA 9817 [7703]. A QSS-audio-IF signal SIF1 is generated for demodulation in the sound processor [7600]. Audio carriers are converted from the tuner IF level into the audio IF position and further processed in the audio demodulator [7600]. The AFC coil [5703] on the TDA 9817 is adjusted so that when a frequency of 45.75 MHz is supplied to the IF output of the tuner, the AFC voltage on pin 17 of the TDA 9817 is 2.5V. The HF-AGC is set using the AGC controller [3707] so that, with a sufficiently large antenna input signal (74 dBV) the voltage at the IF output of the tuner [1705] pin 11 is 500 mVpp. This setting must be carried out, when the audio carrier is switched off. The demodulated video signal appears on pin 16 [7703]. The demodulator AGC voltage at pin4 is used to determine the antenna signal strength after a buffer [7705] with the signal AGC_MUTE. In the opposite direction this line may be used to mute the demodulator to avoid crosstalk in all cases, where the tuner signal is not needed. In this case a "high" signal is sent via AGC_MUTE and the conducting diode [6703] to pin4. The video trap [1703] reduces adjacent channel video and sound carrier remainders in the video. The demodulated video signal VFV is available after the buffer and limiter stage for noise peaks [7706]. The FM-PLL demodulator function of TDA 9817 is not used and deactivated by the resistor [3726].

Audio Demodulator

Sound processor MSP 3445G

The MSP 3445G [7600] is a NTSC sound processor. Amplitude and bandwidth of the demodulated audio signals can be determined in the MSP using the corresponding commands via the I2C bus. The audio signal from the tuner is available at the pins 30 AFER and 31 AFEL.

9.4.8 Video-Routing (Nafta Version)

General Description:

The complete Video- I/O-switching is basically realised by the I/O switch STV6410A, which is controlled via IIC-Bus-0 (SDA/SCL) by the all in one C on the analogue board. The STV 6410 has three YCVBS, three chroma, and one RGB switch which is not used in the Nafta I/O. All switches have 6dB amplification on the outputs. The YCVBS inputs have bottom clamp, the chroma inputs have average clamp, and the RGB switch has bottom clamp circuits at the inputs. The R/C inputs can be switched to average clamp for chroma signals via I2C bus.

Two pre-selectors BA 7652 are additionally used: One for switching between Y- Rear and Front, the second for switching between Chroma-Rear and Front signal. Both preselectors are controlled via IS1 and IS2 from the analogue board C.

CVBS Signals:

There are two CVBS input connection possibilities: Front chinch (E5) and Rear Chinch In (E3). Both CVBS sources are connected direct to the STV 6410 and routed to Rear Out 1 and Rear Out 2 via the 75-Ohm driver BA 7623. Both CVBS output sockets are connected to BA 7623 in parallel. Independent of the input signal quality (CVBS, S-Video or Y/ UV) the digital board supplies also S-Video and Y/UV signals to the corresponding sockets.

S-Video Signals:

There are also two S-Video input connection possibilities: Front (E4) and Rear (E2) S-Video In which are connected to the pre-selector IC's BA 7652. One is used for Y, the other for Chroma switching. The output of the pre-selector switches is connected to the STV 6410, and then the signal is routed via the 75-Ohm driver BA 7623 to the Rear Out S-Video socket. Also the video quality will be S-Video, the digital board supplies also CVBS and Y/UV to the corresponding sockets.

Y/UV Signals:

The Y/UV In signal is routed direct to the digital board, there is no Y/UV IN -> Y/UV Out loop through in low power standby. As the digital board supplies only RGB signals, a RGB Y/UV matrix is used. This matrix consists of the operational amplifier TSH95 which generates the U and V signals according the formulas: 2U=B-0,338R-0,661G. 2V=R-0,838G-0,161B. Then the signals are routed to the UV Output sockets via the 75-Ohm driver BA 7623. The corresponding Y signal is coming from the digital board via the STV 6410. The 75 Ohm Y socket is driven by the 75-Ohm driver BA 7623 and finally connected to the of the Y/UV Output.

Detection of Status-Information

WSS on Y/C-Plug:

- Picture-Ratio-Information (16:9 or 4:3) on SVHSconnections is coded via the average DC-level of the Chroma-signal-line, detection is realised by using an analogue-input-port of the CC-C.
- ADC- value lower or equal 40h (4:3-picture-ratio delivered
- ADC-value greater 40h (16:9-picture-ratio available on
- Y/C-Rear is determined via Port40/AIN3 (Pin14) of CC (WSRI-line) and Port41/AIN4 (Pin15) is used for Y/C-Front (WSFI-line).

Generation of Status-Information

WSS on Y/C-Plug:

The appropriate DC-level on Chroma-signal-line for Y/C-Rear-Out is produced via Port57 (Pin10) of the CC-C (WSRO-line).

- 4:3 Picture-ratio supported on Y/C-Plug: Port57 set to 0
- 16:9 Picture-ratio supported on Y/C-Plug: Port57 set to

Audio routing Analogue board (Europe / Nafta)

General Description:

The Audio- I/O switching is realised by the STV6410 I/O switch.

By I²C Bus (SDA-0/SCL-0) it is possible to control all the Audio in- and outputs (for detailed Information we refer to the STV6410 routing overview).

Analog audio coming from DV-Board and second rear Cinch input is routed via MSP3415 to the STV 6410. After selecting the audio source via STV 6410, the signal must be transformed into the digital domain. For this, the UDA 1360TS (ADC) is responsible. An input-voltage of up to 2Vrms can be handled from the IC's. For further processing, the UDA 1360TS (ADC) delivers the data-in I2S format to the digital-board. After a certain delay the (processed) data come back from the digital board to the UDA 1328 (DAC). The UDA 1328 (DAC) transforms the I²S data back into the analog domain and feeds the signals direct to the MC33078 (OPV). From the MC33078 (OPV) the signals are delivered back to the STV 6410 and also direct to the 2nd rear out Cinch. The other outputs (Scart, Cinch) are supported by the STV 6410.

Detailed Description STV 6410:

The STV 6410 is an I²C bus controlled audio and video switch matrix, which is able to handle audio input signals up to 2 Vrms. The used outputs are equipped with internal level adjustment possibility. Low distortion and very good channel separation is a typical peculiarity of this IC. The output resistance is very low and the frequency bandwidth is up to 50 kHz.

Detailed Description UDA 1360:

The UDA 1360TS is a stereo Analog-to-Digital Converter employing bitstream conversion techniques.

The UDA supports the I²S-bus data format and the MSBjustified data format with word lengths of up to 20 bits. The IC supports also 2Vrms input signals and is designed for 3V3 supply voltage.

The device is able to handle system clocks of 256fs and

Typical THD+N at 0dB is -85dB and a S/N performance up to 97dB is possible.

Detailed Description UDA 1328:

The UDA1328 is a 6 channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.

The UDA 1328 supports the I²S-bus data format with word lengths of up to 24 bits.

Digital sound features can be controlled with the L3 interface. System clock can be set to 256fs or 384fs.

The Device also provides 2 high quality differential outputs. Typical THD+N at 0dB is -95dB and a S/N of up to 106dB is possible.

Supply voltage is 3V3.

Detailed Description MC 33078:

The MC33078 is a dual operational amplifier for audio applications.

It offers low voltage noise (4,5nV/√Hz) and high frequency performances (15MHz Gain Bandwidth product, 7V/s slew

In addition the MC33078 has a very low distortion (0,002%).

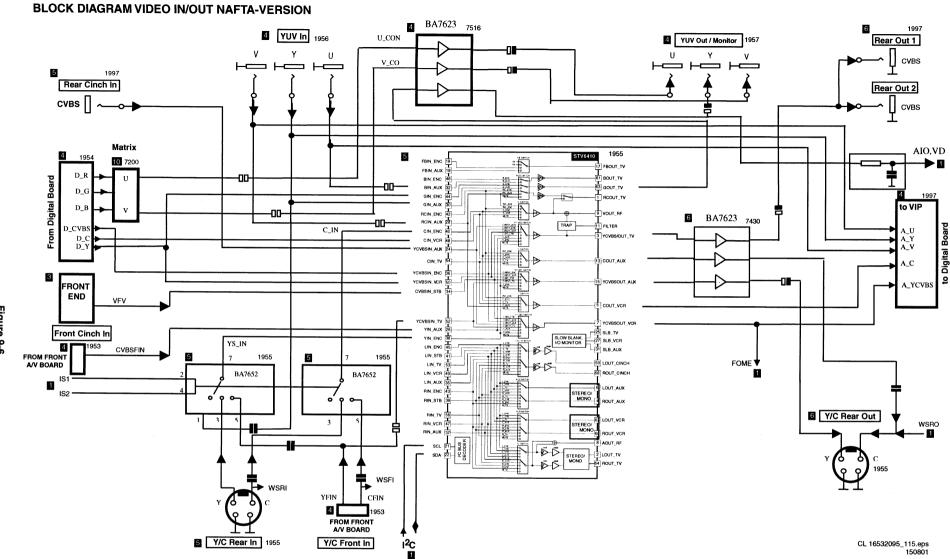
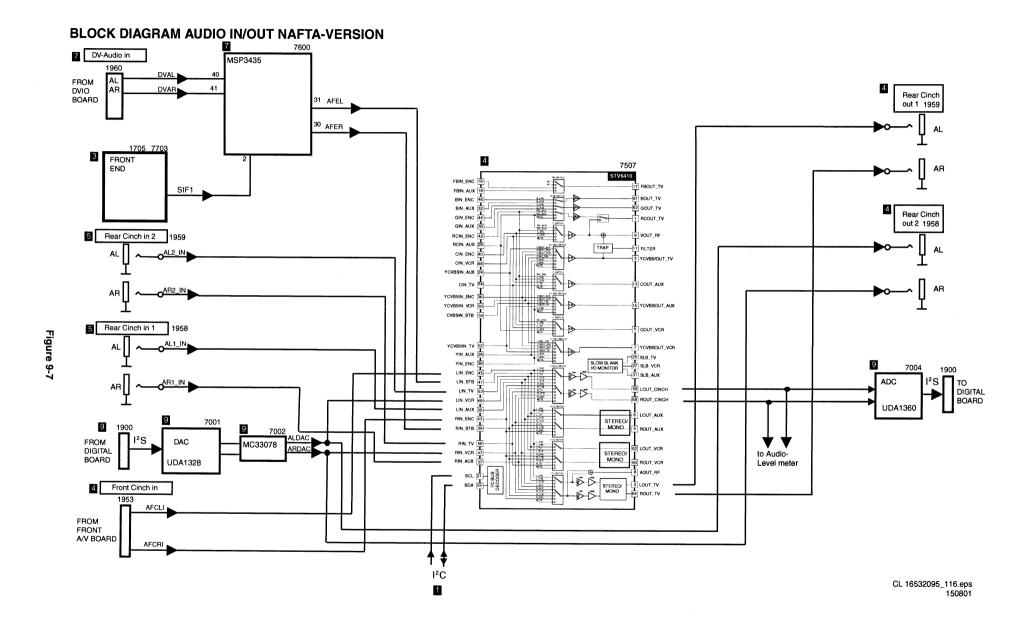


Figure 9-6



Digital Board

9.5.1 **Record Mode**

Video Part

Analog Video input signals CVBS, YC and UV are routed via the analog board to connector 1601 and sent to IC7552 SAA7118 (Video Input Processor). Digital video input signals (DV_IN_DATA(7:0)) are sent from the DIVIO board through the connector 1501 and further also to IC7552. IC7552 (VIP) decodes the analog video to digital video and processes the digital video to a digital video stream (CCIR656 format). This output stream (VIP_YUV[7:0]) goes to IC7410 SAA6750 (EMPIRE) and to IC7100 Versatile Stream Manager. The latter uses the data for VBI (vertical blanking interval) extraction.

IC7410 (EMPIRE) encodes the digital video stream into a MPEG2 video stream that is fed to IC7100 (VSM).

Audio Part

I2S audio are sent from the analog board to IC7703 DSP56362 (Audio Digital Signal Processor) via connector 1602. The DSP compresses I2S audio data into an AC3/ MPEG1 audio stream which is fed to IC7100 (VSM).

Front-End I2S

IC7100 (VSM) interfaces directly to the different hardware modules such as Basic Engine, MPEG encoder IC7410, MPEG decoder IC7202 (Sti5505) and buffers the data streams that are coming from or going to these hardware

In IC7100 (VSM), the video MPEG2 stream and the audio AC3/MPEG1 stream are multiplexed into a I2S packetized stream. The serial data are sent to the Basic Engine to be recorded.

Loop-Through

The multiplexed audio and video stream in the VSM is fed back via the parallel front-end interface to IC7202 (Sti5505). This IC decodes the MPEG stream into analog video and I2S audio. The video and audio signals are routed to the analog board via connectors 1601 and 1602. During recording, the recorded signal is present at the outputs of the analog board.

9.5.2 Playback Mode

During playback, the serial data from the Basic Engine pass through the VSM and are sent to the Sti5505 via the serial front-end I2S interface.

The Sti5505 is a MPEG & Audio/video decoder and has the following outputs:

To the analog board:

- analog video RGB, YC, CVBS
- I2S audio (PCM format)
- SPDIF audio (digital audio output)

To the Progressive scan board:

digital video YC(7:0).

9.5.3 S2B Interface

The S2B interface between the Host decoder Sti5505 and the Servo processor MACE3 controls the Basic Engine during record and playback mode.

9.5.4 System Clock

System clock of VSM and Sti5505 (27MHz) is generated by oscillator 7802.

9.5.5 Audio Clock

During record mode, the audio clock ACC_ACLK_OSC is generated by IC7806 (PLL) because then, the audio clock must be sychronized with the incoming video (VIP_FID) from the VIP

During playback mode, the audio clock ACC_ACLK_PLL is generated by the clock synthesizer IC7800 (MK2703). Both ACC_ACLK_OSC and ACC_ACLK_PLL are fed to the VSM. This IC selects the appropriate clock fo the audio decoder. From the incoming audio clocks, the VSM derives the I2S audio encoder clocks AE_BCLK and AE_WCLK.

9.5.6 ON/OFF

The digital board is not powered in standby mode. Control signal ION, coming from the analog board, will enable the PSU and power the digital board.

- ION = High: the digital board is in powered down standby mode
- ION = Low: the power supply to the digital board is enabled

9.5.7 RESET

Control signal IRESET_DIG, controlled by the microprocessor on the analog board is sent to the RESET LOGIC circuit.

- IRESET_DIG = Low in standby mode
- IRESET_DIG = High: the whole system is reset and the Digital board is waked up.

9.5.8 I2C Bus

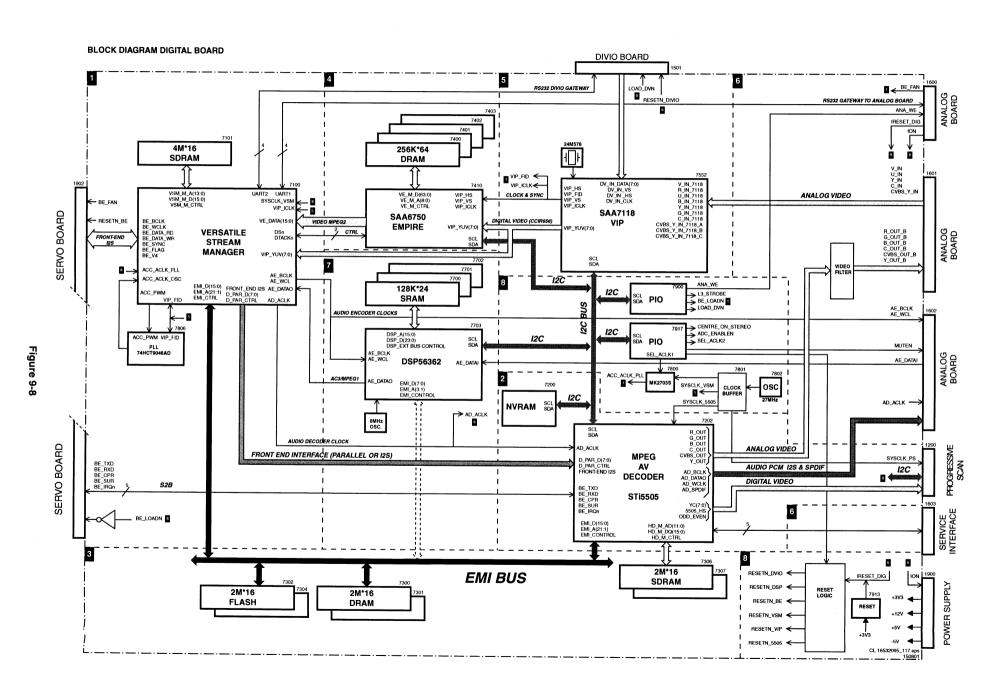
Sti5505 is master of the I2C bus. The following IC's are controlled by the I2C bus:

- IC7200 NVRAM
- IC7703 DSP56362
- IC7410 EMPIRE
- IC7552 VIP
- IC7900 Programmed Input/Output: LOAD_BE, LOAD_DVN, ANA WE, L3 STROBE.
- IC7917 Programmed Input/Output: CENTRE_ON_STEREO, ADC ENABLEN

9.5.9 EMI Bus

The following IC's are connected to the External Memory Interface bus (EMI) which functions as system bus:

- IC7302 and 7304: Flash memories which contain the application and diagnostic software
- IC7300 and 7301: DRAM's.
- IC7100: VSM
- IC7703: DSP56362: only for downloading the microclock into the IC
- IC7202: MPEG AV Decoder



9.6 **Divio Board**

9.6.1 **Short Description of the Module:**

The DVIO Module is a decoder for DV streams. The module is intended for the Philips DVDR1000/001 en DVDR1000/

171 DVD+RW recorders. Input is a stream from a DVcamcorder IEEE1394. Outputs are CCIR656 Video and Analog audio (L+R). A serial control interface is present. The following picture shows the location of the DVIO Module inside the DVDR set.

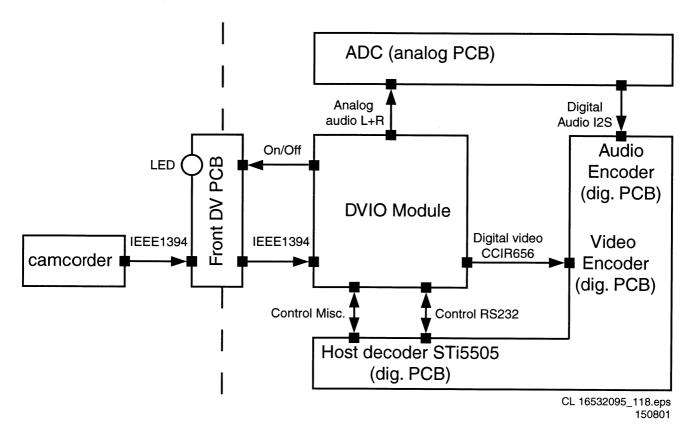


Figure 9-9

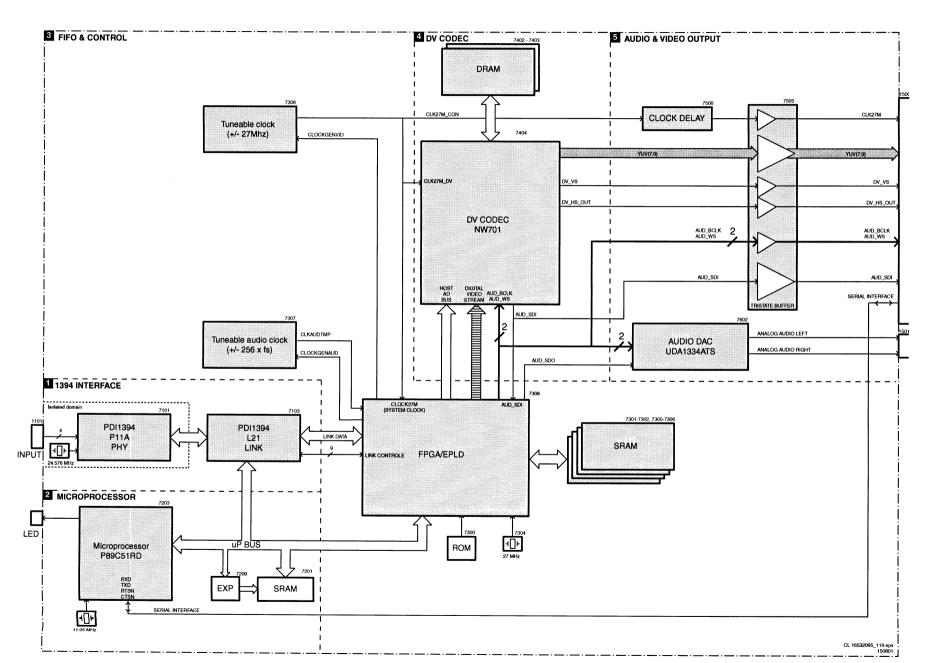


Figure 9-10

9.6.3 Functional Description

The DVIO module consists of the following blocks (see blockdiagram):

- 1. IEEE1394 Interface
 - PDI1394P11A (7101)
 - PDI1394L21(7103)
- 2. Micro-controller
 - 89C51RD(7203)
 - 32kb RAM(7201)
- 3. FIFO and Control
 - FPGA/EPLD(7308)
 - SRAM(7301, 7302, 7305, 7306)
 - Clock generation(7307, 7308)
 - Independently tuneable audio and video clock, implemented with FPGA and PLL
- 4. DV-Codec
 - NW701(7404)
 - DRAM(7402, 7403)
- 5. Audio & Video output
 - Audio DAC UDA1334ATS(7602)
 - Clock delay(7500)
 - Tristate buffer(7505)

IEEE1394 Interface

The 1394 interface consists of a PDI1394P11A physical layer and a PDI1394L21 link layer. The physical layer has its own isolated power supply. It has the following features:

- · S200 operation (200 megabit per second)
- One i.Link port (4 pin)
- 1nF isolation barrier between link and phy
- AV link port
- · Isolated power supply for phy

Micro-Controller

The 89C51RD processor has a 8051 cpu with the following extra features:

- 64 kilobyte of flash memory as program memory
- 1 kilobyte of internal data memory
- watchdog timer
- PCA outputs
- · Power control modes
- Speed allowed up to 33 MHz but used at 22.1184 MHz
- On board ISP(In Circuit Programming) functionality

ISP

By use of In Circuit Programming, it is possible to update the software of the DVIO board that is in the 89C51RD+. ISP can be made active by resetting the processor and keeping the ISPN pin low during reset. During ISP, the ISPN signal on the board has to be kept low. This because the ISPN signal not only drives the PSEN pin low, but will also put 12V instead of 5V on the VPP pin. When the ISP mode is active, the new program can be sent to the microprocessor through the serial port.

Fifo & Control

In decode mode, an isochronous AV-stream is flowing through the IEEE1394 Interface into the FPGA. The FPGA stores the data in a FIFO buffer (ping-pong buffer type, i.e. 2 buffers that can hold one whole frame each).

Reset

The FPGA controls the reset signals on the board. This has the advantage that it is possible to reset the board both from software and hardware.

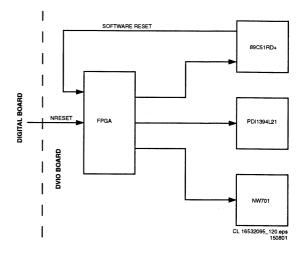


Figure 9-11

The board reset NRESET will reset the whole board, and the software reset can reset everything except the microprocessor itself. Power-on reset is implemented by adding pull-ups and pull-downs to the reset inputs of the devices. Since the FPGA will tri-state all the pins during configuration, reset is active during configuration time. After configuration of the FPGA, the reset signals are driven inactive. The NRESET signal is used to reset the DVIO board. After reset, the tri-state buffers to connector 1500 are disabled.

Clock Circuit

There are 2 clocks to consider in the system, this is the video clock and the audio clock. These two clocks do not have a relation, so these clocks must be considered independently. The video clock is approximately 27 MHz. When data is flowing from an external source that is supposed to have the same frequency, it does not have exactly the same clock. Because of this, buffers may under-run of over-run. Since the clock can not be directly recovered from the 1394 interface, there has to be another solution. This solution is a tuneable clock that is adjusted to the required frequency to process at the rate of the incoming data.

The hardware implementation of such a tuneable clock is as follows:

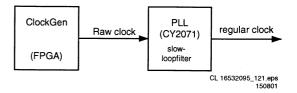


Figure 9-12

The same can be applied for the audio clock. For this clock, a frequency of 8.192 MHz, 11.2896 MHz or 12.228 MHz is required. This depends on the sample-rate of the audio signal.

DV Codec

The AV-data will go from the FIFO to the NW701. The NW701 decodes the stream into video data in 656 format and audio data in I2S format.

The microprocessor has the ability to read the status registers of the NW701 through the FPGA. By reading these registers, extra data from the DV stream, that is not decoded into audio or video, can be sent to the digital board using pin TXD of the serial interface. This data includes time stamp and some more.

Audio & Video Output

The audio I2S data are sent to audio DAC UDA1334. Analog audio left and right signals are connected to the analog board.

The tristate buffer enables the digital video stream to the Video Input Processor on the digital board when the DV source is selected.

The clock delay synchronizes the AV clock with the AV data at the output.

9.7 **Progressive Scan**

9.7.1 **Block Diagram**

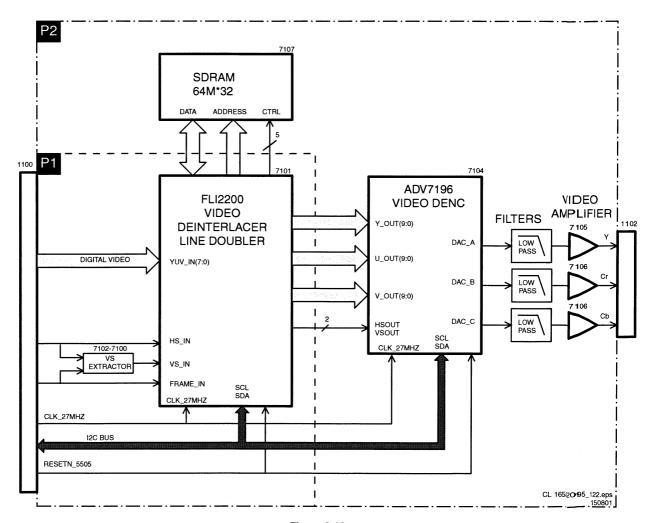


Figure 9-13

9.7.2 Description

The progressive scan module, used in the first generation DVD+RW player, is built around the SAGE Fli2200 deinterlacer / line doubler (7101). This I2C controlled deinterlacer uses a 64Mbit SDRAM (32bit x 2M) to perform high quality deinterlacing (meshing). The de-interlacer gets his digital YUV input data from the STi5505 (7202), located on the digital board. Via a 24-poled flex, digital video, power supply, reset and I2C is connected to the board. The format of the digital YUV input to the SAGE is CCIR656 with separated Hsync, Vsync and odd/even signal running on 27Mhz.

Because the STi5505 doesn't have a Vsync output the odd/ even output of this IC has to be translated to a Vsvnc signal. Some glue logic has been added to extract the vertical sync. The glue logic circuit consists of Flip-Flop IC 74HC74D (7102) and EXOR 74LVC86 (7100). The next diagram shows how the vertical sync is extracted.

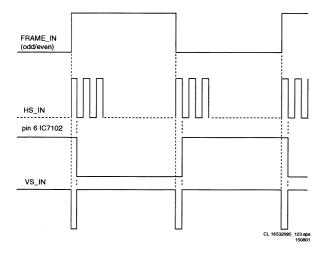


Figure 9-14

The output of the de-interlacer (4:4:4 progressive video) is fed to the Analog Devices AD7196 MacroVision compliant DENC (7104).

The YUV current output of the DENC is fed via a low pass filter to the single supply output opamps AD8061/8062 (7105-7106). The analog video is fed via a 7 poled flex to the analog board where the YUV 2FH cinch connectors are located.

The board uses as power supply 3.3V and 5V. The 2,5V power required for the SAGE is derived locally from the 3.3V with voltage regulator LF25C (7103).

IC's Analogue Board 9.8

9.8.1 IC7001: UDA1328T

Multi-channel filter DAC

UDA1328T

FEATURES

1.1 General

- 2.7 to 3.6 V power supply
- 5 V tolerant TTL compatible inputs
- Selectable control via L3 microcontroller interface or via static pin control
- · Multi-channel integrated digital filter plus non-inverting Digital-to-Analog Converter (DAC)
- Supports sample frequencies between 5 and 100 kHz
- Digital silence detection (output)
- Slave mode only applications
- · No analog post filtering required for DAC
- · Easy application.

1.2 Multiple format input interface

- I²S-bus, MSB-justified and LSB-justified format compatible (in L3 mode)
- I²S-bus and LSB-justified format compatible
- 1fs input format data rate.

1.3 **Multi-channel DAC**

- 6-channel DAC with power on/off control
- Digital logarithmic volume control via L3; volume can be set for each of the channels individually
- Digital de-emphasis for 32, 44.1, 48 and 96 kHz f_s via L3 and, for 32, 44.1 and 48 kHz in static mode
- · Soft or quick mute via L3
- Output signal polarity control via L3 microcontroller interface.

1.4 Advanced audio conpguration

- 6-channel line output (under L3 volume control)
- A stereo differential output (channel 1 and channel 2) for improved performance
- · High linearity, wide dynamic range, low distortion.

BITSTREAM CONVERSION

APPLICATIONS

This multi-channel DAC is eminently suitable for DVD-like applications in which 5.1 channel encoded signals are used.

3 **GENERAL DESCRIPTION**

The UDA1328 is a single-chip 6-channel DAC employing bitstream conversion techniques, which can be used either in L3 microcontroller mode or in static pin mode.

The UDA1328 supports the I²S-bus data format with word lengths of up to 24 bits, the MSB-justified data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 18, 20 and 24 bits.

All digital sound processing features can be controlled with the L3 interface e.g. volume control, selecting digital silence type, output polarity control and mute. Also system features such as power control, digital silence detection mode and output polarity control.

Under static pin control, via static pins, the system clock can be set to either 256fs or 384fs support, digital de-emphasis can be set, there is digital mute and the digital input formats can also be set.

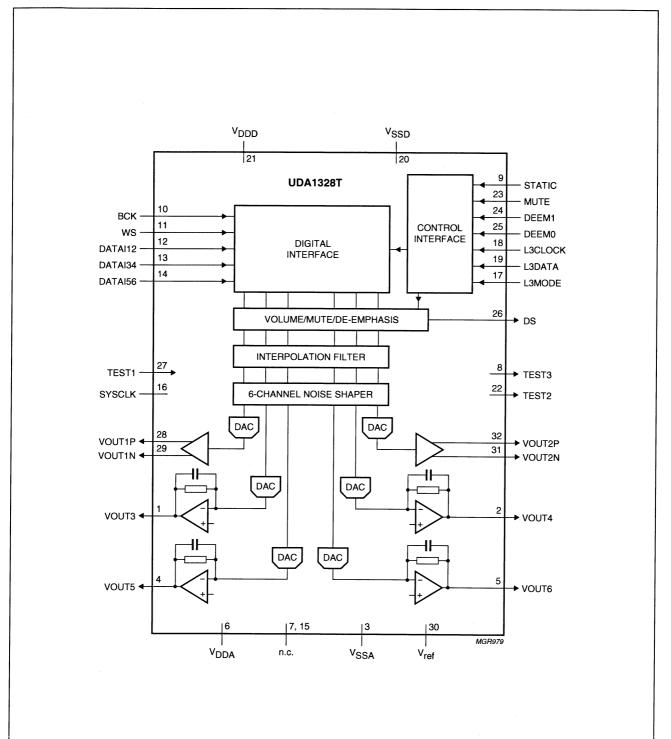
ORDERING INFORMATION

TYPE		PACKAGE		
NUMBER	NAME	DESCRIPTION	VERSION	
UDA1328T	SO32	plastic small outline package; 32 leads; body width 7.5 mm	SOT287-1	

Multi-channel filter DAC

UDA1328T

BLOCK DIAGRAM

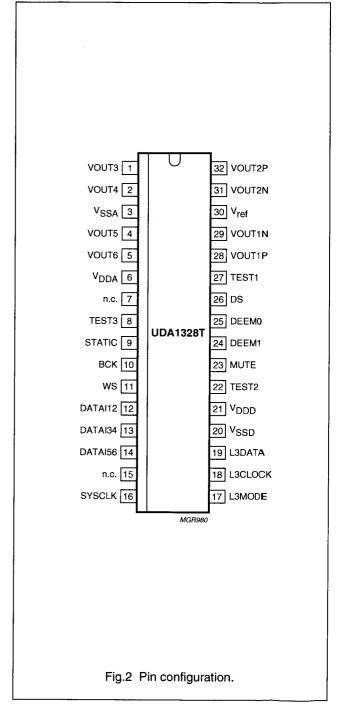


Multi-channel filter DAC

UDA1328T

PINNING

SYMBOL	PIN	DESCRIPTION	
VOUT3	1	channel 3 analog output	
VOUT4	2	channel 4 analog output	
V _{SSA}	3	analog ground	
VOUT5	4	channel 5 analog output	
VOUT6	5	channel 6 analog output	
V_{DDA}	6	analog supply voltage	
n.c.	7	not connected (reserved)	
TEST3	8	test output 3	
STATIC	9	static mode/L3 mode switch input	
BCK	10	bit clock input	
ws	11	word select input	
DATAI12	12	data input channel 1 and 2	
DATAI34	13	data input channel 3 and 4	
DATAI56	14	data input channel 5 and 6	
n.c.	15	not connected (reserved)	
SYSCLK	16	system clock: 256f _s , 384f _s , 512f _s and 768f _s	
L3MODE	17	L3 mode selection input	
L3CLOCK	18	L3 clock input	
L3DATA	19	L3 data input	
V _{SSD}	20	digital ground	
V_{DDD}	21	digital supply voltage	
TEST2	22	test output 2	
MUTE	23	static mute control input	
DEEM1	24	DEEM control 1 input (static mode)	
DEEM0	25	L3 address select (L3 mode)/DEEM control 0 input (static mode)	
DS	26	digital silence detect output	
TEST1	27	test input 1	
VOUT1P	28	channel 1 analog output P	
VOUT1N	29	channel 1 analog output N	
V _{ref}	30	DAC reference voltage	
VOUT2N	31	channel 2 analog output N	
VOUT2P	32	channel 2 analog output P	



Multi-channel Piter DAC

UDA1328T

FUNCTIONAL DESCRIPTION

System clock 8.1

The UDA1328 operates in slave mode only, this means that in all applications the system must provide the system clock. The system frequency is selectable. The options are 256f_s, 384f_s, 512f_s and 768f_s for the L3 mode and 256f_s or 384f_s for the static mode. The system clock must be frequency-locked to the digital interface signals.

It should be noted that the UDA1328 can operate from 5 to 100 kHz sampling frequency (f_s). However in 768f_s mode the sampling frequency must be limited to 55 kHz.

8.2 **Application modes**

Operating mode can be set with the STATIC pin, either to L3 mode (STATIC = LOW) or to the static mode (STATIC = HIGH). See Table 1 for pin functions in the static mode.

Table 1 Mode selection in the static mode

PIN	L3 MODE	STATIC MODE
L3CLOCK	L3CLOCK	clock select
L3MODE	L3MODE	SF1 ⁽¹⁾
L3DATA	L3DATA	SF0 ⁽¹⁾
MUTE	X ⁽²⁾	MUTE
DEEM1	X ⁽²⁾	DEEM1
DEEMO	L3ADR	DEEM0

Notes

- 1. SF1 and SF0 are the Serial Format inputs (2-bit).
- 2. X means that the pin has no function in this mode and can best be connected to ground.

8.3 Interpolation Piter (DAC)

The digital filter interpolates from 1 to 128fs by cascading a half-band filter and a FIR filter, see Table 2. The overall filter characteristic of the digital filters is illustrated in Fig.3, and the pass-band ripple is illustrated in Fig.4. Both figures are with a 44.1 kHz sampling frequency.

Table 2 Interpolation Piter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	0 to 0.45f _s	±0.02
Stop band	>0.55f _s	-55
Dynamic range	0 to 0.45f _s	>114
DC gain	_	-3.5

8.4 Digital silence detection

The UDA1328 can detect digital silence conditions in channels 1 to 6, and report this via the output pin DS. This function is implemented to allow for external manipulation of the audio signal in the absence of program material, such as muting or recorder control.

An active LOW output is produced at the DS pin if the channels selected via L3 or for all channels in static mode. carries all zeroes for at least 9600 consecutive audio samples (equals 200 ms for $f_s = 48 \text{ kHz}$). The DS pin is also active LOW when the output is digitally muted either via the L3 interface or via the STATIC pin.

In static mode all channels participate in the digital silence detection. In L3 mode control each channel can be set, either to participate in the digital silence detection or not.

8.5 Noise shaper

The 3rd-order noise shaper operates at 128fs. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

8.6 Filter stream DAC

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post-filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

The output voltage of the FSDAC scales proportionally with the power supply voltage.

8.7 Static mode

The UDA1328 is set to static mode by setting the STATIC pin HIGH. The function of 6 pins of the device now get another function as can be seen in Table 1.

8.7 1 SYSTEM CLOCK SETTING

In static mode pin 18 (L3CLOCK) is used to select the system clock setting. When pin 18 is LOW, the device is in $256f_s$ mode, when pin 18 is HIGH the device is in $384f_s$ mode.

Multi-channel filter DAC

UDA1328T

8.7.2 **DE-EMPHASIS CONTROL**

In static pin mode the pins DEEM0 and DEEM1 control the de-emphasis mode; see Table 3.

Table 3 De-emphasis control

DEEM MODE	DEEM1	DEEM0
No de-emphasis	0	0
32 kHz de-emphasis	0	1
44.1 kHz de-emphasis	1	0
48 kHz de-emphasis	1	1

8.7.3 DIGITAL INTERFACE FORMATS

In static pin mode the digital audio interface formats can be selected via pin 17 (SF1) and 19 (SF0). The following interface formats can be selected (see also Table 4):

- I²S-bus with data word length of up to 24 bits
- · LSB-justified format with data word length of 16, 20 or 24 bits.

Table 4 Input format selection in the static mode

INPUT FORMAT	SF1	SF0
l ² S-bus	0	. 0
LSB-justiPed 16bits	0	1
LSB-justiPed 20bits	1	0
LSB-justiPed 24bits	1	1

It should be noted that the digital audio interface holds that the BCK frequency can be 64 times the WS maximum frequency, or $f_{BCK} \le 64 \times f_{WS}$

8.8 L3 mode

The device is set to L3 mode by setting the STATIC pin to LOW. The device can then be controlled via the L3 microcontroller interface (see Chapter 9).

8.8.1 DIGITAL INTERFACE FORMATS

The following interface formats can be selected in the L3 mode:

- I²S-bus with data word length of up to 24 bits
- MSB-justified with data word length of up to 24 bits
- · LSB-justified format with data word length of 16, 18, 20 or 24 bits.

8.8.2 L3 ADDRESS

The UDA1328 can be addressed via the L3 microcontroller interface using one of two addresses. This is done in order to individually control the UDA1328 and other Philips DACs or CODECs via the same L3 bus.

The address can be selected using pin 25 (DEEM0) in L3 mode. When pin 25 is set LOW, the address is 000100. When pin 25 is set HIGH the address is 000101.

9.8.2 IC7004: UDA1360TS

Low-voltage low-power stereo audio ADC

UDA1360TS

FEATURES

General

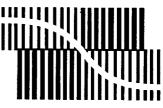
- · Low power consumption
- 2.4 to 3.6 V power supply
- Supports 256 and 384f_s system clock
- Supports sampling frequency range of 5 to 55 kHz
- Small package size (SSOP16)
- Integrated high-pass filter to cancel DC offset
- · Power-down mode
- Supports 2 V (RMS) input signals
- · Easy application
- · Non-inverting ADC plus decimation filter.

Multiple format output interface

- I²S-bus and MSB-justified format compatible
- Up to 20 significant bits serial output.

Advanced audio configuration

- · Stereo single-ended input configuration
- · High linearity, dynamic range and low distortion.



BITSTREAM CONVERSION

GENERAL DESCRIPTION

The UDA1360TS is a single chip stereo Analog-to-Digital Converter (ADC) employing bitstream conversion techniques. The low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates recording functions.

The UDA1360TS supports the I2S-bus data format and the MSB-justified data format with word lengths of up to 20 bits.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies				· · · · · · · · · · · · · · · · · · ·	<u> </u>	<u> </u>
V _{DDA}	analog supply voltage		2.4	3.0	3.6	V
V_{DDD}	digital supply voltage		2.4	3.0	3.6	V
I _{DDA}	analog supply current		_	9	_	mA
I _{DDD}	digital supply current		-	3.5	1-	mA
T _{amb}	operating ambient temperature		-40	-	+85	°C
ADC				-1	····	
V _{i(rms)}	input voltage (RMS value)	see Table 1	-	1.0	1-	V
(THD + N)/S	total harmonic distortion plus	at 0 dB	_	-85	-80	dB
	noise-to-signal ratio	at -60 dB; A-weighted	-	-37	-33	dB
S/N	signal-to-noise ratio	V _I = 0 V; A-weighted	_	97	-	dB
α _{cs}	channel separation		_	100	_	dB

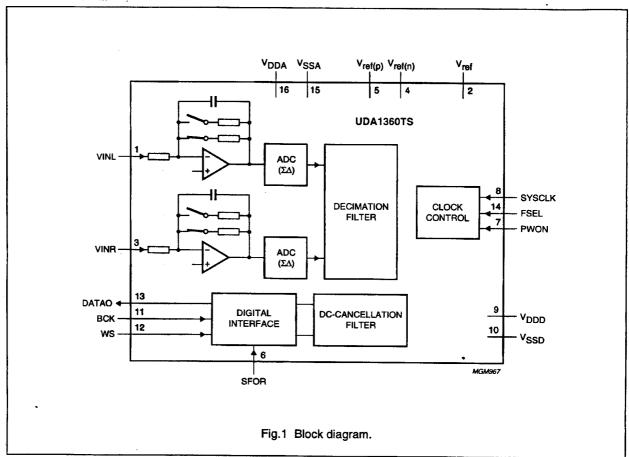
ORDERING INFORMATION

TYPE	PACKAGE					
NUMBER	NAME	DESCRIPTION	VERSION			
UDA1360TS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT369-1			

Low-voltage low-power stereo audio ADC

UDA1360TS

BLOCK DIAGRAM



Low-voltage low-power stereo audio ADC

UDA1360TS

PINNING

SYMBOL	PIN	DESCRIPTION
VINL	1	left channel input
V _{ref}	2	reference voltage
VINR	3	right channel input
V _{ref(n)}	4	ADC negative reference voltage
V _{ref(p)}	5	ADC positive reference voltage
SFOR	6	data format selection input
PWON	7	power control input
SYSCLK	8	system clock input 256 or 384fs
V_{DDD}	9	digital supply voltage
V _{SSD}	10	digital ground
BCK	11	bit clock input
WS	12	word selection input
DATAO	13	data output
FSEL	14	system clock frequency select
V _{SSA}	15	analog ground
V_{DDA}	16	analog supply voltage

FUNCTIONAL DESCRIPTION

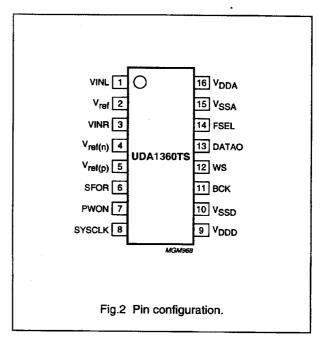
System clock

The UDA1360TS accommodates slave mode only, this means that in all applications the system devices must provide the system clock. The system frequency is selectable via the static FSEL pin, and the system clock must be locked in frequency to the digital interface input signals.

The options are 256fs (FSEL = LOW) and 384fs (FSEL = HIGH). The sampling frequency range is 5 to 55 kHz.

The BCK clock can be up to 128fs, or in other words the BCK frequency is 128 times the Word Select (WS) frequency or less: $f_{BCK} \le 128 \times f_{WS}$.

- 1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface.
- 2. For MSB justified formats it is important to have a WS signal with 50% duty factor.



Analog-to-Digital Converter (ADC)

The stereo ADC of the UDA1360TS consists of two 3rd-order Sigma-Delta modulators. They have a modified Ritchie-coder architecture in a differential switched capacitor implementation. The over-sampling ratio is 128.

The overall system gain is proportional to $\ensuremath{V_{DDA}}.$ The 0 dB input level is defined as that which gives a -1 dB FS digital output (relative to the full-scale swing). In addition, an input gain switch is incorporated with the above definitions.

The UDA1360TS front-end is equipped with a selectable 0 or 6 dB gain, in order to supports 2 V (RMS) input using a series resistor of 12 k Ω .

For the definition of the pin settings for 1 or 2 V (RMS) mode given in Table 1, it is assumed that this resistor is present as a default component.

If the 2 V (RMS) signal input is not needed, the external resistor should not be used.

Low-voltage low-power stereo audio ADC

UDA1360TS

Table 1 Application modes using input gain stage

RESISTOR (12 kΩ)	INPUT GAIN SWITCH	MAXIMUM INPUT VOLTAGE
Present	0 dB	2 V (RMS)
Present	6 dB	1 V (RMS)
Absent	0 dB	1 V (RMS)
Absent	6 dB	0.5 V (RMS)

Multiple format output interface

The UDA1360TS supports the following data output formats:

- I2S-bus with data word length of up to 20 bits
- MSB-justified serial format with data word length of up to 20 bits.

The output format can be set by the static SFOR pin. When SFOR is LOW, the I²S-bus is selected, when SFOR is set HIGH the MSB-justified format is selected.

The data formats are illustrated in Fig. 4. Left and right data channel words are time multiplexed.

Decimation filter

The decimation from $128f_s$ is performed in two stages. The first stage realizes 3rd-order sin x/x characteristic. This filter decreases the sample rate by 16. The second stage (an FIR filter) consists of 3 half-band filters, each decimating by a factor of 2.

Table 2 DC cancellation filter characteristics

ITEM	ITEM CONDITION	
Pass-band ripple		none
Pass-band gain		0
Stop band	>0.55f _s	-60
Droop	at 0.00045f _s	0.031
Attenuation at DC	at 0.00000036fs	>40
Dynamic range	0 to 0.45f _s	>110

Mute

On recovery from power-down, the serial data output DATAO is held LOW until valid data is available from the decimation filter. This time tracks with the sampling frequency:

$$t\,=\,\frac{12288}{f_s}\,=\,279~\text{ms}$$
 ; where $f_s=44.1~\text{kHz}.$

Power-down mode

The PWON pin can control the power saving together with the optional gain switch for 2 V (RMS) or 1 V (RMS) input. When the PWON pin is set LOW, the ADC is set to power-down. When PWON is set to HIGH or to half the power supply, then either 6 dB gain or 0 dB gain in the analog front-end is selected.

Application modes

The UDA1360TS can be set to different modes using two 3-level pins and one 2-level pin. The selection of modes is given in Table 3.

Table 3 Mode selection summary

PIN	V _{SS} •	1/2V _{DD}	V _{DD}
SFOR	I ² S-bus	test mode	MSB
PWON	power-down	0 dB gain	6 dB gain
FSEL	256f _s	_	384f _s

9.8.3 IC7430: BA7660FS

3-channel 75 Ω driver **BA7660FS**

The BA7660FS is a 75 Ω driver with a 6dB amplifier and three internal circuits, and provides 75 Ω drive of composite Y signals and C signals, as well as RGB signals. Each load is capable of driving two circuits, and a sag correction function reduces the capacitance of the output coupling capacitor.

The input voltage is within a range of 0V to 1.5V, enabling direct connection of ordinary D / A converter output. An internal power-saving circuit is also included which provides simultaneous muting on all three channels, and output pin shorting protection.

Applications

DVDs, set top boxes and other digital video devices

Features

- 1) Can be coupled directly to D / A converter output.
- 2) Operates at a low power consumption (115mW typ.).
- 3) Internal output muting circuit.
- 4) Internal power-saving circuit.
- 5) Internal output protection circuit.

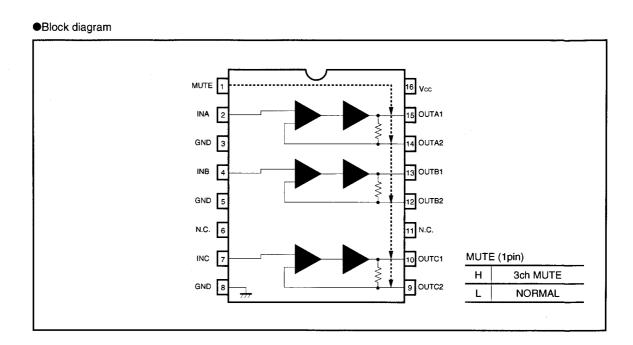
- 6) An internal sag correction function makes it possible to reduce the capacitance of the output coupling capacitor.
- 7) Each load is capable of driving two circuits.
- 8) The compact 16-pin SSOP-A package is used.

● Absolute maximum ratings (Ta = 25C)

Parameter	Symbol	Limits	Unit
Power supply voltage	Vcc	8	٧
Power dissipation	Pd	650	mW
Operating temperature	Topr	– 25 ~ + 75	°C
Storage temperature	Tstg	- 55 ~ + 125	°C

•Recommended operating conditions (Ta = 25C)

				r	
Parameter	Symbol	Min.	Тур.	Max.	Unit
Operating power supply voltage	Vcc	4.5	5.0	5.5	V



●Pin descriptions and input / output circuits

Pin. No	Pin name	IN	оит	Reference voltage	Equivalent circuit	Function
1	MUTE	К	_		15k	Muting control If MUTE (pin 1) is set to HIGH, muting is carried out simultaneously on all three channels.
2 4 7	INA INB INC	к	_	_		Signal input Input signals consist of composite video signals, Y signals, C signals, RGB, and others. The input level is within a range of 0 to 1.3 (min.) to 1.5 (typ.).
3 5 8	GND	-	_	ov	O	Ground
14 12 9 15 13 10	OUTA2 OUTB2 OUTC2 OUTA1 OUTB1 OUTC1		к	0.9V 0.95V	14pin 12pin 9pin 15pin 13pin 10pin	Signal output The signal output level is (0.9 + 2 × input voltage [V]). Pins 9, 12, and 14 are the pins for sag correction. If pins 10, 13, and 15 are set to 0.2V or less, the protective circuit is triggered and the power-saving mode is accessed.
16	Vcc		_	5.0V	→ Vcc	Power supply

STV6410

AUDIO/VIDEO SWITCH MATRIX

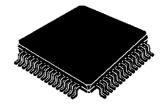
- I²C BUS CONTROL
- STANDBY MODE

VIDEO SECTION

- 5 CVBS INPUTS, 4 CVBS OUTPUTS (ONE WITH SELECTABLE CHROMATRAP FILTER)
- 5 Y/C INPUTS, 3 Y/C OUTPUTS
- 6dB GAIN ON ALL CVBS/Y AND C OUTPUTS
- 1 Y/C ADDER
- 2 RGB/FB INPUTS, 1 RGB/FB OUTPUT WITH 6dB ADJUSTABLE GAIN
- VIDEO MUTING ON ALL THE OUTPUTS
- 3 SLOW BLANKING INPUTS/OUTPUTS
- SYNC BOTTOM CLAMP ON ALL CVBS/Y AND RGB INPUTS, AVERAGE ON C INPUTS
- BANDWIDTH: 15MHz
- CROSSTALK: 60dB Typ.

AUDIO SECTION

- 5 STEREO INPUTS, 4 STEREO OUTPUTS (TWO WITH LEVEL ADJUSTMENT)
- MONO SOUND OUTPUT
- MONO SOUND CAPABILITY ON TV OUTPUTS
- AUDIO MUTING ON ALL THE OUTPUTS



TQFP64 (Plastic Quad Flat Pack)

ORDER CODE: STV6410D

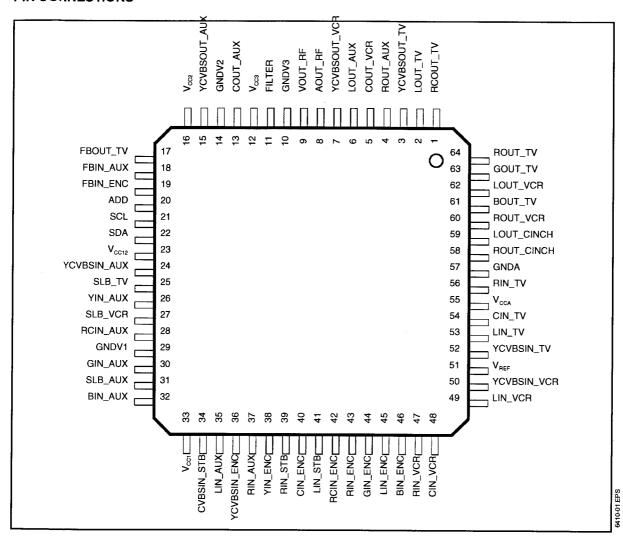
DESCRIPTION

The STV6410 is a highly integrated I²C bus-controlled audio and video switch matrix, optimized for use in digital set-top box applications. It provides all the audio and video routings required in a full three scart set-top box design. It is also fully pin compatible with STV6411, the two scart version.

GB 190

STV6410

PIN CONNECTIONS



PIN LIST

Pin Number	Symbol	Description	7
1	RCOUT_TV	Red/chroma Output, to TV Scart	1
2	LOUT_TV	Audio Left Output, to TV Scart	1
3	YCVBSOUT_TV	Y/CVBS Output, to TV scart	1
4	ROUT_AUX	Audio Right Output, to AUX Scart	1
5	COUT_VCR	Chroma Output, to VCR Scart	1
6	LOUT_AUX	Audio Left Output, to AUX Scart	1
7	YCVBSOUT_VCR	Y/CVBS Output, to VCR Scart	1
8	AOUT_RF	Audio (L+R) Output to RF Modulator	1
9	VOUT_RF	Video (CVBS) Output to RF Modulator	1
10	GNDV3	Video Switches Ground 3	1
11	FILTER	Chroma Trap Filter	1
12	V _{CCV3}	Video Switches Supply 3 (8V)	1
13	COUT_AUX	Chroma Output, to AUX Scart	1
14	GNDV2	Video Switches Ground 2	3410-01 TBI
15	YCVBSOUT_AUX	Y/CVBS Output, to AUX Scart	18

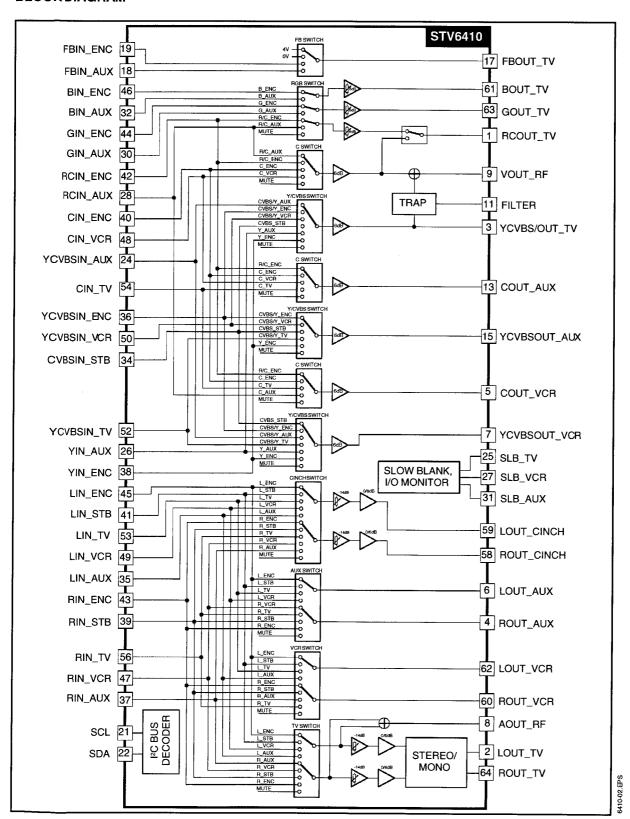
STV6410

PIN LIST (continued)

Pin Number	Symbol	Description			
16	Vccv2	Video Switches Supply 2 (8V)			
17	FBOUT_TV	Fast Blanking Output, to TV Scart			
18	FBIN_AUX	Fast Blanking Input, from AUX Scart			
19	FBIN_ENC	Fast Blanking Input, from Encoder			
20	ADD	I2C Bus IC Address Programmation			
21	SCL	I2C Bus Clock			
22	SDA	I2C Bus Data			
23	VCC12	Slow Blanking Power Supply (12V)			
24	YCVBSIN_AUX	Y/CVBS Input from AUX Scart			
25	SLB_TV	Slow Blanking Input/Ouput from TV			
26	YIN_AUX	Y Input, from AUX Scart			
27	SLB_VCR	Slow Blanking Input/Ouput from VCR			
28	RCIN_AUX	Red/Chroma Input, from AUX Scart			
29	GNDV1	Video Switches Ground 1			
30	GIN_AUX	Green Input, from AUX Scart			
31	SLB_AUX	Slow Blanking Input/Ouput from AUX			
32	BIN_AUX	Blue Input, from AUX Scart			
33	Vccv1	Video Switches Supply 1 (8V)			
34	CVBSIN_STB	CVBS Input from STB			
35	LIN_AUX	Audio Left Input, from AUX Scart			
36	YCVBSIN_ENC	Y/CVBS Input from Encoder			
37	RIN_AUX	Audio Right Input, from AUX Scart			
38	YIN_ENC	Y Input, from Encoder			
39	RIN_STB	Audio Right Input, from STB			
40	CIN_ENC	Chroma Input, from Encoder			
41	LIN_STB_	Audio Left Input, from STB			
42	RCIN_ENC	Red/Chroma Input, from Encoder			
43	RIN_ENC	Audio Right Input, from Encoder			
44	GIN_ENC	Green Input, from Encoder			
45	LIN_ENC	Audio Left Input, from Encoder			
46	BIN_ENC	Blue Input, from Encoder			
47	RIN_VCR	Audio Right Input, from VCR Scart			
48	CIN_VCR	Chroma Input, from VCR Scart			
49	LIN_VCR	Audio Left Input, from VCR			
50	YCVBSIN_VCR	Y/CVBS Input from VCR Scart			
51	V REF	Voltage Reference Decoupling			
52	YCVBSIN_TV	Y/CVBS Input, from TV Scart			
53	LIN_TV	Audio Left Input, from TV Scart			
54	CIN_TV	Chroma Input, from TV Scart			
55	V cca	Audio Switches Supply (8V)			
56	RIN_TV	Audio right input, from TV Scart			
57	GNDA	Audio Switches Ground			
58	ROUT_CINCH	Audio Right Output, to CINCH			
59	LOUT_CINCH	Audio Left Output, to CINCH			
60	ROUT_VCR	Audio Right Output, to VCR sCart			
61	BOUT_TV	Blue Output, to TV Scart			
62	LOUT_VCR	Audio Left Output, to VCR Scart			
63	GOUT_TV	Green Output, to TV Scart			
64	ROUT_TV	Audio Right Output, to TV Scart			

STV6410

BLOCK DIAGRAM



Multistandard Sound Processor Family

Release Note: Revision bars indicate significant changes to the previous edition. The hardware and software description in this document is valid for the MSP 34x5G version B8 and following versions.

1. Introduction

The MSP 34x5G family of single-chip Multistandard Sound Processors covers the sound processing of all analog TV standards worldwide, as well as the NICAM digital sound standards. The full TV sound processing, starting with analog sound IF signal-in, down to processed analog AF-out, is performed in a single chip. Figure 1-1 shows a simplified functional block diagram of the MSP 34x5G.

These TV sound processing ICs include versions for processing the multichannel television sound (MTS) signal conforming to the standard recommended by the Broadcast Television Systems Committee (BTSC). The DBX noise reduction, or alternatively, Micronas Noise Reduction (MNR) is performed alignment free.

Other processed standards are the Japanese FM-FM multiplex standard (EIA-J) and the FM-Stereo-Radio standard.

Current ICs have to perform adjustment procedures in order to achieve good stereo separation for BTSC and EIA-J. The MSP 34x5G has optimum stereo performance without any adjustments.

All MSP 34xxG versions are pin compatible to the MSP 34xxD. Only minor modifications are necessary to adapt a MSP 34xxD controlling software to the MSP 34xxG. The MSP 34x5G further simplifies controlling software. Standard selection requires a single I²C transmission only.

Note: The MSP 34x5G version has reduced control registers and less functional pins. The remaining registers are software-compatible to the MSP 34x0G. The pinning is compatible to the MSP 34x0G.

The MSP 34x5G has built-in automatic functions: The IC is able to detect the actual sound standard automatically (Automatic Standard Detection). Furthermore, pilot levels and identification signals can be evaluated internally with subsequent switching between mono/ stereo/bilingual; no I²C interaction is necessary (Automatic Sound Selection).

The MSP 34x5G can handle very high FM deviations even in conjunction with NICAM processing. This is especially important for the introduction of NICAM in China

The ICs are produced in submicron CMOS technology. The MSP 34x5G is available in the following packages: PSDIP64, PSDIP52, PMQFP44, PLQFP64, and PQFP80.

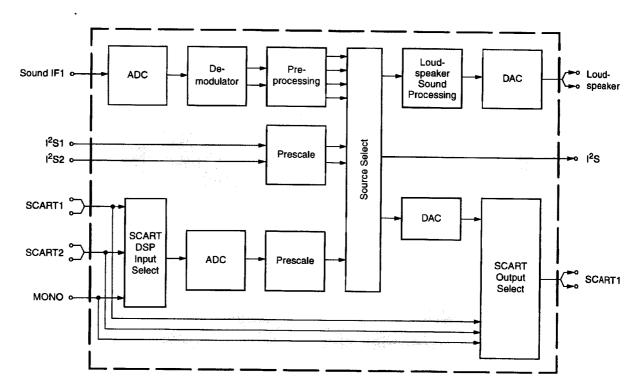


Fig. 1-1: Simplified functional block diagram of MSP 34x5G

Functional Description

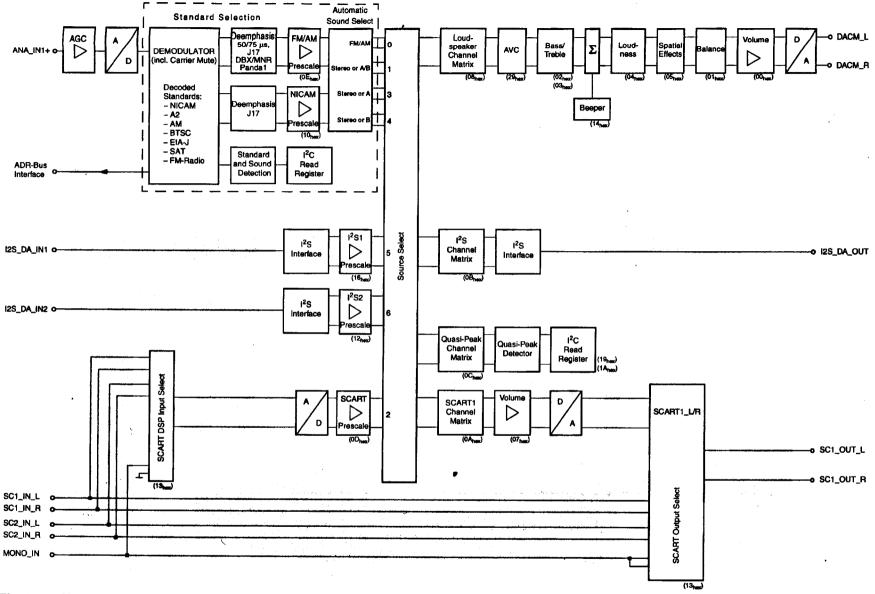


Fig. 2-1: Signal flow block diagram of the MSP 34x5G (input and output names correspond to pin names).

2.1. Architecture of the MSP 34x5G Family

Fig. 2-1 on page 8 shows a simplified block diagram of the IC. The block diagram contains all features of the MSP 3455G. Other members of the MSP 34x5G family do not have the complete set of features: The demodulator handles only a subset of the standards presented in the demodulator block; NICAM processing is only possible in the MSP 3415G and MSP 3455G (see dashed block in Fig. 2-1).

2.2. Sound IF Processing

2.2.1. Analog Sound IF Input

The input pins ANA_IN1+ and ANA_IN- offer the possibility to connect sound IF (SIF) sources to the MSP 34x5G. The analog-to-digital conversion of the preselected sound IF signal is done by an A/D-converter. An analog automatic gain circuit (AGC) allows a wide range of input levels. The high-pass filter formed by the coupling capacitor at pin ANA_IN1+ (see Section 7. "Appendix D: Application Information" on page 92) is sufficient in most cases to suppress video components. Some combinations of SAW filters and sound IF mixer ICs, however, show large picture components on their outputs. In this case, further filtering is recommended.

2.2.2. Demodulator: Standards and Features

The MSP 34x5G is able to demodulate all TV sound standards worldwide including the digital NICAM system. Depending on the MSP 34x5G version, the following demodulation modes can be performed:

A2-Systems: Detection and demodulation of two separate FM carriers (FM1 and FM2), demodulation and evaluation of the identification signal of carrier FM2.

NICAM-Systems: Demodulation and decoding of the NICAM carrier, detection and demodulation of the analog (FM or AM) carrier. For D/K-NICAM, the FM carrier may have a maximum deviation of 384 kHz.

Very high deviation FM-Mono: Detection and robust demodulation of one FM carrier with a maximum deviation of 540 kHz.

BTSC-Stereo: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, AM demodulation of the (L-R)-carrier and detection of the SAP subcarrier. Processing of the DBX noise reduction or Micronas Noise Reduction (MNR).

BTSC-Mono + SAP: Detection and FM demodulation of the aural carrier resulting in the MTS/MPX signal. Detection and evaluation of the pilot carrier, detection and FM demodulation of the SAP-subcarrier. Processing of the DBX noise reduction or Micronas Noise Reduction (MNR).

Japan Stereo: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Demodulation and evaluation of the identification signal and FM demodulation of the (L-R)-carrier.

FM-Satellite Sound: Demodulation of one or two FM carriers. Processing of high-deviation mono or narrow bandwidth mono, stereo, or bilingual satellite sound according to the ASTRA specification.

FM-Stereo-Radio: Detection and FM demodulation of the aural carrier resulting in the MPX signal. Detection and evaluation of the pilot carrier and AM demodulation of the (L-R)-carrier.

The demodulator blocks of all MSP 34x5G versions have identical user interfaces. Even completely different systems like the BTSC and NICAM systems are controlled the same way. Standards are selected by means of MSP Standard Codes. Automatic processes handle standard detection and identification without controller interaction. The key features of the MSP 34x5G demodulator blocks are

Standard Selection: The controlling of the demodulator is minimized: All parameters, such as tuning frequencies or filter bandwidth, are adjusted automatically by transmitting one single value to the STANDARD SELECT register. For all standards, specific MSP standard codes are defined.

Automatic Standard Detection: If the TV sound standard is unknown, the MSP 34x5G can automatically detect the actual standard, switch to that standard, and respond the actual MSP standard code.

Automatic Carrier Mute: To prevent noise effects or FM identification problems in the absence of an FM carrier, the MSP 34x5G offers a configurable carrier mute feature, which is activated automatically if the TV sound standard is selected by means of the STAN-DARD SELECT register. If no FM carrier is detected at one of the two MSP demodulator channels, the corresponding demodulator output is muted. This is indicated in the STATUS register.

2.2.3. Preprocessing of Demodulator Signals

The NICAM signals must be processed by a deemphasis filter and adjusted in level. The analog demodulated signals must be processed by a deemphasis filter, adjusted in level, and dematrixed. The correct deemphasis filters are already selected by setting the standard in the STANDARD SELECT register. The level adjustment has to be done by means of the FM/ AM and NICAM prescale registers. The necessary dematrix function depends on the selected sound standard and the actual broadcasted sound mode (mono, stereo, or bilingual). It can be manually set by the FM Matrix Mode register or automatically by the Automatic Sound Selection.

2.2.4. Automatic Sound Select

In the Automatic Sound Select mode, the dematrix function is automatically selected based on the identification information in the STATUS register. No I²C interaction is necessary when the broadcasted sound mode changes (e.g. from mono to stereo).

The demodulator supports the identification check by switching between mono-compatible standards (standards that have the same FM-Mono carrier) automatically and non-audible. If B/G-FM or B/G-NICAM is selected, the MSP will switch between these standards. The same action is performed for the standards: D/K1-FM, D/K2-FM, and D/K-NICAM. Switching is only done in the absence of any stereo or bilingual identification. If identification is found, the MSP keeps the detected standard.

In case of high bit-error rates, the MSP 34x5G automatically falls back from digital NICAM sound to analog FM or AM mono.

Table 2-1 summarizes all actions that take place when Automatic Sound Select is switched on.

To provide more flexibility, the Automatic Sound Select block prepares four different source channels of demodulated sound (Fig. 2-2). By choosing one of the four demodulator channels, the preferred sound mode can be selected for each of the output channels (loudspeaker, headphone, etc.). This is done by means of the Source Select registers.

The following source channels of demodulated sound are defined:

- "FM/AM" channel: Analog mono sound, stereo if available. In case of NICAM, analog mono only (FM or AM mono).
- "Stereo or A/B" channel: Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains both languages A (left) and B (right).

- "Stereo or A" channel: Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language A (on left and right).
- "Stereo or B" channel: Analog or digital mono sound, stereo if available. In case of bilingual broadcast, it contains language B (on left and right).

Fig. 2-2 and Table 2-2 show the source channel assignment of the demodulated signals in case of Automatic Sound Select mode for all sound standards.

Note: The analog primary input channel contains the signal of the mono FM/AM carrier or the L+R signal of the MPX carrier. The secondary input channel contains the signal of the 2nd FM carrier, the L-R signal of the MPX carrier, or the SAP signal.

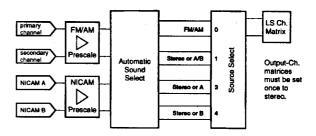


Fig. 2-2: Source channel assignment of demodulated signals in Automatic Sound Select Mode

2.2.5. Manual Mode

Fig. 2-3 shows the source channel assignment of demodulated signals in case of manual mode. If manual mode is required, more information can be found in Section 6.7. "Demodulator Source Channels in Manual Mode" on page 90.

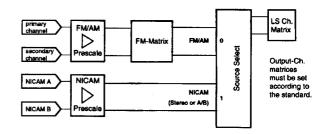


Fig. 2-3: Source channel assignment of demodulated signals in Manual Mode

2.3. Preprocessing for SCART and I²S Input Signals

The SCART and I2S inputs need only be adjusted in level by means of the SCART and I2S prescale regis-

2.4. Source Selection and Output Channel Matrix

The Source Selector makes it possible to distribute all source signals (one of the demodulator source channels or SCART) to the desired output channels (loudspeaker, etc.). All input and output signals can be processed simultaneously. Each source channel is identified by a unique source address.

For each output channel, the sound mode can be set to sound A, sound B, stereo, or mono by means of the output channel matrix.

If Automatic Sound Select is on, the output channel matrix can stay fixed to stereo (transparent) for demodulated signals.

2.5. Audio Baseband Processing

2.5.1. Automatic Volume Correction (AVC)

Different sound sources (e.g. terrestrial channels, SAT channels, or SCART) fairly often do not have the same volume level. Advertisements during movies usually have a higher volume level than the movie itself. This results in annoying volume changes. The AVC solves this problem by equalizing the volume level.

To prevent clipping, the AVC's gain decreases quickly in dynamic boost conditions. To suppress oscillation effects, the gain increases rather slowly for low level inputs. The decay time is programmable by means of the AVC register (see page 30).

For input signals ranging from -24 dBr to 0 dBr, the AVC maintains a fixed output level of -18 dBr. Fig. 2-4 shows the AVC output level versus its input level. For prescale and volume registers set to 0 dB, a level of 0 dBr corresponds to full scale input/output. This is

- SCART input/output 0 dBr = 2.0 V_{rms}
- Loudspeaker output 0 dBr = 1.4 V_{rms}

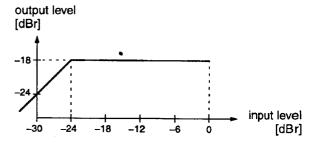


Fig. 2-4: Simplified AVC characteristics

2.5.2. Loudspeaker Outputs

The following baseband features are implemented in the loudspeaker output channels: bass/treble, loudness, balance, and volume. A square wave beeper can be added to the loudspeaker channel.

2.5.3. Quasi-Peak Detector

The quasi-peak readout register can be used to read out the quasi-peak level of any input source. The feature is based on following filter time constants:

attack time: 1.3 ms decay time: 37 ms

2.6. SCART Signal Routing

2.6.1. SCART DSP in and SCART Out Select

The SCART DSP Input Select and SCART Output Select blocks include full matrix switching facilities. To design a TV set with two pairs of SCART-inputs and one pair of SCART-outputs, no external switching hardware is required. The switches are controlled by the ACB user register (see page 34).

2.6.2. Stand-by Mode

If the MSP 34x5G is switched off by first pulling STANDBYQ low and then (after >1 µs delay) switching off DVSUP and AVSUP, but keeping AHVSUP ('Stand-by'-mode), the SCART switches maintain their position and function. This allows the copying from selected SCART-inputs to SCART-outputs in the TV set's stand-by mode.

In case of power on or starting from stand-by (switching on the DVSUP and AVSUP, RESETQ going high 2 ms later), all internal registers except the ACB register (page 34) are reset to the default configuration (see Table 3-5 on page 18). The reset position of the ACB register becomes active after the first I²C transmission into the Baseband Processing part. By transmitting the ACB register first, the reset state can be redefined.

2.7. I²S Bus Interface

The MSP 34x5G has a synchronous master/slave input/output interface running on 32 kHz.

The interface accepts two formats:

- 1. I²S_WS changes at the word boundary
- 2. I²S_WS changes one I²S-clock period before the word boundaries.

All I2S options are set by means of the MODUS and the I2S_CONFIG registers.

The I²S bus interface consists of five pins:

- 12S_DA_IN1,12S_DA_IN2: I²S serial data input: 16, 18....32 bits per sample
- I²S serial data output: 16, 18...32 bits per sample
- I2S CL: I²S serial clock
- I2S_WS: I²S word strobe signal defines the left and right

If the MSP 34x5G serves as the master on the I2S interface, the clock and word strobe lines are driven by the IC. In this mode, only 16 or 32 bits per sample can be selected. In slave mode, these lines are input to the IC and the MSP clock is synchronized to 576 times the I2S_WS rate (32 kHz). NICAM operation is not possible in slave mode.

An I²S timing diagram is shown in Fig. 4-28 on page 62.

2.8. ADR Bus interface

For the ASTRA Digital Radio System (ADR), the MSP 3405G, MSP 3415G, and MSP 3455G performs preprocessing such as carrier selection and filtering. Via the 3-line ADR-bus, the resulting signals are transferred to the DRP 3510A coprocessor, where the source decoding is performed. To be prepared for an upgrade to ADR with an additional DRP board, the following lines of MSP 34x5G should be provided on a feature connector:

- I2S_DA_IN1 or I2S_DA_IN2
- I2S_DA_OUT
- I2S_WS
- I2S_CL
- ADR_CL, ADR_WS, ADR_DA

For more details, please refer to the DRP 3510A data sheet.

2.9. Digital Control I/O Pins and **Status Change Indication**

The static level of the digital input/output pins D_CTR_I/O_0/1 is switchable between HIGH and LOW via the I²C-bus by means of the ACB register (see page 34). This enables the controlling of external hardware switches or other devices via I²C-bus.

The digital input/output pins can be set to high impedance by means of the MODUS register (see page 23). In this mode, the pins can be used as input. The current state can be read out of the STATUS register (see page 25).

Optionally, the pin D_CTR_I/O_1 can be used as an interrupt request signal to the controller, indicating any changes in the read register STATUS. This makes polling unnecessary; I²C-bus interactions are reduced to a minimum (see STATUS register on page 25 and MODUS register on page 23).

2.10.Clock PLL Oscillator and **Crystal Specifications**

The MSP 34x5G derives all internal system clocks from the 18.432 MHz oscillator. In NICAM or in I2S-Slave mode, the clock is phase-locked to the corresponding source. Therefore, it is not possible to use NICAM and I²S-Slave mode at the same time.

For proper performance, the MSP clock oscillator requires a 18.432-MHz crystal. Note, that for the phase-locked mode (NICAM, I²S slave), crystals with tighter tolerance are required.

4.2. Pin Connections and Short Descriptions

NC = not connected; leave vacant LV = if not used, leave vacant DVSS: if not used, connect to DVSS X = obligatory; connect as described in circuit diagram

AHVSS: connect to AHVSS

PQFP	PLQFP	Pin No.	PSDIP	PSDIP	Pin Name	Туре	Connection (if not used)	Short Description
80-pin	64-pin	44-pin	64-pin	52-pin				
1	64	_	8	-	NC		LV	Not connected
2	1	12	9	7	I2C_CL	IN/OUT	X	I ² C clock
3	2	13	10	8	I2C_DA	IN/OUT	X	I ² C data
4	3	14	11	9	12S_CL		LV	I ² S clock
5	4	15	12	10	12S_WS		LV	I ² S word strobe
6	5	16	13	11	I2S_DA_OUT		LV	I ² S data output
7	6	17	14	12	I2S_DA_IN1		LV	I ² S1 data input
8	7		15	13	ADR_DA		ĽV	ADR data output
9	8		16	14	ADR_WS		ΓΛ	ADR word strobe
10	9	18	17	15	ADR_CL		LV	ADR clock
11		 .	*****	-	DVSUP		Х	Digital power supply +5 V
12 [`]	_	***		-	DVSUP		X	Digital power supply +5 V
13	10	19	18	16	DVSUP		x	Digital power supply +5 V
14	_	20	-auje		DVSS		Х	Digital ground
15	-		_	-	DVSS		X	Digital ground
16	11		19	17	DVSS		Х	Digital ground
17	12	21	20	18	I2S_DA_IN2		ΓΛ	I ² S2-data input
18	13	_	21	19	NC		LV	Not connected
19	14		22		NC		LV	Not connected
20	15		23	_	NC		LV ·	Not connected
21	16	22	24	20	RESETQ	IN	X,	Power-on-reset
22				****	NC	·	LV	Not connected
23	-			_	NC		LV	Not connected
24	17	23	25	21	NC		LV	Not connected
25	18	24	26	22	NC		LV	Not connected

PQFP 80-pin	PLOFP 64-pin	Pin No.	PSDI P 64-pin	PSDIP 52-pin	Pin Name	Туре	Connection (if not used)	Short Description
26	19	44-pin 25	27	23	VREF2		x	Reference ground 2 high-voltage part
27	20	26	28	24	DACM_R	OUT	LV	Loudspeaker out, right
28	21	27	29	25	DACM_L	OUT	LV	Loudspeaker out, left
29	22	<u>-</u> -	30	_	NC		LV	Not connected
30	23	=	31	26	NC		LV	Not connected
31	24	_	32	_	NC		LV	Not connected
32	-			-	NC	:	LV	Not connected
33	25	-	33	27	NC		LV	Not connected
34	26	28	34	28	NC		LV	Not connected
35	27	29	35	29	VREF1		X	Reference ground 1 high-voltage part
36	28	30	36	30	SC1_OUT_R	OUT	LV	SCART 1 output, right
37	29	31	37	31	SC1_OUT_L	OUT	LV	SCART 1 output, left
38	30	32	38	32	NC		LV	Not connected
39	31	33	39	33	AHVSUP		Х	Analog power supply 8.0 V
40	32	34	40	34	CAPL_M		X	Volume capacitor MAIN
41		_	***	. —	NC		LV	Not connected
42	_	-	rejess.		NC		LV	Not connected
43		_	***	-	AHVSS		X ·	Analog ground
44	33	35	41	35	AHVSS		×	Analog ground
45	34	36	42	36	AGNDC		X	Analog reference voltag high-voltage part
46	-	-			NC		LV	Not connected
47	35	canca	43		NC .		ĽV	Not connected
48	36		44	-	NC		LV	Not connected
49	37	<u>-</u>	45	***	NC		LV	Not connected
50	38		46	37	NC		LV	Not connected
51	39		47	38	NC		LV	Not connected
52	40		48	-	NC		AHVSS	Analog Shield Grou nd
53	41	37	49	39	SC2_IN_L	IŅ	LV	SCART 2 input, let
54	42	38	50	40	SC2_IN_R	IN	LV	SCART 2 input, right

PQFP 80-pin	PLQFP 64-pin	Pin No. PMQFP 44-pin	SC 27 30	PSDIP 52-pin	Pin Name	Туре	Connection (if not used)	Short Description
55	43	39	51	_	ASG		AHVSS	Analog Shield Ground
56	44	40	52	41	SC1_IN_L	IN	LV	SCART 1 input, left
57	45	41	53	42	SC1_IN_R	IN	LV :	SCART 1 input, right
58	46	42	54	43	VREFTOP	÷	X	Reference voltage IF A/D converter
59			_		NC		LV	Not connected
60	47	43	55	44	MONO_IN	IN	LV	Mono input
61		_	_		AVSS		x	Analog ground
62	48	44	56	45	AVSS		х	Analog ground
63			-		NC		LV	Not connected
64	-	_		_	NC		LV	Not connected
65		-	*****		AVSUP		х	Analog power supply +5 V
66	49	1	57	46	AVSUP		X	Analog power supply +5 V
67	50	2	58	47	ANA_IN1+	IN	LV	IF input 1
68	51	3	59	48	ANA_IN-	IN	LV	IF common
69	52	-	60	49	NC		LV	Not connected
70	53	4	61	50	TESTEN	IN	X	Test pin
71	54	5	62	51	XTAL_IN	IN	X	Crystal oscillator
72	55	6	63	52	XTAL_OUT	OUT	X	Crystal oscillator
73	56	7	64	1	ТР		LV	Test pin
74	57		1	2	NC		ΓΛ	Not connected
75	58,		2	· ••••	NC		ΓΛ	Not connected
76	59		3	•••	NC		LV	Not connected
77	60	8	4	3	D_CTR_I/O_1	IN/OUT	ΓΛ	D_CTR_I/O_1
78	61	9	5	4	D_CTR_I/O_0	IN/OUT	LV	D_CTR_I/O_0
79	62	10	6	5	ADR_SEL	IN	Х	I ² C Bus address select
80	63	11	7	6	STANDBYQ	IN	Х	Standby (low-active)

9.8.6 IC7703: TDA9818

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

FEATURES

- 5 V supply voltage
- · Applicable for IFs (Intermediate Frequencies) of 38.9 MHz, 45.75 MHz and 58.75 MHz
- Gain controlled wide band Video IF (VIF)-amplifier (AC-coupled)
- True synchronous demodulation with active carrier regeneration (very linear demodulation, good intermodulation figures, reduced harmonics, excellent pulse response)
- Robustness for over-modulation better than 105% due to gated phase detector at L/L accent standard and PLL-bandwidth control at negative modulated standards
- VCO (Voltage Controlled Oscillator) frequency switchable between L and L accent (alignment external) picture carrier frequency
- VIF AGC (Automatic Gain Control) detector for gain control, operating as peak sync detector for B/G, peak white detector for L; signal controlled reaction time for L
- Tuner AGC with adjustable TakeOver Point (TOP)
- AFC (Automatic Frequency Control) detector without extra reference circuit

- · AC-coupled limiter amplifier for sound intercarrier signal
- Alignment-free FM PLL (Phase Locked Loop) demodulator with high linearity
- · SIF (Sound IF) input for single reference QSS (Quasi Split Sound) mode (PLL controlled); SIF AGC detector for gain controlled SIF amplifier; single reference QSS mixer able to operate in high performance single reference QSS mode and in intercarrier mode
- AM demodulator without extra reference circuit
- · Stabilizer circuit for ripple rejection and to achieve constant output signals
- ESD (Electrostatic Discharge) protection for all pins.

GENERAL DESCRIPTION

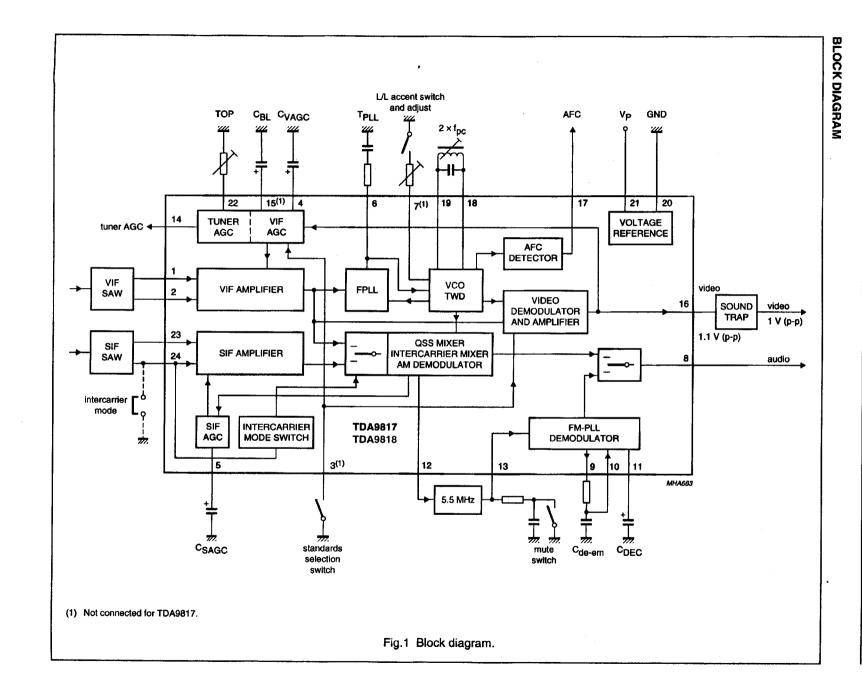
The TDA9817 is an integrated circuit for single standard vision IF signal processing and FM demodulation.

The TDA9818 is an integrated circuit for multistandard vision IF signal processing, sound AM and FM demodulation.

ORDERING INFORMATION

TYPE NUMBER		PACKAGE				
TIPENOMIBER	NAME	DESCRIPTION	VERSION			
TDA9817	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1			
TDA9818	SDIP24	plastic shrink dual in-line package; 24 leads (400 mil)	SOT234-1			

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

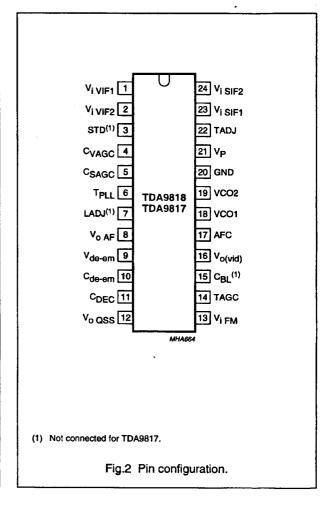


Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

PINNING

SYMBOL	PIN	DESCRIPTION
V _{I VIF1}	1	VIF differential input signal voltage 1
V _{i VIF2}	2	VIF differential input signal voltage 2
STD ⁽¹⁾	3	standard switch
C _{VAGC}	4	VIF AGC capacitor
CSAGC	5	SIF AGC capacitor
T _{PLL}	6	PLL loop filter
LADJ ⁽¹⁾	7	L/L accent switch and adjust
V _{o AF}	8	audio output
V _{de-em}	9	de-emphasis input
C _{de-em}	10	de-emphasis output
C _{DEC}	11	decoupling capacitor
V _{o QSS}	12	single reference QSS/intercarrier output voltage
V _{i FM}	13	sound intercarrier input voltage
TAGC	14	tuner AGC output
C _{BL} ⁽¹⁾	15	black level detector
V _{o(vid)}	16	composite video output voltage
AFC	17	AFC output
VCO1	18	VCO1 resonance circuit
VCO2	19	VCO2 resonance circuit
GND	20	ground
V _P	21	supply voltage
TADJ	22	tuner AGC takeover point adjust
V _{i SIF1}	23	SIF differential input signal voltage 1
V _{i SIF2}	24	SIF differential input signal voltage 2



Note

1. Not connected for TDA9817.

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

FUNCTIONAL DESCRIPTION

The integrated circuit comprises the functional blocks as shown in Fig.1:

- · Vision IF amplifier and VIF AGC detector
- Tuner AGC
- Frequency Phase Locked Loop detector (FPLL)
- VCO, Travelling Wave Divider (TWD) and AFC
- Video demodulator and amplifier
- SIF amplifier and SIF AGC
- Single reference QSS mixer
- · AM demodulator
- FM-PLL demodulator
- · AF (Audio Frequency) signal processing
- · Internal voltage stabilizer.

Vision IF amplifier and VIF AGC detector

The vision IF amplifier consists of three AC-coupled differential amplifier stages. Each differential stage comprises a feedback network controlled by emitter degeneration.

The AGC detector generates the required VIF gain control voltage for constant video output by charging/discharging the AGC capacitor. Therefore for negative video modulation the sync level and for positive video modulation the peak white level of the video signal is detected. In order to reduce the reaction time for positive modulation, where a very large time constant is needed, an additional level detector increases the discharging current of the AGC capacitor (fast mode) in the event of a decreasing VIF amplitude step. The additional level information is given by the black-level detector voltage.

Tuner AGC

The AGC capacitor voltage is converted to an internal IF control signal, and is fed to the tuner AGC to generate the tuner AGC output current at pin TAGC (open-collector output). The tuner AGC takeover point can be adjusted at pin TADJ. This allows to match the tuner to the SAW filter in order to achieve the optimum IF input level.

Frequency Phase Locked Loop detector (FPLL)

The VIF-amplifier output signal is fed into a frequency detector and into a phase detector via a limiting amplifier. During acquisition the frequency detector produces a DC current proportional to the frequency difference between the input and the VCO signal. After frequency lock-in the phase detector produces a DC current proportional to the

phase difference between the VCO and the input signal. The DC current of either frequency detector or phase detector is converted into a DC voltage via the loop filter. which controls the VCO frequency. In the event of positive modulated signals the phase detector is gated by composite sync in order to avoid signal distortion for overmodulated VIF signals.

VCO, Travelling Wave Divider (TWD) and AFC

The VCO operates with a resonance circuit (with L and C in parallel) at double the PC frequency. The VCO is controlled by two integrated variable capacitors. The control voltage required to tune the VCO from its free-running frequency to actually double the PC frequency is generated by the frequency-phase detector (FPLL) and fed via the loop filter to the first variable capacitor. This control voltage is amplified and additionally converted into a current which represents the AFC output signal. At centre frequency the AFC output current is equal to zero.

For TDA9818: the VCO centre frequency can be decreased (required for L accent standard) by activating an additional internal capacitor. This is achieved by using the L accent switch. In this event the second variable capacitor can be controlled by a variable resistor at the L accent switch for setting the VCO centre frequency to the required L accent value.

The oscillator signal is divided by 2 with a TWD which generates two differential output signals with a 90 degree phase difference independent of the frequency.

Video demodulator and amplifier

The video demodulator is realized by a multiplier which is designed for low distortion and large bandwidth. The vision IF input signal is multiplied with the 'in phase' signal of the travelling wave divider output. In the demodulator stage the video signal polarity can be switched in accordance with the TV standard.

The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the video amplifier. The video amplifier is realized by an operational amplifier with internal feedback and high bandwidth. A low-pass filter is integrated to achieve an attenuation of the carrier harmonics for B/G and L standard. The standard dependent level shift in this stage delivers the same sync level for positive and negative modulation. The video output signal at Vo(vid) is 1.1 V (p-p) for nominal vision IF modulation, in order to achieve 1 V (p-p) at sound trap output.

Single/multistandard VIF/SIF-PLL and FM-PLL/AM demodulators

TDA9817; TDA9818

SIF amplifier and SIF AGC

The sound IF amplifier consists of two AC-coupled differential amplifier stages. Each differential stage comprises a controlled feedback network provided by emitter degeneration.

The SIF AGC detector is related to the SIF input signal (average level of AM or FM carrier) and controls the SIF amplifier to provide a constant SIF signal to the AM demodulator and single reference QSS mixer. At L standard (AM sound) the SIF AGC reaction time is set to 'slow' for nominal video conditions. But with a decreasing VIF amplitude step the SIF AGC is set to 'fast' mode controlled by the VIF AGC detector. In FM mode this reaction time is always 'fast'.

Single reference QSS mixer

The single reference QSS mixer is realized by a multiplier. The SIF amplifier output signal is fed to the single reference QSS mixer and converted to intercarrier frequency by the regenerated picture carrier (VCO). The mixer output signal is fed via a high-pass for attenuation of the video signal components to the output pin 12. With this system a high performance hi-fi stereo sound processing can be achieved.

For a simplified application without a sound IF SAW filter the single reference QSS mixer can be switched to the intercarrier mode by connecting pin 24 to ground. In this mode the sound IF passes the vision IF SAW filter and the composite IF signal is fed to the single reference QSS mixer. This IF signal is multiplied with the 90 degree TWD output signal for converting the sound IF to intercarrier frequency. This composite intercarrier signal is fed to the output pin 12, too. By using this quadrature detection, the low frequency video signals are removed.

AM demodulator

The AM demodulator is realized by a multiplier. The modulated SIF amplifier output signal is multiplied in phase with the limited (AM is removed) SIF amplifier output signal. The demodulator output signal is fed via an integrated low-pass filter for attenuation of the carrier harmonics to the AF amplifier.

FM-PLL demodulator

The FM-PLL demodulator consists of a limiter and an FM-PLL. The limiter provides the amplification and limitation of the FM sound intercarrier signal. The result is high sensitivity and AM suppression. The amplifier

consists of 7 stages which are internally AC-coupled in order to minimize the DC offset.

Furthermore the AF output signal can be muted by connecting a resistor between the limiter input pin 13 and ground.

The FM-PLL consists of an integrated relaxation oscillator, an integrated loop filter and a phase detector. The oscillator is locked to the FM intercarrier signal, output from the limiter. As a result of locking, the oscillator frequency tracks with the modulation of the input signal and the oscillator control voltage is superimposed by the AF voltage. The FM-PLL operates as an FM demodulator.

AF signal processing

The AF amplifier consists of two parts:

- 1. The AF pre-amplifier for FM sound is an operational amplifier with internal feedback, high gain and high common mode rejection. The AF voltage from the PLL demodulator, by principle a small output signal, is amplified by approximately 33 dB. The low-pass characteristic of the amplifier reduces the harmonics of the intercarrier signal at the sound output terminal pin 9 at which the de-emphasis network for FM sound is applied. An additional DC control circuitis implemented to keep the DC level constant. independent of process spread.
- 2. The AF output amplifier (10 dB) provides the required output level by a rail-to-rail output stage. This amplifier makes use of an input selector for switching to AM, FM de-emphasis or mute state, controlled by the standard switching voltage and the mute switching voltage.

Internal voltage stabilizer

The bandgap circuit internally generates a voltage of approximately 1.25 V, independent of supply voltage and temperature. A voltage regulator circuit, connected to this voltage, produces a constant voltage of 3.6 V which is used as an internal reference voltage.

9.8.7 IC7803: TMP93C071

CMOS 16-Bit Microcontroller TMP93C071F

Outline and Feature

TMP93C071F is a high-speed advanced 16-bit microcontroller developed for application with VCR system control, software servo motor control and timer control.

In addition to basics such as I/O ports, the TMP93C071F has high-speed/high-precision signal measuring circuit, PWM (Pulse-Width-Modulator) and high-precision real timing pulse generator.

The device characteristics are as follows:

- (1) Original 16-bit CPU (900L_CPU)
 - TLCS-90 instruction mnemonic upward compatible
 - · 16 Mbyte linear address space
 - · General-purpose registers and register bank system
 - 16-bit multiplication/division and bit transfer/arithmetic instructions
 - High-speed micro DMA: 4 channels (1.6 µs / 2 byte at 20 MHz)
- Minimum instruction execution time: 200 ns at 20 MHz
- (3)Internal ROM: ROMless
- (4) Internal RAM: 8 Kbyte
- (5) External memory expansion
 - · Can be expanded up to 16 Mbyte (for both programs and data)
 - AM8/16 pin (select the external data bus width)
 - · Can be mixed 8 and 16bit external data buses.
 - ... Dynamic data bus sizing.
- 20-bit time-base-counter (TBC)
 - free running counter
 - · accuracy: 100 ns (at 20 MHz)
 - · overflow: 105 ms (at 20 MHz)
- 8-bit timer (TC0): 1 channel
 - · for CTL linear time counter
- (8)16-bit timer (TC1-5): 5 channels
 - · C-sync count, capstan FG count, general: (3 channels)
- (9) Timing pulse generator (TPG): 2 channels
 - (16-bit timing data + 6-bit-output data) with 8-stages FIFO: 1 channel
 - (16-bit timing data + 4-bit-output data): 1 channel
 - · accuracy: 400 ns (at 20 MHz)
- (10) Pulse width modulation outputs (PWM)
 - 14-bit PWM: 3 channels (for controlling capstan, drum and tuner)
 - 8-bit PWM: 9 channels (for controlling volume)
 - carrier frequency: 39.1 kHz (at 20 MHz)

980910EBP1

• For a discussion of how the reliability of microcontrollers can be predicted, please refer to Section 1.3 of the chapter entitled Quality and Reliability Assurance / Handling Precautions.

• TOSHIBA is continually working to improve the quality and the reliability of its products. Nevertheless, semiconductor devices in general can malfunction or fail due to their inherent electrical sensitivity and vulnerability to physical stress. It is the responsibility of the buyer, when utilizing TOSHIBA products, to observe standards of safety, and to avoid situations in which a malfunction or failure of a TOSHIBA product could cause loss of human life, bodily injury or damage to property. In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent products specifications. Also, please keep in mind the precautions and conditions set forth in the TOSHIBA Semiconductor Reliability Handbook.

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The information contained herein is subject to change without notice.

```
(11) 24-bit time base counter capture circuit (Capture 0)

    (18-bit timing data + 6-bit trigger data) with 8-stages FIFO: 1 channel

    capture input sources: Remote-control-input (RMTIN), V-sync, CTL, Drum-PG,

                                      general (1 channel)

    accuracy: 400 ns (at 20 MHz)

(12) 17-bit time base counter capture circuit (Capture 1/2)
             • (16-bit timing data + 1-bit trigger data): 2 channel
             · capture input sources: Drum-FG, Capstan-FG

 accuracy: 100 ns (at 20 MHz)

(13) VISS/VASS detection circuit (VISS/VASS)
             · CTL duty detection

    VASS data 16-bit latch

(14) Composite-sync-signal (C-sync) input (C-sync In)

    Vertical-sync-signal (V-sync) separation (V-sepa)

(15) Head Amp switch/Color Rotary control (HA/CR)
(16) Pseudo-V/H generator (PV/PH)
(17) 8-bit A/D converter (ADC): 16 channels

    Conversion speed: 95states (9.5 µs at 20 MHz)

(18) Serial bus I/F
             • 8-bit synchronous (SIO0, 1): 2 channels
             • UART: 1 channel

    I<sup>2</sup>CBUS: 1 channel/2 ports

                               Multi - Master function/Master transfer with micro DMA.
(19) Watch dog timer (WDT)
(20) Interrupt controller (INTC)
             • CPU: 2 sources • • • SWI instruction, and illegal instruction
             • Internal: 20 sources 7-level priority can be set.
             · External: 5 sources-
(21) I/O ports

    57 I/O ports (multiplexed functional pins)

             • 8 Input ports (P40/AIN3-P47/AIN10: These pins are used as analog input for
                                                    A/D converter.)
             • 4 Output ports (P24/A20-P27/A23: These pins are also used as address bus outputs.)
(22) Standby function: 4 halt modes (RUN, IDLE2, IDLE1, STOP)
(23) System clock function
             • Dual clock operation 20 MHz (High-speed: normal)/32 kHz(Low-speed: slow)
                               17-bit Real Time Counter built in
(24) Operating Voltage

    Vcc = 2.7 to 5.5 V (at 32 kHz)

    Vcc = 4.5 to 5.5 V (at 20 MHz)

(25) Package

    120 pin QFP 28 mm × 28 mm (Pin pitch: 0.8 mm)
```

Type name QFP120-P-2828-0.80A

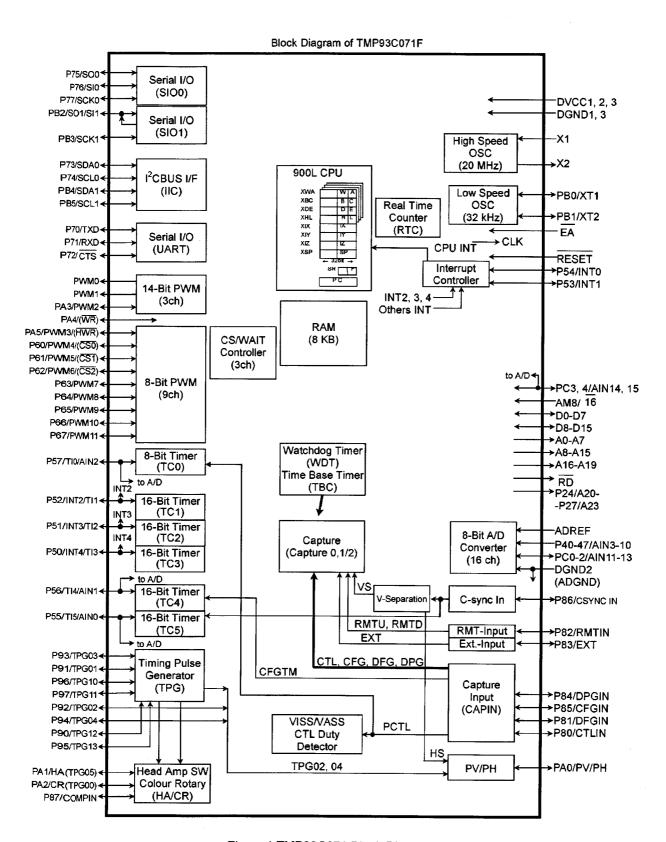


Figure 1 TMP93C071 Block Diagram

2. Pin Assignment And Functions

The assignment of input and output pins for the TMP93C071, their names and functions are described below.

2.1 Pin Assignment

Figure 2.1.1 shows pin assignment of the TMP93C071.

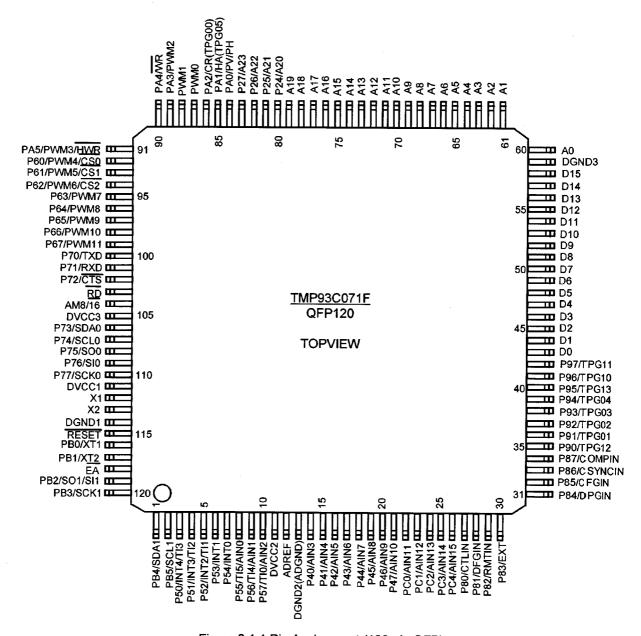


Figure 2.1.1 Pin Assignment (120-pin QFP)

2.2 Pin Names and Functions

The names of input/output pins and their functions are described below.

Table 2.2.1 Pin Names and Function (1/5)

Pin name	Number of pins	1/0	Functions
D0 to D15	16	I/O (3-state)	data: 0 to 15 for data bus
A0 to A19	20	Output	Address: 0 to 19 for address bus
A20 to A23/	4	Output	Address: 20 to 23 for address bus
P24 to P27		Output	Port 2: Output port
RD	1	Output	Read: strobe signal for reading external memory
AM8/16	1	Input	data bus width select input (only 8 bit or 8 bit/16 bit)
PC3, 4/ 16	2	1/0	Port C3, 4: I/O port that allows selection of I/O on a bit basis.
AIN14, 15		Input	Analog Input: Analog input signal for A/D converter
ĒĀ	1	Input	External access: Always set to 0
RESET	1	Input	Reset: Initializes LSI.(with pull-up R)
X1/X2	2	1/0	High Frequency Oscillator connecting pins (20 MHz)
PB0/	1	1/0	Port B0: I/O port (Open Drain Output)
XT1		Input	Low Frequency Oscillator connecting pin (32 kHz)
PB1/	1	1/0	Port B1: I/O port (Open drain Output)
XT2		Output	Low Frequency Oscillator connecting pin
ADREF	1	Input	A/D reference Voltage input
P40 to P47/	8	Input	Port 4: Input ports
AIN3 to AIN10		Input	Analog input: Analog input signal for A/D converter
PC0 to PC2/	3	I/O	Port C: PC0 to PC2 I/O port that allows selection of I/O on a bit basis.
AIN11 to AIN13		Input	Analog input: Analog input signal for A/D converter
P57/	1	I/O	Port 57: I/O port
TI0/		Input	8-bit timer0 (TC0) Input 0
	İ	(schmitt)	
AIN2		Input	Analog input: Analog input signal for A/D converter
P56/	1	1/0	Port 56: I/O port
TI4/		Input	16-bit timer4 (TC4) Input 4
	l	(schmitt)	
AIN1		Input	Analog input: Analog input signal for A/D converter
P55/	1	1/0	Port 55: I/O port
TI5/		Input	16-bit timer5 (TC5) Input 5
		(schmitt)	
AIN0		Input	Analog input: Analog input signal for A/D converter
P54/	1	1/0	Port 54: I/O port
INTO		input	External Interrupt request input 0: Rising edge/ Level selectable
		(schmitt)	
P53/	1		Port 53: I/O port
INT1		Input	External Interrupt request input 1: Rising edge/ Level selectable
		(schmitt)	
P52/	1	1/0	Port 52: I/O port
INT2/		Input	External Interrupt request input 2 Rising edge/Falling edge selectable
Tl1		Input	→
		(schmitt)	16-bit timer1(TC1) Input 1

		Table 2.2	.1 Pin Names and Function (2/5)
Pin name	Number of pins	1/0	Functions
P51/	1	1/0	Port 51: I/O port
INT3/		Input	External Interrupt request input 3 Rising edge/Falling edge selectable
Ti2		Input	√ ~_
		(schmitt)	16-bit timer2 (TC2) Input 2
P50/	1	1/0	Port 50: I/O port
INT4/	.	Input	External Interrupt request input 4 Rising edge/Falling edge selectable
TI3		Input	√ ¬
		(schmitt)	16-bit timer3 (TC3) Input 3
PWM0	1	Output	PWM (14 bit) output 0: PWM0 output
		3-state	push/pull or open drain output selectable
		Open Drain	
PWM1	1	Output	PWM (14 bit) output 1: PWM1 output
		3-state	push/pull or open drain output selectable
		Open Drain	
PA3/	1	1/0	Port A3: I/O port
PWM2	ľ	3-state	PWM (14 bit) output 2: PWM2 output
		Open Drain	push/pull or open drain output selectable
PA4/	1	1/0	Port A4: I/O port
. , , , ,	1	3-state	push/pull or open drain output selectable
		Open Drain	
		Open Brain	
₩R		Output	Write: Strobe signal for writing data on pins D0 to D7
PA5/	1	1/0	Port A5: I/O port
PWM3/	l'	Output	8-bit PWM output 3: PWM3 output
1 111107		3-state	push/pull or open drain output selectable
		Open Drain	prompting of open drain surpar solocus.
HWR		Output	High write: Strobe signal for writing data on pins D8 to D15
P60/	1	1/0	Port 60: I/O port
PWM4/	ľ	Output	8-bit PWM output 4: PWM4 output
,		3-state	push/pull or open drain output selectable
		Open Drain	
CS0		Output	Chip select0: Output _0_ when address is within specified address area.
P61/	1	1/0	Port 61: I/O port
PWM5/		Output	8-bit PWM output 5: PWM5 output
,		3-state	push/pull or open drain output selectable
		Open Drain	
CS1		Output	Chip select1: Output _0_ when address is within specified address area.
P62/	1	1/0	Port 62: I/O port
PWM6/		Output	8-bit PWM output 6: PWM6 output
1 11410/		3-state	push/pull or open drain output selectable
		Open Drain	Passingali of open didili output selectable
CS2		Output	Chip select2: Output _0_ when address is within specified addiess area.

Table 2.2.1 Pin Names and Function (3/5)

Pin name	Number of pins	1/0	Functions
P63/	1	1/0	Port 63: I/O port
PWM7		Output	8-bit PWM output7: PWM7 output
	İ	3-state	push/pull or open drain output selectable
		Open Drain	
P64/	1	1/0	Port 64: I/O port
PWM8		Output	8-bit PWM output8: PWM8 output
		3-state	push/pull or open drain output selectable
<u> </u>		Open Drain	
P65/	1	I/O	Port 65: I/O port
PWM9	ľ	Output	8-bit PWM output9: PWM9 output
		3-state	push/pull or open drain output selectable
-		Open Drain	
P66/	1	1/0	Port 66: I/O port
PWM10		Output	8-bit PWM output 10: PWM10 output
		3-state	push/pull or open drain output selectable
P67/	1	Open Drain I/O	Port 67: I/O port
PWM11	"	Output	8-bit PWM output 11: PWM11 output
*******		3-state	push/pull or open drain output selectable
		Open Drain	pushipuh of open drain output selectable
P73/	1	I/O	Port 73: I/O port
SDA0	'	1/0	I ² CBUS SDA line 0
		(schmitt)	push/pull or open drain output selectable
		Open Drain	passingan or open diam output solicotable
P74/	1	1/0	Port 74: I/O port
SCLO		1/0	I²CBUS SCL line 0
		(schmitt)	
		Open Drain	push/pull or open drain output selectable
P75/	1	1/0	Port 75: I/O port
SO0	ı	Output	SIO0 send data 0
		(schmitt)	push/pull or open drain output selectable
		Open Drain	
P76/	1	1/0	Port 76: I/O port
SIO		Input	SIO0 receive data 0
		(schmitt)	
P77/	1	1/0	Port 77: I/O port
SCK0		1/0	SIO0 transfer clock input/output 0
	ļ.	(schmitt)	
		Open Drain	push/pull or open drain output selectable
P70/	1	1/0	Port 70: I/O port
TXD		Output	UART send data
		(schmitt)	push/pull or open drain output selectable
		Open Drain	
P71/	1	1/0	Port 71: I/O port
RXD		Input	UART receive data
D72 /		(schmitt)	D 170 V9
P72/	1	I/O	Port 72: I/O port
CTS		Input	UART clear to send
Den /		(schmitt)	D-100 VO
P80/ CTLIN	1	I/O	Port 80: I/O port
CILIN		Input	Capture input for Control signal (CTL)
		(schmitt)	

Table 2.2.1 Pin Names and Function (4/5)

Table 2.2.1 Pin Names and Function (4/5)					
Pin Name	Number of pins	1/0	Functions		
P81/	1	1/0	Port 81: I/O port		
DFGIN		Input	Capture input for Drum-FG signal (DFG)		
		(schmitt)			
P82/	1	1/0	Port 82: I/O port		
RMTIN		Input	Capture input for Remote Control Input signal		
		(schmitt)			
P83/	1	I/O	Port 83: I/O port		
EXT		Input	External Capture input (Rising edge only)		
		(schmitt)			
P84/	1	I/O	Port 84: I/O port		
DPGIN		Input	Capture input for Drum-PG signal (DPG)		
		(schmitt)			
P85/	1	I/O	Port 85: I/O port		
CFGIN		Input	Capture input for Capstan-FG signal (CFG)		
		(schmitt)			
P86/	1	1/0	Port 86: I/O port		
CSYNC IN		Input	Capture input for C-sync		
		(schmitt)			
P87/	1	1/0	Port 87: I/O port		
COMPIN		Input	Envelope Comparator Input (to HA/CR)		
		(schmitt)			
P90/	1	1/0	Port 90: I/O port		
TPG12	1	Output	TPG12: TPG output 12		
		Open Drain	push/pull or open drain output selectable		
P91/	1	I/O	Port 91: I/O port		
TPG01	ľ	Output	TPG01: TPG output 01		
		Open Drain	push/pull or open drain output selectable		
P92/	1	1/0	Port 92: I/O port		
TPG02	ľ	Output	TPG02: TPG output 02 (Internally connected to PV/PH Logic)		
11.002		Open Drain	push/pull or open drain output selectable		
P93/	1	1/0	Port 93: I/O port		
TPG03	ľ	Output	TPG03: TPG output 03		
1'' 000		Open Drain	push/pull or open drain output selectable		
P94/	1	I/O	Port 93: I/O port		
TPG04	`	Output	TPG04: TPG output 04 (Internally connected to PV/PH Logic)		
004			push/pull or open drain output selectable		
P95/	1	1/0	Port 95: I/O port		
TPG13		Output	TPG13: TPG output 13		
11 013		Open Drain	push/pull or open drain output selectable		
P96/	1	I/O	Port 96: I/O port		
TPG10		Output	TPG10: TPG output 10		
17910		Open Drain	1		
D07/	1	I/O	push/pull or open drain output selectable Port 97: I/O port		
P97/ TPG11	['	Output	TPG11: TPG output 11		
I POLI			· ·		
BAO	1	Open Drain	push/pull or open drain output selectable		
PA0/	[1	I/O	Port PA0: I/O Port		
PV-PH		Output	Pseudo-Vsync/Pseudo-Hsync (PV/PH) output (controlled by		
544		3-state	TPG02/04.)		
PA1/	1	1/0	Port PA1: I/O Port		
HA (TPG05)		Output	HA: Head amp switch output (are also used as TPG05 output.)		
PA2/	1	1/0	Port PA2: I/O Port		
CR (TPG00)		Output	CR: Colour Rotary output (are also used as TPG00 output.)		

Table 2.2.1 Pin Names and Function (5/5)

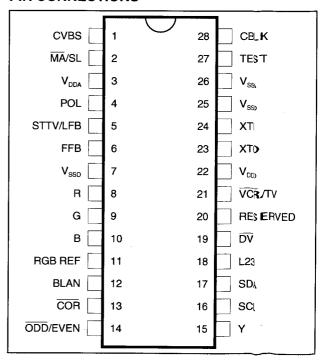
Pin name	Number of pins	I/O	Functions
PB2/	1	1/0	Port PB2: I/O Port
SO1/SI1		I/O (schmitt)	SIO1 send data 1 and receive data 1 (Internally connected)
		Open Drain	push/pull or open drain output selectable
PB3/	1	I/O	Port PB3: I/O Port
SCK1		1/0	SIO1 transfer clock input/output 1
		(schmitt)	
		Open Drain	push/pull or open drain output selectable
PB4/	1	1/0	Port PB4: I/O Port
SDA1		1/0	l ² CBUS SDA line 1
		(schmitt)	
		Open Drain	push/pull or open drain output selectable
PB5/	1	1/0	Port PB5: I/O Port
SCL1		1/0	I ² CBUS SCL line 1
		(schmitt)	
		Open Drain	push/pull or open drain output selectable
DVCC1, 2, 3	3		Power supply pins All of these pins should be connected to power
			source.
DGND1, DGND2 (ADGND),	3		GND pins (0 V) All of these pins should be connected to GND (0 V)
DGND3			line.
			DGND2 are also used as ADGND for A/D converter.

STV5348

- COMPLETE TELETEXT AND VPS DECODER INCLUDING AN 8 PAGE MEMORY ON A SIN-GLE CHIP
- UPWARD SOFTWARE COMPATIBLE WITH PREVIOUS SGS-THOMSON'S MULTICHIP SOLUTIONS (SAA5231, SDA5243, STV5345)
- PERFORM PDC SYSTEM A (VPS) AND PDC SYSTEM B (8/30/2) DATA STORAGE SEPA-RATLY
- DEDICATED "ERROR FREE" OUTPUT FOR VALID PDC DATA
- INDICATION OF LINE 23 FOR EXTERNAL USE
- SINGLE +5V SUPPLY VOLTAGE
- SINGLE 13.875MHz CRYSTAL
- REDUCED SET OF EXTERNAL COMPO-NENTS, NO EXTERNAL ADJUSTMENT
- OPTIMIZED NUMBER OF DIGITAL SIGNALS REDUCING EMC RADIATION
- HIGH DENSITY CMOS TECHNOLOGY
- DIGITAL DATA SLICER AND DISPLAY **CLOCK PHASE LOCK LOOP**
- 28 PIN DIP & SO PACKAGE

(Plastic Package) **ORDER CODE:** STV5348 West European STV5348/H East European STV5348/T Turkish & European **SO28** (Plastic Package) **ORDER CODE:** STV5348D West European STV5348D/H East European STV5348D/T Turkish & European

PIN CONNECTIONS



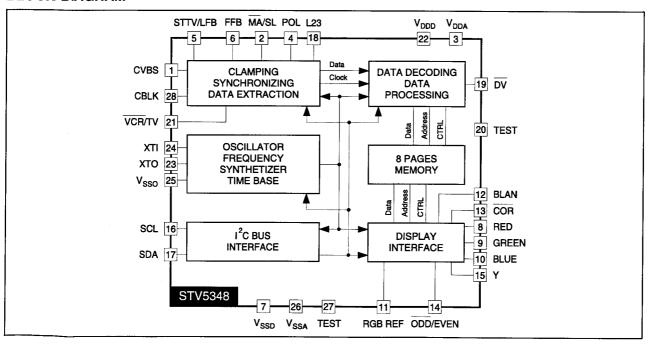
DESCRIPTION

The STV5348 decoder is a computer-controlled teletext device including an 8 page internal memory. Data slicing and capturing extracts the teletext information embedded in the composite video signal. Control is accomplished via a two wire serial I²C bus ®. Chip address is 22h. Internal ROM provides a character set suitable to display text using up to seven national languages. Hardware and software features allow selectable master/slave synchronization configurations. The STV5348 also supports facilities for reception and display of current level protocol data.

PIN DESCRIPTION

Pin N ^o	Symbol	Function	Description	Figure
1	CVBS	Input	Composite Video Signal Input through Coupling Capacitor	9
2	MA/SL	Input	Master/Slave Selection Mode	11
3	V_{DDA}	Analog Supply	+5V	-
4	POL	Input	STTV / LFB / FFB Polarity Selection	12
5	STTV/LFB	Output / Input	Composite Sync Output, Line Flyback Input	15
6	FFB	Input	Field Flyback Input	12
7	V _{SSD}	Ground	Digital Ground	-
8	R	Output	Video Red Signal	13
9	G	Output	Video Green Signal	13
10	В	Output	Video Blue Signal	13
11	RGBREF	Supply	DC Voltage to define RGB High Level	13
12	BLAN	Output	Fast Blanking Output TTL Level	15
13	COR	Output	Open Drain Contrast Reduction Output	15
14	ODD/EVEN	Output	25Hz Output Field synchronized for non-interlaced display	15
15	Y	Output	Open Drain Foreground Information Output	15
16	SCL	Input	Serial Clock Input	16
17	SDA	Input/ Output	Serial Data Input/Output	17
18	L23	Output	Line 23 Identification	15
19	DV	Output	VPS Data Valid	15
20	RESERVED	Test	To be connected to V _{SSD} through a resistor	15
21	VCR/TV	Input	PLL Time Constant Selection	15
22	V_{DDD}	Digital Supply	+5V	-
23	XTO	Crystal Output	Oscillator Output 13.875MHz	14
24	XTI	Crystal Input	Oscillator Input 13.875MHz	14
25	Vsso	Ground	Oscillator Ground	
26	V _{SSA}	Ground	Analog Ground -	
27	TEST	Test	Grounded to V _{SSA}	11
28	CBLK	Input / Output	To connect Black Level Storage Capacitor 28	

BLOCK DIAGRAM



5348-01.TBL

9.8.9 Tuner1705: UV1316K

VHF/UHF television tuner

UV1336K MK3

FEATURES

Member of UV1300 MK3 family of small-sized **UHF/VHF** tuners

Integrated with passive splitter

Covers systems M, N

Digitally-controlled (PLL) tuning via I²C-bus

Fast 400kHz I²C bus protocol compatible with

3.3V and 5V micro controllers

181 channels coverage (Off-air and full cable)

World standardized mechanical dimensions and

pinning. Horizontal mounting is optionally

available.



DESCRIPTION

The UV1336K MK3 splitter - tuner belongs to the UV1300 family of WSP tuners, which are designed to meet a wide range of TV applications. It is a full band tuner suitable for NTSC M, N and PAL M, N. The low IF output impedance is designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

The UV1336K MK3 incorporates internal wideband-AGC with selectable TOP adjustment via I2C.

This tuner complies with the requirements of radiation, conforming with:

FCC Part 15, Subpart B

BETS 7

CISPR13

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner:

Type number

Code number

Origin letter of factory

Change code

Year and week code

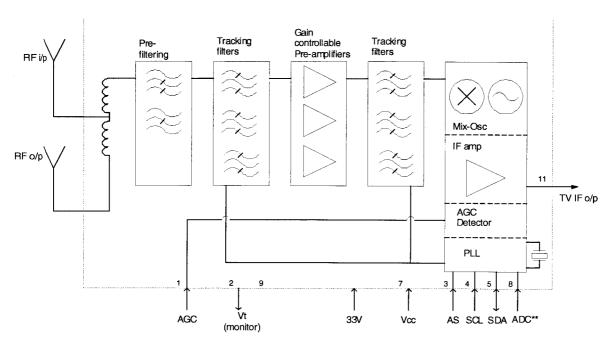
ORDERING INFORMATION

TYPE	DESCRIPTION	ORDER NUMBERS	
UV1336K/A F G S-3	F connector, wideband AGC, switchable FM trap	3139 147 1701 1	

VHF/UHF television tuner

UV1336K MK3

BLOCK DIAGRAM



** ADC option not available in NTSC versions

PINNING

SYMBOL	PIN	DESCRIPTION	
AGC	1	Gain Control Voltage	
TU	2	Tuning voltage	
AS	3	I ² C-Bus Address Select	
SCL	4	I ² C-Bus Serial Clock	
SDA	5	I ² C-Bus Serial Data	
n.c.	6	Not Connected	
V _s	7	PLL Supply Voltage +5V	
n.c	8	Not Connected	
V _{ST}	9	Fixed tuning Supply Voltage +33V	
n.c	10	Not connected	
IF1	11	Asymmetrical IF Output	
GND	M1,M2,M3,M4	Mounting Tags (Ground)	

9.9 **IC's Digital Board**

9.9.1 IC7100: VSM

VERSATILE STREAM MANAGER

GENERAL DESCRIPTION

The Versatile Stream Manager (VSM) is an ASIC used in the first generation DVD Video Recorder. Main function of the VSM is to interface directly to the different hardware modules such as Basic Engine, MPEG encoders, MPEG decoders and buffering the data streams that are coming from or going to these hardware modules.

The VSM contains a memory interface to support one 4M*16 SDRAM device. A host interface allows a CPU to directly access this memory and the VSM's internal registers.

Handling of data streams is done using scatter / gather DMA's under software control. Hardware support is provided in the VSM to support software MPEG AV multiplexing.

FEATURES

The VSM features include:

SDRAM memory interface to support one 4 banks*1M*16 (64Mbit) SDRAM device.

Glueless Host Interface for STM's STi5505.

Glueless MPEG Decoder interface for STM's STi5505

Glueless interface to Philips' SAA6750 MPEG Video Encoder or SAA6752 MPEG AV Encoder.

Glueless interface to Motorola's DSP56362 used as MPEG Audio Encoder.

Glueless interface to Philips' HDR65 as part of Basic Engine interface including the Sector Processor as also included in the STi5505.

Audio Clock Control providing PLL loop and clock lock detection.

Double Extraction of VBI decoded data from extended CCIR 656 stream.

Double UART with hardware handshake and 8 byte Rx/Tx FIFO.

Generation of additional Host Bus to support Audio Encoder DSP56362.

Descriptor based DMA Controllers for data stream handling.

Hardware support for software MPEG multiplex process.

Internal Interrupt Controller to handle internal and 4 external interrupt sources.

Operates from single 27 MHz clock input.

JTAG for production tests.

3.3V logic core.

3.3V / 5V toleration IO pins.

208 PIN LQFP Package. (CR1087)

BLOCK DIAGRAM

Figure 2.1 shows the block diagram of the VSM. The hardware blocks can be divided in to three categories:

General modules: Host Interface, Memory Interface, Interrupt Controller.

DMA Controllers.

Functional Interfaces; the link between the actual external hardware interface and the DMA Controller. Some Functional Interfaces have knowledge about the stream coming through in order to perform for example MPEG stream characteristics extraction and insertion.

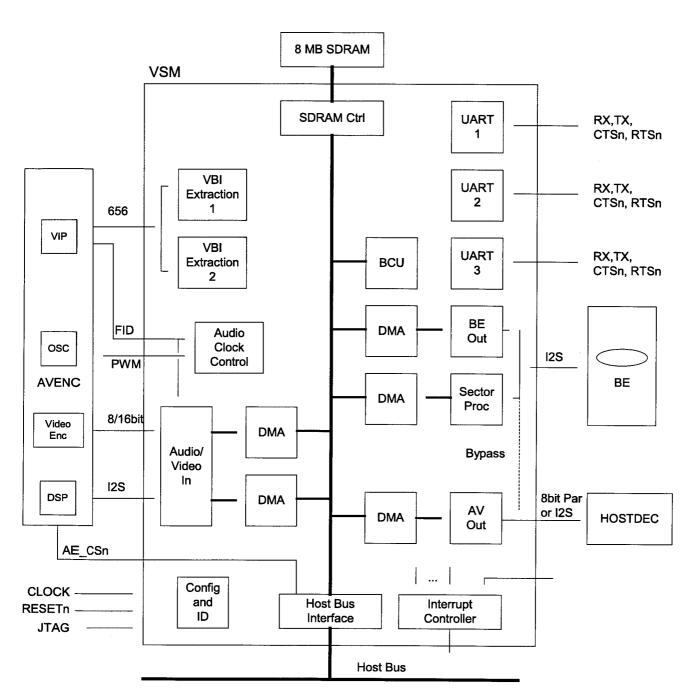


Figure 2.1: VSM Overview

PINNING

OVERVIEW

Name	Pins	Туре	Function
System			
RESETn	1	In	
SYSCLK (27MHz)	1	ln	
Host Interface			
HO_A(21:1)	21	In	
HO_D(15:0)	16	In/Out	
HO_BEn(1:0)	2	In	
HO RWn	1	In	
HO CSLn	1	In	
HO CSHn	1	In	
HO A22	1	In	
HO WAIT	1	Out	
HO_PROCCLK	1	ln	
Memory Interface		•	
M_A(13:0)	14	Out	
M_DQ(15:0)	16	In/Out	
M RASn	1	Out	
M CASn	1	Out	
M WEn	1	Out	
M LDQM	1	Out	
M UDQM	1	Out	
M CLKOUT	1	Out	
M CLKEN	1	Out	
Basic Engine Interface	-		
BE BCLK	1	In	
BE DATI	1	In	
BE WCLK	1	In	
BE SYNC	1	In/Out	
BE FLAG	1	In	
BE V4	1	ln In	
BE DATO	1	Out	
Video Encoder Interface			
VE D(15:0)	16	In	
VE_DSn	1	Out	
VE DTACKn	- i -	In	
VE VIP ERROR	1	ln In	Signal coming from SAA7114
Audio Encoder Interface		1 111	Cignal colling from SAA7 114
AE_CSn	1	Out	
AE BCLK	1	In/Out	(CR151,CR157)
AE WCLK	1	In/Out	(CR151,CR157)
AE DATA	1	In	(CR157)
'\D'\\\	i	l ""	1,/

Decoder Interface			
D PAR D(7:0)	8	Out	
D PAR DVALID	1	Out	
D PAR STR	1	Out	
D PAR REQ	1	In	
D PAR SYNC	1 1	Out	
D_PAR_STNC	1 1		
D V4	· · · · · · · · · · · · · · · · · · ·	Out	
	1 1	Out	
Audio Clock Control ACC FID	1 4	1	(CR200)
	1 1	ln Out	(CINZOU)
ACC_PWM	1	Out	
ACC_ACLK_OSC	1 1	<u>In</u>	
ACC_ACLK_DAI	1	<u>In</u>	
ACC_ACLK_PLL	1	ln	
ACC_ACLK_DEC	1	Out	
VBI Extractor	-	· T · · · · · · · · · · · · · · · · · · ·	
VBI_IPD(7:0)	8	<u>In</u>	
VBI_ICLK	1	ln .	
UART 1			
UART1_RX	1	<u>In</u>	
UART1_TX	1	Out (OC)	
UART1_CTSn	1	In	
UART1_RTSn	1	Out (OC)	
UART 2			
UART2_RX	1	ln	
UART2_TX	1	Out (OC)	
UART2_CTSn	1	ln	
UART2_RTSn	1	Out (OC)	
UART 3 (VSM1B)			
UART3_RX	1	In	
UART3_TX	1	Out	
UART3_CTSn	1	In	
UART3 RTSn	1	Out	
Interrupt Controller			
EXTINT(3:0)	4	In	From: VEnc, AEnc, BE, VSync (STi5505)
CPUINT(1:0)	2	Out (OC)	
JTAG		<u> </u>	
TCK	1	In	Boundary Scan
TDI	1 1	In	
TDO	1 1	Out/Z	
TMS	1	In	
TRSTn	1 1	In	
Test	<u> </u>	111	
TESTO	1	ln	Amsal Test
TEST1	1	In	Alloal I Col
Power Supply	I	111	
VDD	20	Dower	100/ of total pine poels
VSS	20	Power	10% of total pins package
V33	20	Power	10% of total pins package
Total Diva	000	1	
Total Pins	208		

9.9.2 IC7101; IC7306: SDRAM

SDRAM MT48LC1M16A1 SIT - 512K x 16 x 2 banks

FEATURES

- PC100 functionality
- · Fully synchronous; all signals registered on positive edge of system clock
- · Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge 1 Meg x 16 - 512K x 16 x 2 banks architecture with 11 row, 8 column addresses per bank
- Programmable burst lengths: 1, 2, 4, 8 or full page
- Auto Precharge Mode, includes CONCURRENT **AUTO PRECHARGE**
- Self Refresh and Adaptable Auto Refresh Modes
 - 32ms, 2,048-cycle refresh or
 - 64ms, 2,048-cycle refresh or
 - 64ms, 4,096-cycle refresh
- LVTTL-compatible inputs and outputs
- Single $+3.3V \pm 0.3V$ power supply
- Supports CAS latency of 1, 2 and 3
- Industrial temperature range: -40°C to +85°C

OPTIONS

MARKING

•	Configuration 1 Meg x 16 (512K x 16 x 2 banks)	1M16A1
•	Plastic Package - OCPL* 50-pin TSOP (400 mil)	TG
•	Timing (Cycle Time) 6ns (166 MHz) 7ns (143 MHz)	-6 -7
	8ns (125 MHz)	-8A

 Refresh 2K or 4K with Self Refresh Mode at 64ms S

• Operating Temperature -40°C to +85°C

Part Number Example: MT48LC1M16A1TG-7SIT

KEY TIMING PARAMETERS

SPEED	CLOCK	ACCESS TIME	SETUP	HOLD
		CL = 3**		
-6	166 MHz	5.5ns	2ns	1ns
-7	143 MHz	5.5ns	2ns	1ns
-8A	125 MHz	6ns	2ns	1ns

PIN ASSIGNMENT (Top View) 50-Pin TSOP VDD ₩ Vss HHH | DQ15 | DQ14 | DQ14 | DQ14 | DQ13 | DQ12 | DQ11 | DQ11 | DQ11 | DQ11 | DQ11 | DQ9 | DQ8 | DQ8 | DQ8 | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH | DQMH DQ0 DQ1 VssQ 48 DQ2 DQ3 нявяваннянняння VDDQ DQ4 DQ5 11 12 40 39 DQ6 DQ7 VDDQ DQML 14 15 WE# CAS# RAS# 35 34 33 32 31 30 18 BA A10 20 A0 A1 A2 22 23 29 28 HH АЗ VDD Note: The # symbol indicates signal is active LOW. 1 Meg x 16 Configuration 512K x 16 x 2 banks Refresh Count 2K or 4K Row Addressing 2K (A0-A10)

16Mb (x16) SDRAM PART NUMBER

PART NUMBER	ARCHITECTURE
MT48LC1M16A1TG SIT	1 Meg x 16

2 (BA)

256 (AO-A7)

GENERAL DESCRIPTION

Bank Addressing

Column Addressing

The 16Mb SDRAM is a high-speed CMOS, dynamic random-access memory containing 16,777216 bits. It is internally configured as a dual 512K x 16 DRAM with a synchronous interface (all signals are registered on the positive edge of the clock signal, CLK). Each of the 512K x 16-bit banks is organized as 2,048 rows by 256 columns by 16 bits. Read and write accesses to the SDRAM are burst oriented; accesses start at a selected location and continue for a programmed number of locations in aprogrammed

GENERAL DESCRIPTION (continued)

sequence. Accesses begin with the registration of an AC-TIVE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVE command are used to select the bank and row to be accessed (BA selects the bank, A0-A10 select the row). The address bits registered coincident with the READ or WRITE command are used to select the starting column location for the burst access.

The SDRAM provides for programmable READ or WRITE burst lengths of 1, 2, 4 or 8 locations, or the full page, with a burst terminate option. An AUTO PRECHARGE function may be enabled to provide a self-timed row precharge that is initiated at the end of the burst sequence.

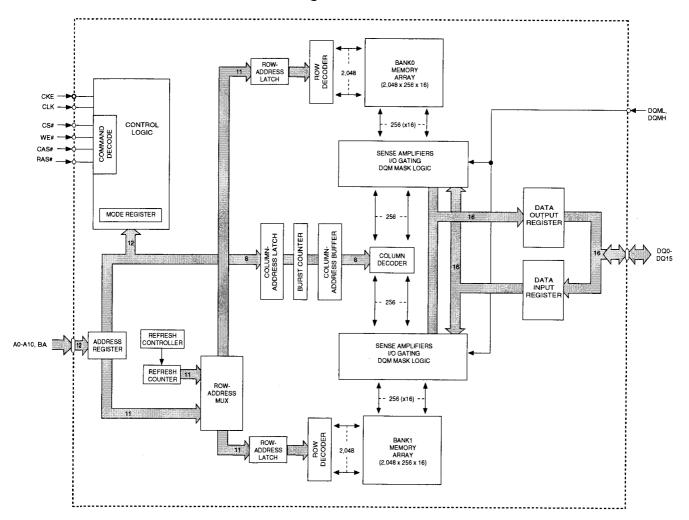
The 1 Meg x 16 SDRAM uses an internal pipelined architecture to achieve high-speed operation. This architecture is compatible with the 2*n* rule of prefetch architectures,

but it also allows the column address to be changed on every clock cycle to achieve a high-speed, fully random access. Precharging one bank while accessing the alternate bank will hide the PRECHARGE cycles and provide seamless, high-speed, random-access operation.

The 1 Meg x 16 SDRAM is designed to operate in 3.3V, low-power memory systems. An auto refresh mode is provided, along with a power-saving, power-down mode. All inputs and outputs are LVTTL-compatible.

SDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a high data rate with automatic columnaddress generation, the ability to interleave between internal banks in order to hide precharge time, and the capability to randomly change column addresses on each clock cycle during a burst access.

FUNCTIONAL BLOCK DIAGRAM 1 Meg x 16 SDRAM



PIN DESCRIPTIONS

PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION	
35	CLK	Input	Clock: CLK is driven by the system clock. All SDRAM input signals are sampled on the positive edge of CLK. CLK also increments the internal burst counter and controls the output registers.	
34	CKE	Input	Clock Enable: CKE activates (HIGH) and deactivates (LOW) the CLK signal. Deactivating the clock provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), ACTIVE POWER-DOWN (row ACTIVE in either bank) or CLOCK SUSPEND operation (burst/access in progress). CKE is synchronous except after the device enters power-down and self refresh modes, where CKE becomes asynchronous until after exiting the same mode. The input buffers, including CLK, are disabled during power-down and self refresh modes, providing low standby power. CKE may be tied HIGH.	
18	CS#	Input	Chip Select: CS# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when CS# is registered HIGH. CS# provides for external bank selection on systems with multiple banks. CS# is considered part of the command code.	
15, 16, 17	WE#, CAS#, RAS#	Input	Command Inputs: RAS#, CAS# and WE# (along with CS#) define the command being entered.	
14, 36	DQML, DQMH	Input	Input/Output Mask: DQM is an input mask signal for write accesses and an output enable signal for read accesses. Input data is masked when DQM is sampled HIGH during a WRITE cycle. The output buffers are placed in a High-Z state (two-clock latency) when DQM is sampled HIGH during a READ cycle. DQML corresponds to DQ0-DQ7; DQMH corresponds to DQ8-DQ15. DQML and DQMH are considered same state when referenced as DQM.	
19	ВА	Input	Bank Address Inputs: BA defines to which bank the ACTIVE, READ, WRITE or PRECHARGE command is being applied. BA is also used to program the twelfth bit of the Mode Register.	
21-24, 27-32, 20	A0-A10	Input Address Inputs: A0-A10 are sampled during the ACTIVE comman address A0-A10) and READ/WRITE command (column-address A10 defining AUTO PRECHARGE) to select one location out of the available in the respective bank. A10 is sampled during a PRECH command to determine if all banks are to be precharged (A10 HIG address inputs also provide the op-code during a LOAD MODE RI command.		
2, 3, 5, 6, 8, 9, 11, 12, 39, 40, 42, 43, 45, 46, 48, 49	DQ0- DQ15	Input/ Output	Data I/Os: Data bus.	
33, 37	NC		No Connect: These pins should be left unconnected.	
7, 13, 38, 44	VddQ	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.	
4, 10, 41, 47	VssQ	Supply		
1, 25	VDD	Supply	Power Supply: +3.3V ±0.3V.	
26, 50	Vss	Supply	Ground.	

9.9.3 IC7200: NVRAM

M24C64 M24C32

64/32 Kbit Serial I2C Bus EEPROM

- Compatible with I²C Extended Addressing
- Two Wire I²C Serial Interface Supports 400 kHz Protocol
- Single Supply Voltage:
 - 4.5V to 5.5V for M24Cxx
 - 2.5V to 5.5V for M24Cxx-W
 - 1.8V to 3.6V for M24Cxx-R
- Hardware Write Control
- BYTE and PAGE WRITE (up to 32 Bytes)
- RANDOM and SEQUENTIAL READ Modes
- Self-Timed Programming Cycle
- Automatic Address Incrementing
- Enhanced ESD/Latch-Up Behavior
- 1 Million Erase/Write Cycles (minimum)
- 40 Year Data Retention (minimum)

DESCRIPTION

These I²C-compatible electrically erasable programmable memory (EEPROM) devices are organized as 8192x8 bits (M24C64) and 4096x8 bits (M24C32), and operate down to 2.5 V (for the -W version of each device), and down to 1.8 V (for the -R version of each device).

The M24C64 and M24C32 are available in Plastic Dual-in-Line, Plastic Small Outline and Thin Shrink Small Outline packages.

Table 1. Signal Names

E0, E1, E2	Chip Enable Inputs	
SDA	Serial Data/Address Input/ Output	
SCL	Serial Clock	
WC	Write Control	
VCC	Supply Voltage	
V _{SS}	Ground	

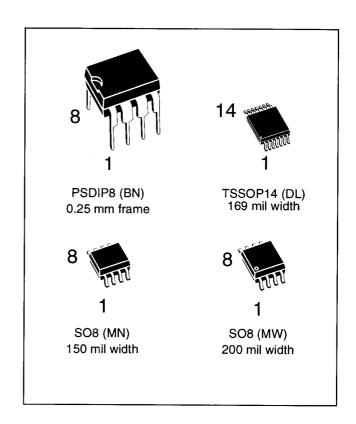
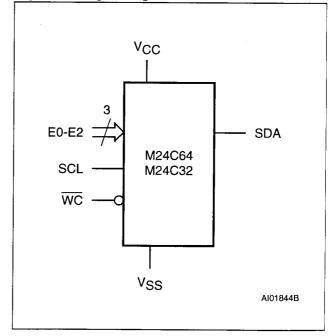


Figure 1. Logic Diagram



M24C64, M24C32

Figure 2A. DIP Connections

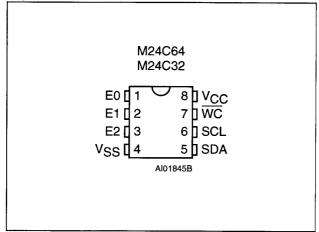
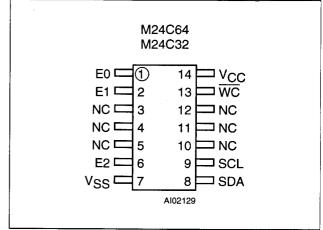
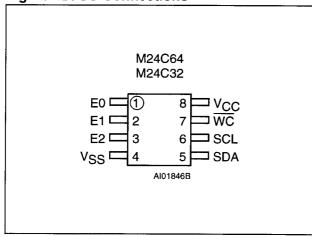


Figure 2C. TSSOP Connections



Note: 1. NC = Not Connected

Figure 2B. SO Connections



These memory devices are compatible with the I²C extended memory standard. This is a two wire serial interface that uses a bi-directional data bus and serial clock. The memory carries a built-in 4bit unique Device Type Identifier code (1010) in accordance with the 12C bus definition.

The memory behaves as a slave device in the I²C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the bus master. The START condition is followed by a Device Select Code and RW bit (as described in Table 3), terminated by an acknowledge bit.

When writing data to the memory, the memory inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission.

Table 2. Absolute Maximum Ratings ¹

Symbol	Parameter	Value	Unit	
T _A	Ambient Operating Temperature		-40 to 125	°C
T _{STG}	Storage Temperature		-65 to 150	°C
T _{LEAD} Lead Temperature during Soldering SO		PSDIP8: 10 sec SO8: 40 sec TSSOP14: t.b.c.	260 215 t.b.c.	°C
V _{IO}	Input or Output range		-0.6 to 6.5	V
V _{CC}	Supply Voltage		-0.3 to 6.5	V
V _{ESD}	Electrostatic Discharge Voltage (Human E	4000	V	

Note: 1. Except for the rating "Operating Temperature Range", stresses above those listed in the Table "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum R ating conditions for extended periods may affect device reliability. Refer also to the ST SURE Program and other relevant quality documents. 2. MIL-STD-883C, 3015.7 (100 pF, 1500 Ω)

DVD BACKEND DECODER WITH INTEGRATED HOST PROCESSOR

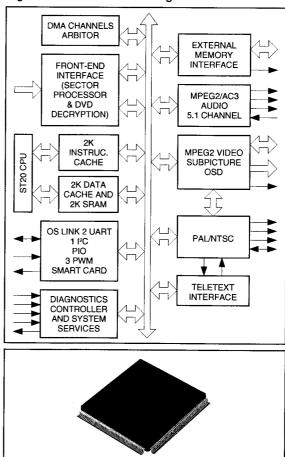
PRODUCT PREVIEW

- INTEGRATED 32-BIT RISC HOST CPU
 - 2KBYTES INSTRUCTION CACHE, 2KBYTES DATA CACHE/SRAM
 - 50K DHRYSTONES/SEC (2.1) 50MHz
- VIDEO DECODER
 - FULLY SUPPORTS MPEG-2 MP@ML
 - MEMORY REDUCTION PAL IN 12MBITS
- SUBPICTURE DECODER
- HIGH PERFORMANCE ON-SCREEN DISPLAY
- AUDIO DECODER
 - 5.1 CHANNEL DOLBY AC-3® / MULTI CHANNEL MPEG-2 DECODING
 - DOWNMIX TO STEREO OR TO DOLBY PRO-LOGIC COMPATIBLE OUTPUTS FOR MPEG-2 AND AC-3
 - IEC6958 IEC61937 COMPATIBLE OUTPUT
 - LPCM (DVD) MODE SUPPORTED
 - 6 CHANNELS OUTPUT
- PAL/NTSC ENCODER
 - MACROVISIONTM 7.01/6.1 COMPATIBLE
 - TELETEXT, AND CLOSED CAPTION
- HIGH PERFORMANCE SDRAM INTERFACE
- PROGRAMMABLE MEMORY INTERFACE FOR DRAM, ROM, PERIPHERALS ETC.
- FRONT-END CHANNEL IC INTERFACE
 - DVD, VCD AND CD-DA COMPATIBLE
 - DSS DVB BISTREAMS
 - SERIAL AND PARALLEL INTERFACES
 - HARDWARE SECTOR FILTERING
 - INTEGRATED CSS DECRYPTION AND TRACK BUFFER
- INTEGRATED PERIPHERALS
 - 2 UARTS, 1 I²C CONTROLLER, 3 PWM OUT-PUTS, 3 TIMERS, 3 CAPTURE TIMERS. **SMART CARD**
 - 34 BITS OF PROGRAMMABLE I/O
 - OS LINK
- PROFESSIONAL TOOLSET SUPPORT
 - ANSI C COMPILER AND LIBRARIES
 - OPERATING SYSTEMS SUPPORT
 - ADVANCED DEBUGGING TOOLS
- 208 PIN PQFP PACKAGE

DESCRIPTION

The STi5505 provides a very highly integrated backend solution for DVD and combo DVD-DVB (Set Top Box) applications. The STi5505 incorporates a host CPU which handles both general application (DVD navigation, CD-DA, VCD, DVB) and drivers of the different embedded periphals (audio/video, subpicture decoders, OSD, PAL/NTSC encoder...). The STi5505 offers one of the best cost-effective (memory savings, internal peripherals availability) solution to DVD-DVB applications with rapid time to market (Reference design, DVD-DVB Software Toolkit).

Figure 1: General Block Diagram





I - GENERAL DESCRIPTION

The performance offered by the ST20 CPU and its associated hardware (decoders, encoder, peripherals...) allows an integrated and unified DVD or DVD-DVB software solution.

All the following operations are performed inside the STi5505:

- application management (DVD Navigation, VCD, CD-DA, DVB-Program Guide ...),
- device data retrieval drivers (demultiplex, stream buffer management ...),
- device presentation drivers (video decoder, subpicture decoder, on-screen display, audio decoder, PAL/NTSC encoder ...),
- embedded peripherals drivers (UART, I²C, Programmable I/O, Smart Card ...).

I.1 - ST20 32-bit CPU

The ST20 micro-core family has been developped by SGS-THOMSON Microelectronics to provide the tools and building blocks to enable the development of highly integrated application-specific 32bits device at the lowest cost and fastest time to market.

The STi5505 integrates a ST20 C2 core with the following characteristics:

- 50K Dhrystones/s at 50MHz,
- 8/16 bits instructions (32 most common instructions in 8 bits),
- instruction cache 2Kbytes write back replacement policy,
- internal SRAM 2Kbytes to ensure fast access to critical code, data, interrupt handler ...
- data cache 2 Kbytes write back replacement policy, The STi5505's ST20 is provided with advanced debugging tools:
- on-chip real-time emulation,
- debugging with minimal impact on software and performance.
- non intrusive attachment to the host via JTAG (IEEE1149.1),
- no intrusion into the performance of the CPU core,
- no intrusion into user code space by a debug kernel,
- only 40bytes used for breakpoint handler.

I.2 - Video Decoder

The video decoder implemented in the STi5505 uses a patented memory reduction/bandwith reduction scheme to offer the user the best bandwidth/memory size compromise.

The algorithm is lossless and uses "on-the-fly" decoding to reduce the memory requirements to two frame buffers in memory reduction mode.

In this mode, PAL decoding is contained in 12Mbits. When used in bandwith reduction mode, the memory usage is the normal three buffers but the bandwith required by the decoder is significantly reduced compared to a classical implementation.

In summary, the features of the decoder are:

- MPEG-2 Main Profile/Main Level (MP@ML) support,
- MPEG-2 program streams, Packet Elementary streams and MPEG-1 system streams support,
- memory reduction architecture allowing sharing of single 16 Mbits SDRAM between MPEG decoding, micro and transport functions - memory expandable to 32 Mbits of SDRAM,
- letter box (16:9) filter,
- pan-scan, horizontal and vertical image resizing,
- automatic error concealment.

I.3 - Subpicture Decoder

The STi5505 has a hardware DVD compliant subpicture decoder. Subpicture units are copied by DMA into subpicture bit buffer.

The subpicture decoder can decode complete subpicture units without any interaction from the ST20.

The main subpicture decoder features are:

- up to 720x480 or 720x576 subpicture area.
- internal LUTs for Sub Picture, Highlight and PCI (4 bits color and contrast outputs),
- internal color LUT (4 bits from SP, HL, PCI to 24 Y, Cr, Cb bits) for SP color inputs to MPEG, OSD, SP mixer.

I.4 - Audio Decoder

The audio decoder cell is a fully compatible Dolby AC-3™ / MPEG-1/MPEG-2 decoder capable of decoding both 5.1 and 2 channel streams compatible with the DVD standard.

Downmix from 5.1 channels is supported for both Dolby and MPEG-2 streams. The output can be sent directly to external DACs or formatted for transmission in accordance with the IE6958 stand-

The decoder can also handle linear PCM in accordance with the DVD standard. An integrated downsampler is provided for conversion from 96 kHz to 48kHz.

I - GENERAL DESCRIPTION (continued)

The main features of the decoder core are:

- Decodes 5.1 Dolby AC-3 Digital surround,
- Output to 6 channels. Downmix modes: 1, 2, 3 or 4 channels for MPEG and AC-3 streams,
- Karaoke mode for DVD. MPEG-2 capable, AC-3 capable,
- MPEG-1, 2-channel audio decoder layers 1 and 2,
- MPEG-2, 6-channel audio decoder laver 2,
- PCM: transparent. downsampling 96 to 48 kHz,
- Accepts MPEG-2 PES stream format for : MPEG-2, MPEG-1, Dolby AC-3 and Linear PCM,
- IEC6958 Output Interface,
- CD-DA PCM format (subcode output in IEC6958 user data),
- Downmix for Dolby Pro Logic compatible outputs for AC-3 and MPEG-2 (Pro Logic encoder),
- Pro Logic decoder,
- PLL for Internal 44.1 and 48kHz PCM clock generation,
- On chip pink noise generator.

I.5 - High Performance On-Screen Display

The graphics performance of the STi5505 supports the new requirements for intelligent program guides and interactive applications.

The display interface supports up to 256 colors for each OSD region and a transparency feature allows mixing of video with the OSD. Fast access graphics and many other additional features are available and are supported by a graphics library.

Very high system performance is obtained by closely coupling the ST20 RISC processor and cache with the MPEG audio/video core and display

Low latency RISC access and DMA engines allow rapid construction of bit maps.

I.6 - PAL/NTSC Encoder

The STi5505 integrates a PAL/NTSC encoder. It converts the digital MPEG/Sub Picture/OSD stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. Six analog output pins are available on which it is possible to output CVBS, S-VHS (Y/C) and RGB formats.

The encoder handles interlaced and non-interlaced mode.

It can perform Closed Captions, CGMS or Teletext encoding and allows Macrovision 7.01/6.1 copy protection.

The encoder supports both master and slave modes for synchronization.

I.7 - Memory Interfaces

The STi5505 has been designed to minimize system costs by enabling various memory savings. Two kinds of memory interfaces are used on the STi5505: a programmable External Memory Interface (EMI) and a high performance SDRAM interface.

The External Memory Interface supports several address ranges (memory banks). In each bank, a set of signals are entirely programmable and can be used to map 8/16 bits peripherals such as Front End channel ICs in DVD applications.

The EMI contains a zero glue logic DRAM and a low-cost EPROM interface.

This interface can be programmed to interface very easily peripherals.

The SDRAM memory interface supports gluelessly 125 MHz SDRAMs providing the adequate bandwiths to achieve MPEG decoding and display, OSD drawing and display, and general system use.

Memory savings can be realized on ROM requirements too: the ST20 VL-RISC micro-core has the highest code density of any 32 bit CPU, leading to the lowest cost program ROM.

I.8 - Front-End Interface

The STi5505 's front end interface accepts:

- DVD, VCD and CD-DA sectors,
- DVB-DSS transport stream.

In DVD mode, DVD, VCD and CD-DA information can be input into STi5505 through a serial interface or a generic parallel interface.

In serial mode, data are captured and filtered from I2S and V4 interfaces by an internal sector processor. V4 interface is used to capture VCD and CD-DA subcode information. In parallel mode, sector processor is bypassed.

I - GENERAL DESCRIPTION (continued)

The main features of the DVD interface are:

- DVD, VCD and CD-DA compatible,
- hardware sector filtering,
- subcode error correction for CD-DA,
- integrated CSS decryption,
- integrated track buffer support.
- DMA engine to ST20 memory.

In DVB-DSS mode, DVB-DSS transport stream is input through a serial interface. The STi5505 extracts and descrambles Packet Elementary Streams belonging to one user selected program to be decoded and presented.

The main features of the DVB-DSS interface are:

- descrambling (transport packet and packet elementary streams in DVB mode, transport packet in DSS mode; up to 32 streams descrambling),
- PID and section filtering.
- clock recovery,
- DMA engine.

In DVB-DSS mode, a high speed digital interface

allows to transfer packets between the Set Top Box and external units, either for recording or playback purposes. This interface provides also full support for an external IEEE1394 connection.

I.9 - Integrated Peripherals

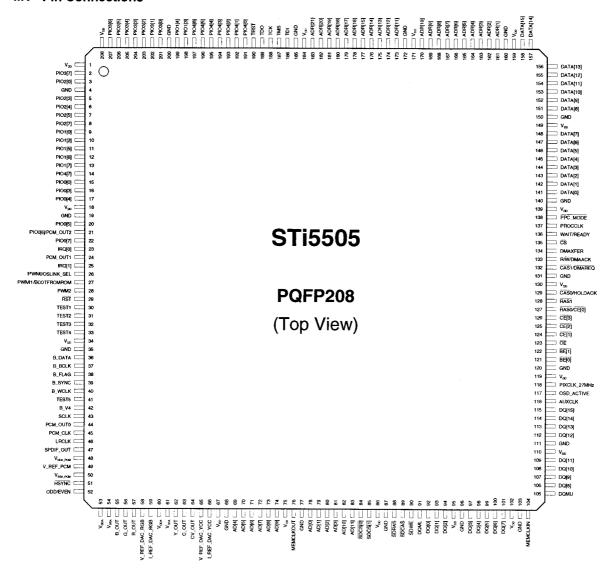
Several peripherals generally used in DVD players or DVD-DVB combos have been integrated into the STi5505.

They are:

- two UARTs to interface remote control receivers, DVD front end, modem ...,
- one I²C controller to interface serial memories, remote control receivers, microcontrollers...,
- 2 SmartCard interfaces (ISO7816-3) for DVB-DSS conditionnal access, pay per view ...,
- PWM/timer module for control of system clock,
- 34 programmable I/O pins,
- OS Link interface,
- JTAG with boundary scan for debug.

II - PIN DESCRIPTION

II.1 - Pin Connections



II - PIN DESCRIPTION (continued)

II.2 - Pin List

Pin	Name	Туре	Function
SUPPLIES		71-2	L
1, 18, 34, 67, 75, 86, 95, 102, 110, 119, 130, 139, 149, 159, 171, 184, 208			Power Supply
4, 19, 35, 68, 77, 87, 96, 103, 111, 120, 131, 140, 150, 160, 172, 185, 200	GND		Ground
53, 60	V_{DDA}		Analog Power Supply for DENC D/A Converters
54, 61	V _{SSA}		Analog Ground for DENC D/A Converters
48	V _{DDA_PCM}		Analog Power Supply for PLL PCM
49	V_REF_PCM		Analog Reference for PLL PCM
50	V _{SSA_PCM}		Analog Ground for PLL PCM
FRONT-END INTERFACE			
36	B_DATA	I	I ² S Data (DVD) or PARA_DATA[2] (DVD//) or Link Data (DVB/DSS)
40	B_WCLK	1/0	I ² S Word Clock or PARA_DATA[6] (DVD//) or NRSS_CLK (DVB/DSS)
37	B_BCLK	1	I ² S Bit Clock (DVD) or PARA_DATA[3] (DVD//) or Link Bit Clock (DVB/DSS)
38	B_FLAG	1	Error Flag (DVD) or PARA_DATA [4] (DVD//) or Link Sync (DVB/DSS)
39 B_SYNC		1	Sector / Abs Time Sync (DVD) or PARA_DATA[5] (DVD//) or Link Not Valid (DVB/DSS)
42 B_V4		1	Versatile Input Pin (Subcode Input) or PARA_DATA[7] (DVD//) or NRSS_IN (DVB/DSS)
VIDEO OUTPUT INTERFAC	Œ		
57	R_OUT	0	Red Output
56	G_OUT	0	Green Output
55	B_OUT	0	Blue Output
63	C_OUT	0	Chroma Output
64	CV_OUT	0	Composite Video Output
62	Y_OUT	0	Luma Output
59	I_REF_DAC_RGB	l	DAC Current Reference
66	I_REF_DAC_YCC	l l	DAC Current Reference
58	V_REF_DAC_RGB	1	DAC Voltage Reference
65	V_REF_DAC_YCC	1	DAC Voltage Reference
117	OSD_ACTIVE	1/0	OSD Active
118	PIXCLK_27MHz	ı	System Clock Input
51	HSYNC	1/0	Horizontal Sync
52	ODD/EVEN	1/0	Vertical Sync
AC-3/MPEG1-2 AUDIO OUT	TPUT INTERFACE		
43	SCLK	0	Serial Bit Clock
44	PCM_OUT0	0	Audio Serial Output Data 0
24	PCM_OUT1	0	Audio Serial Output Data 1
21	PCM_OUT2	0	Audio Serial Output Data 2
45	PCM_CLK	I/O	PCM Clock In or Out
46	LRCLK	0	Left/Right Clock
	SPDIF_OUT	0	SPDIF Output

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Туре	Function
EXTERNAL INTERRUPTS			
23, 25	IRQ[0:1]	ŀ	External Interrupts
PROGRAMMABLE I/O ANI	D ALTERNATE FUNCTION	(see De	evice Configuration Chapter)
15	PIO0 [0]	I/O	General Purpose I/O or PARA_SYNC (DVD//Front End) or Sc1Data (Smart Card 1 Data I/O)
16	PIO0 [3]	1/0	General Purpose I/O or PARA_REQ (DVD//Front End) or Sc1Clk (Smart Card 1 Clock)
17	PIO0 [4]	1/0	General Purpose I/O or PARA_STR (DVD//Front End) or Sc1RST (Smart Card 1 Reset)
20	PIO0 [5]	1/0	General Purpose I/O or PARA_DATA[0] (DVD//Front End) or Sc1Cmd V _{CC} (Smart Card 1 Voltage Enable)
21	PIO0 [6]	1/0	General Purpose IO or Sc1DataDir (Smart Card 1 Dir)
22	PIO0 [7]	I/O	General Purpose I/O or PARA_DATA[1] (DVD//Front End) or Sc1Detect(Smart Card 1 Detect)
9	PIO1 [0]	1/0	General Purpose I/O or I ² C Data
10	PIO1 [2]	I/O	General Purpose I/O or I ² C Clock
198, 199	PIO1 [3:4]	1/0	General Purpose IO
11	PIO1 [5]	1/0	General Purpose IO or ASC1 TXD
12	PIO1 [6]	1/0	General Purpose IO or ASC1 RXD
13	PIO1 [7]	1/0	General Purpose IO or ASC3 TXD
3	PIO2 [0]	I/O	General Purpose I/O or Sc0Data (Smart Card 0 Data I/O)
5	PIO2 [3]	1/0	General Purpose I/O or Sc0Clk (Smart Card 0 Clock)
6	PIO2 [4]	1/0	General Purpose I/O or Sc0RST (Smart Card 0 Reset)
7	PIO2 [5]	I/O	General Purpose I/O or Sc0CmdV _{CC} (Smart Card 0 Voltage Enable)
8	PIO2 [7]	I/O	General Purpose I/O or Sc0Detect (Smart Card 0 Detect)
201	PIO3 [0]	1/0	General Purpose IO or OSLink In
202	PIO3 [1]	1/0	General Purpose IO or OSLink Out
203	PIO3 [2]	1/0	General Purpose IO or CPUReset
204	PIO3 [3]	1/0	General Purpose IO or CPU Analyse
205	PIO3 [4]	1/0	General Purpose IO or ErrorOut
206, 207, 2	PIO3 [5:7]	1/0	General Purpose IO
191-197	PIO4 [0:6]	1/0	General Purpose IO
14	PIO4 [7]	9	General Purpose IO or ASC3 RXD
JTAG INTERFACE			
188	TCK	1	Test Clock
186	TDI	ı	Test Data Input
189	TDO	0	Test Data Input
187	TMS	ı	Test Mode Select
190	TRST	ı	Test Reset
SYSTEM USE			
28	PWM2	0	PWM2 Output
27	PWM1/BOOTFROMROM	0/1	PWM1 Output or Configuration Oslink Pins
26	PWM0/OSLINK_SEL	O/I	PWM0 Output or Boot from ROM during Reset
29	RST	1	Reset
116	AUXCLK	0	Auxilary Clock for Any Purpose

II - PIN DESCRIPTION (continued)

II.2 - Pin List (continued)

Pin	Name	Туре	Function
SDRAM INTERFACE			
78-81, 69, 70-74, 82, 83	AD[0:11]	0	SDRAM Address Bus
92-94, 97-101, 106-109, 112-115	DQ[0:15]	I/O	SDRAM Data (Lower Byte)
84, 85	SDCS[0:1]	0	SDRAM Chip Selects
89	SDCAS	0	SDRAM CAS
88	SDRAS	0	SDRAM RAS
90	SDWE	0	SDRAM Write Enable
104	MEMCLKIN	l I	SDRAM Memory Clock Input
76	MEMCLKOUT	0	SDRAM Memory Clock Output
91	DQML	0	DQ Mask Enable (Lower)
105	DQMU	0	DQ Mask Enable (Upper)
XTERNAL MEMORY INTE	RFACE		
161-170, 173-183	ADR[1:21]	1/0	External Memory Address Bus
141-148, 151-158	DATA[0:15]	1/0	External Memory Data Bus
128	RAS1/HOLDREQ	0	DRAM RAS or reserved
136	WAIT/READY	1/0	External Wait States or Reserved
133	R/W/DMAACK	1/0	DRAM R/W Strobe or Reserved
121, 122	BE[0:1]	0	Byte enable
129	CAS0/HOLDACK	O/I	DRAM CAS or Reserved
132	CAS1/DMAREQ	0	DRAM CAS or Reserved
124-126	CE[1:3]	0	Chip Select for Banks 1 - 3
135	CS	I	Reserved
137	PROCCLK	1/0	ST20 Clock or Reserved
127	RAS0/CE0	0	DRAM RAS or Chip Select for Bank 0
134	DMAXFER	l	Reserved
138	PPC_MODE	1	Reserved
123	OE	1/0	Output Enable or Reserved
DAV/P1394 INTERFACE			
30	TEST1	1/0	DATA_RX/STROBE_TX (SDAV Mode) or SDAV_CLK (P1394 Mode)
31 TEST2		1/0	STROBE_RX/DATA_TX (SDAV Mode) or DATA_IN/DATA_OUT (P1394 Mode)
32	TEST3	1/0	Direction (SDAV Mode) or DATA_VALID In/Out(P1394 Mode)
MISCELLANEOUS			
41	TEST5	0	NRSS_OUT (DVB/DSS)

III - FUNCTIONAL DESCRIPTION

III.1 - Functional Modules

Figure 1 shows the subsystem modules that make up the STi5505. These modules are outlined below.

III.1 - CPU

The Central Processing Unit (CPU) on the STi5505 is the ST20-C2 32-bit processor core. It contains instruction processing logic, instruction and data pointers and an operand register. It directly accesses the high speed on-chip SRAM memory, which can store data or programs, and uses the Caches to reduce access time to off chip program and data memory.

The processor can access memory via the general purpose External Memory Interface (EMI) or via the SDRAM EMI which is shared with the MPEG decoder.

III.2 - Memory Subsystem

The STi5505 on-chip SRAM memory system provides 160 Mbytes/s internal data bandwidth, supporting pipelined 2 cycles internal memory access at 25ns cycle times. The STi5505 memory system consists of 2 Kbytes of SRAM, 2Kbytes of instruction cache, a 2Kbytes data cache that can be programmed to be SRAM, and an external memory interface (EMI).

The STi5505 product has 2 Kbytes of on-chip SRAM. The advantage of this is the ability to store time critical code on chip, for instance interrupt routines, software kernels or device drivers, and even frequently used data without these being flushed from the caches.

The instruction and data caches are direct mapped with a write-back system for the data cache and support burst accesses to the external memories for refill and write-back which are effective for increasing performance with page-mode and SDRAM memories.

The STi5505 EMI controls access to the external memory and peripherals while the SDRAM EMI provides access to the SDRAM buffer for the MPEG decoders, ST20 and DMA peripherals.

The STi5505 EMI can access a 16 Mbytes (or greater if DRAM is used) physical address space in each of the four general purpose memory banks, and provides sustained transfer rates of up to 80 Mbytes/s. Peripherals that support an asynchronous data acknowledge are supported as is an external Power PC which can share the bus with the STi5505 and access the SDRAM buffer through the device.

High memory bandwidths up to 200 Mbytes/s can be supported by the SDRAM EMI.

The STi5505 internal memory interconnect provides buffering and arbitration of memory access requests to sustain very high throughput of memory

III.3 - Syste m Services Module

The STi5505 system services module includes:

- Phase locked loop (PLL) accepts 27MHz input and generates all the internal high frequency clocks needed for the CPU and the OS-Link.
- test access port JTAG compatible.
- Diagnostics controller accessed via the JTAG port providing:
- Bootstrapping during development
- Hardware breakpoint and watchpoint
- Real time trace
- External LSA triggering support.

III.4 - Serial Communications

To facilitate the connection of this system the front end device and other peripherals, two UARTs (ASCs) are included in the device. The UARTs provide an asynchronous serial interface.

The UART can be programmed to support a range of baud rates and data formats, for example, data size, stop bits and parity. Two synchronous serial communications (SSC) interfaces are provided on the device. These can be used for a remote control device for example via an I2C or SPI bus.

III.5 - Interrupt Subsystem

The STi5505 interrupt subsystem supports eight prioritized interrupt levels. Two external interrupt pins are provided. Level assignment logic allows any of the internal or external interrupts to be assigned and, if necessary, share any interrupt level.

III.6 - Front End Interf ace & DVD Decryption

The front end interface accepts sectors in the case of DVD, MPEG-1 system stream in the case of VCD and PCM data for CD-DA applications on an I2S interface. In the case of VCD and CD-DA disks the subcode information is input via a simple asynchronous serial interface similar to a UART.

The bitstream and subcode stream then pass through a "sector processor" block which handles sector filtering in the case of DVD and sectorizing using the subcode stream for VCD and CD-DA systems.

III - FUNCTIONAL DESCRIPTION (continued)

The block also handles overspeed processing for all systems. The capturing of CD-DA sectors is based on a flywheel tiner to improve robusters by concealing erros in the subcode stream. For DVD the data, having had sector headers removed, then passes through a DVD conformant de-cryption stage and is written into any of the system memories using a programmable DMA engine. When a subcode stream is present it is locally buffered, by subcode block and can be read by the CPU for subsequent processing, if required.

III.7- PWM and counter module

This unit includes three separate pulse width modulator (PWM) generators using a shared counter, and three timer compare and capture channels sharing a second counter.

The counters can be clocked from a pre-scaled internal clock or from a pre-scaled external clock via the capture clock input and the event on which the timer value is captured is also programmable.

The PWM counters are 8-bit with 8-bit registers to set the output high time. The capture/compare counter and the compare and capture registers are 32-bit.

III.8 - Parallel Programmable IO module

40 bits of parallel I/O are provided. 34 of then are connected to actual PIO pins. Each bit is programmable as an output or an input. The output can be configured as a totem pole or open drain driver. Input compare logic is provided which can generate an interrupt on any change on any input bit.

Many pins of the STi5505 device are multi-function and can either be configured as PIO or connected to an internal peripheral signal.

III.9 - MPEG Video decoder

The video decoder is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60 Hz and 720 x 576 x 50 Hz. Picture format conversion for display is performed by vertical and horizontal filters. User-defined bitmaps may be superimposed on the display picture through use of the on-screen display function.

III.10 - PAL/NTSC encoder

The digital encoder which is integrated in the STi5505 converts a multiplexed 4:2:2 YUV stream into a standard analog baseband PAL/NTSC signal and into RGB analog components. The encoder can also perform closed-caption, CGMS or teletext encoding

and allows MacrovisionTM 7.01/6.1 copy protection.

III.11 - MPEG-2 Audio / Dolby AC-3 Decoder

The audio decoder is a Dolby AC-3 decoder capable of decoding both 5.1 and 2 channel DVD comformant bitstreams. The decoder also handles MPEG-1 (layers 1 & 2) and MPEG-2 layer 2 (6 channels). Downmix to 2 channels is possible for Dolby and MPEG standards with optional pro-logic encoding.

The decoder directly accepts MPEG-2 PES streams as input. The decoder is capable of supporting IEC6958-IEC61937 formatted outputs for AC-3 and MPEG audio, linear PCM (left & right, 16, 18, 20 & 24 bits), zero output (Mute mode) and PCM audio.

FLASH AM39LV160DT

GENERAL DESCRIPTION

The Am29LV160D is a 16 Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in 48-ball FBGA, 44-pin SO, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15-DQ0; the byte-wide (x8) data appears on DQ7-DQ0. This device is designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. A 12.0 V V_{PP} or 5.0 V_{CC} are not required for write or erase operations. The device can be programmed in standard EPROM programmers.

The device offers access times of 70, 90, and 120 ns, allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a single 3.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The Am29LV160D is entirely command set compatible with the JEDEC single-power-supply Flash standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the Embedded Program algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The Unlock Bypass mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the Embedded Erase algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The sector erase architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

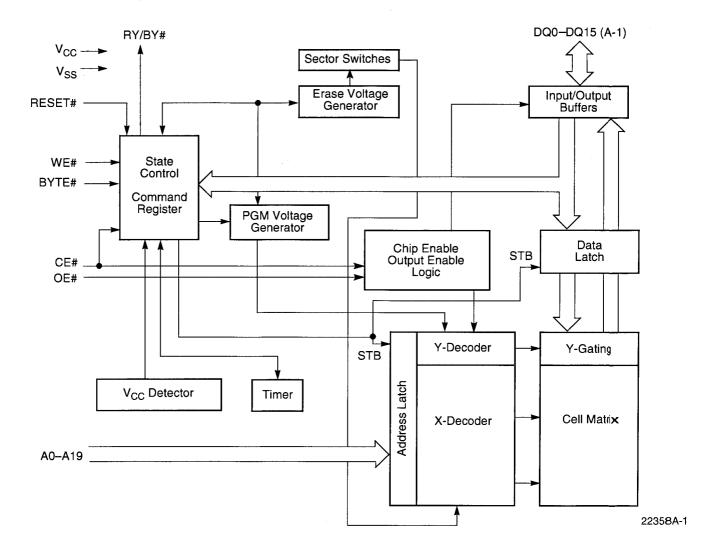
The Erase Suspend/Erase Resume feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The hardware RESET# pin terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

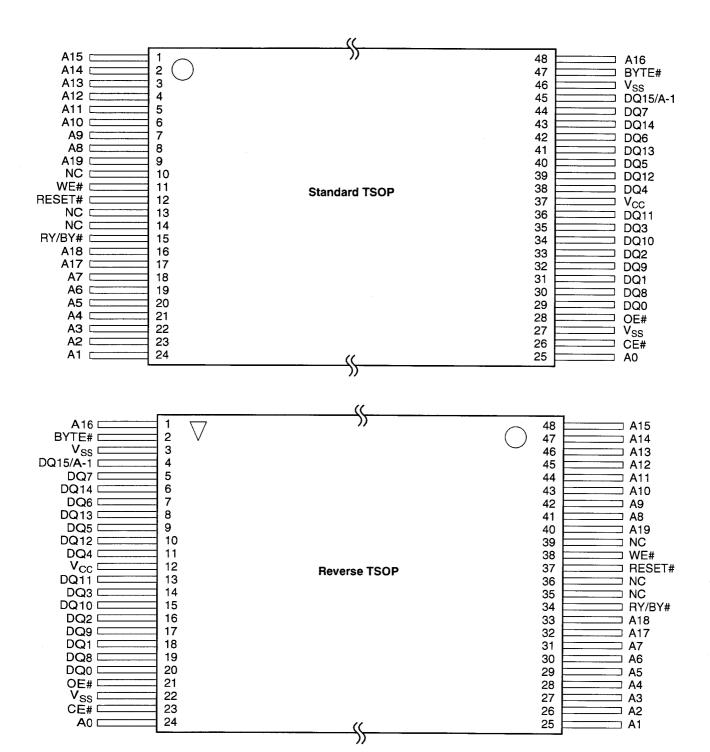
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the automatic sleep mode. The system can also place the device into the standby mode. Power consumption is greatly reduced in both these modes.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

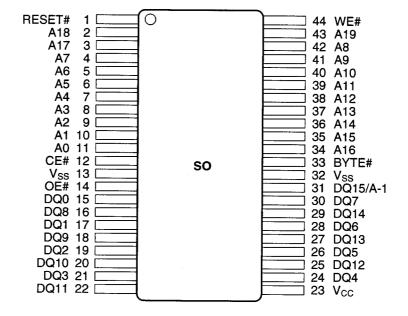
BLOCK DIAGRAM



CONNECTION DIAGRAMS



CONNECTION DIAGRAMS



PIN CONFIGURATION

A0-A19 = 20 addresses

DQ0-DQ14 = 15 data inputs/outputs

DQ15/A-1 = DQ15 (data input/output, word mode),

A-1 (LSB address input, byte mode)

BYTE# Selects 8-bit or 16-bit mode

CE# Chip enable OE# Output enable WE# Write enable

RESET# Hardware reset pin RY/BY#

Ready/Busy output (N/A SO 044)

 V_{CC} = 3.0 volt-only single power supply

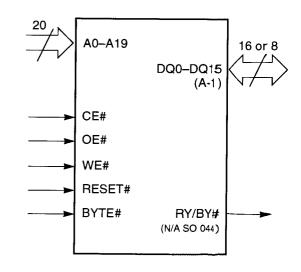
(see Product Selector Guide for speed

options and voltage supply tolerances)

 V_{SS} Device ground

NC Pin not connected internally

LOGIC SYMBOL



IC7300; IC7400; IC7403: DRAM

GM71VS18163CL

Description

The GM71V(S)18163C/CL is the new generation dynamic RAM organized 1,048,576 * Extended Data Out Mode Capability x 16 bit. GM71V(S)18163C/CL has realized *Single Power Supply (3.3V+/-0.3V) higher density, higher performance and various * Fast Access Time & Cycle Time functions by utilizing advanced CMOS process technology. The GM71V(S)18163C/CL offers Extended Data out(EDO) Mode as a high speed access mode. Multiplexed address inputs permit the GM71V(S)18163C/CL to be packaged in standard 400 mil 42pin plastic SOJ, and standard 400mil 44(50)pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

Features

- * 1,048,576Words x 16 Bit Organization

(Unit: ns)

	trac	tcac	trc	t HPC
GM71V(S)18163C/CL-5	50	13	84	20
GM71V(S)18163C/CL-6	60	15	104	25
GM71V(S)18163C/CL-7	70	18	124	30

* Low Power

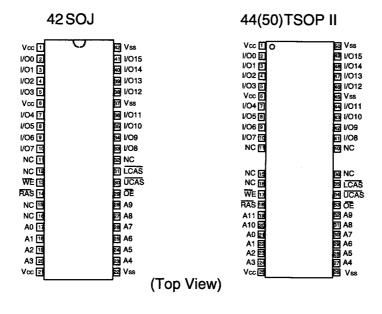
Active: 684/612/540mW (MAX)

Standby: 7.2mW (CMOS level: MAX)

0.869W (L-version: MAX)

- * RAS Only Refresh, CAS before RAS Refresh, Hidden Refresh Capability
- * All inputs and outputs TTL Compatible
- * 1024 Refresh Cycles/16ms
- * 1024 Refresh Cycles/128ms (L-version)
- * Self Refresh Operation (L-version)
- * Battery Back Up Operation (L-version)
- * 2 CAS byte Control

Pin Configuration



Pin Description

Pin	Function	Pin	Function
A0-A9	Address Inputs	WE	Read/Write Enable
A0-A9	Refresh Address Inputs	ŌĒ	Output Enable
I/O0-I/O15	Data-In/Out	Vcc	Power (+3.3V)
RAS	Row Address Strobe	Vss	Ground
UCAS, LCAS	Column Address Strobe	NC	No Connection

EMPIRE(SAA6750H)

FEATURES

- Digital YUV input according to "ITU-T 601" and to "ITU-T 656"
- NTSC and PAL (720 pixel × 480 lines at 60 Hz and 720 pixel × 576 lines at 50 Hz)
- Integrated colour conversion 4:2:2 to 4:2:0
- Integrated format conversion to SIF format (optional)
- Real time MPEG2 Simple Profile at Main Level (SP@ML) encoding
- IP frame or I frame only encoding supported
- Programmable Group Of Pictures (GOP) size
- Integrated motion estimation, half pixel accuracy, search range 128 × 128 pixels
- Motion compensated noise reduction
- Elementary stream data output compliant to MPEG2 standard ("ISO 13818-2")
- Constant Bit-Rate (CBR) and Variable Bit-Rate (VBR) supported
- Bitstream output compatible to 16-bit parallel interface with Motorola (68xxx like) or Intel (xxx86 like) protocol style
- Adaptable to dedicated applications by embedded software
- Standard software package available (refer to software specification)
- No external host processor required
- · High speed real time port for processor co-processor applications
- Only 4 x 4 Mbit external DRAM required
- I²C-bus controlled
- Single external video clock 27 MHz
- Power supply 3.3 V
- Digital inputs 5 V tolerant
- Boundary Scan Test (BST) supported.



GENERAL DESCRIPTION

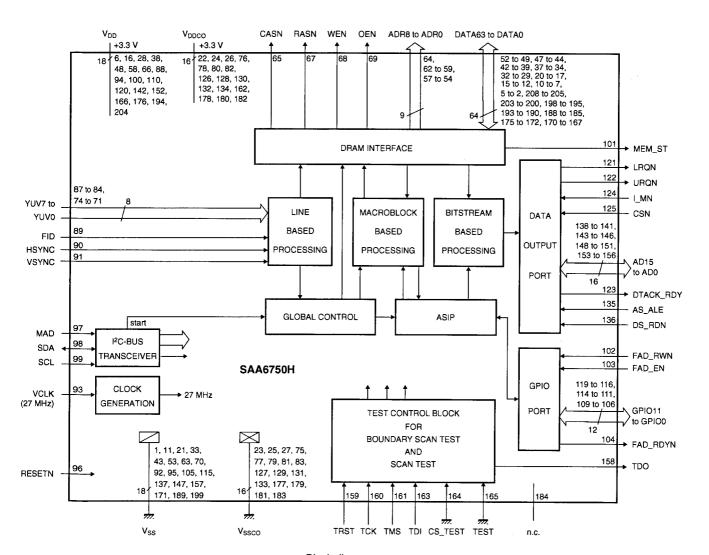
2.1 General

The SAA6750H is a new approach towards a stand-alone MPEG2 video encoder IC. It combines high quality SP at ML compliant real time encoding with cost-effectiveness, allowing for the first time the use of an MPEG2 encoder IC in applications and markets with a high cost pressure. This has been achieved by means of a number of innovations in architecture and algorithms developed by the Philips Research Laboratories. E.g.:

- The unique motion estimation algorithm supports highly efficient encoding by using only I frame and IP frame mode. B frames need not be used. This leads to a significantly smaller internal circuitry and also reduces DRAM memory requirements from at least4 to 2 Mbyte. In addition, the absence of B frames simplifies editing of the compressed data stream.
- The patented, motion-compensated temporal noise filtering which was developed by Philips for professional equipment reduces noise in the input video before compression is performed. This technique gives visible improvements in picture quality, especially in the field of home recordings with noisy signal sources where this has proved to be of significant benefit.

Internally the SAA6750H uses a hardware solution for data compression and a specially developed highperformance processor for control purposes. This programmable embedded Digital Signal Processor (DSP) approach allows Philips to tailor various customized sels of functions for this IC. Contact Philips for information on available software packages.

Blockdiagram



Block diagram.

Pin Description

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{SS}	1	ground	_	ground for pad ring
DATA28	2	input/output	3	DRAM data interface bit 28
DATA29	3	input/output	3	DRAM data interface bit 29
DATA30	4	input/output	3	DRAM data interface bit 30
DATA31	5	input/output	3	DRAM data interface bit 31
V _{DD}	6	supply	_	supply voltage for pad ring
DATA32	7	input/output	3	DRAM data interface bit 32
DATA33	8	input/output	3	DRAM data interface bit 33
DATA34	9	input/output	3	DRAM data interface bit 34
DATA35	10	input/output	3	DRAM data interface bit 35
V _{SS}	11	ground	_	ground for pad ring
DATA36	12	input/output	3	DRAM data interface bit 36
DATA37	13	input/output	3	DRAM data interface bit 37
DATA38	14	input/output	3	DRAM data interface bit 38
DATA39	15	input/output	3	DRAM data interface bit 39
V_{DD}	16	supply	_	supply voltage for pad ring
DATA40	17	input/output	3	DRAM data interface bit 40
DATA41	18	input/output	3	DRAM data interface bit 41
DATA42	19	input/output	3	DRAM data interface bit 42
DATA43	20	input/output	3	DRAM data interface bit 43
V _{SS}	21	ground		ground for pad ring
V _{DDCO}	22	supply	-	supply voltage for core logic
V _{SSCO}	23	ground	_	ground for core logic
V _{DDCO}	24	supply	-	supply voltage for core logic
V _{SSCO}	25	ground		ground for core logic
V_{DDCO}	26	supply	-	supply voltage for core logic
V _{SSCO}	27	ground	_	ground for core logic
V_{DD}	28	supply	_	supply voltage for pad ring
DATA44	29	input/output	3	DRAM data interface bit 44
DATA45	30	input/output	3	DRAM data interface bit 45
DATA46	31	input/output	3	DRAM data interface bit 46
DATA47	32	input/output	3	DRAM data interface bit 47
V _{SS}	33	ground		ground for pad ring
DATA48	34	input/output	3	DRAM data interface bit 48
DATA49	35	input/output	3	DRAM data interface bit 49
DATA50	36	input/output	3	DRAM data interface bit 50
DATA51	37	input/output	3	DRAM data interface bit 51
V_{DD}	38	supply	_	supply voltage for pad ring
DATA52	39	input/output	3	DRAM data interface bit 52

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
DATA53	40	input/output	3	DRAM data interface bit 53
DATA54	41	input/output	3	DRAM data interface bit 54
DATA55	42	input/output	3	DRAM data interface bit 55
V _{SS}	43	ground	-	ground for pad ring
DATA56	44	input/output	3	DRAM data interface bit 56
DATA57	45	input/output	3	DRAM data interface bit 57
DATA58	46	input/output	3	DRAM data interface bit 58
DATA59	47	input/output	3	DRAM data interface bit 59
V_{DD}	48	supply	-	supply voltage for pad ring
DATA60	49	input/output	3	DRAM data interface bit 60
DATA61	50	input/output	3	DRAM data interface bit 61
DATA62	51	input/output	3	DRAM data interface bit 62
DATA63	52	input/output	3	DRAM data interface bit 63 (MSB)
V _{SS}	53	ground	_	ground for pad ring
ADR0	54	output/3-state	3	DRAM address interface bit 0 (LSB)
ADR1	55	output/3-state	3	DRAM address interface bit 1
ADR2	56	output/3-state	3	DRAM address interface bit 2
ADR3	57	output/3-state	3	DRAM address interface bit 3
V_{DD}	58	supply	_	supply voltage for pad ring
ADR4	59	output/3-state	3	DRAM address interface bit 4
ADR5	60	output/3-state	3	DRAM address interface bit 5
ADR6	61	output/3-state	3	DRAM address interface bit 6
ADR7	62	output/3-state	3	DRAM address interface bit 7
V_{SS}	63	ground	_	ground for pad ring
ADR8	64	output/3-state	3	DRAM address interface bit 8 (MSB)
CASN	65	output/3-state	6	DRAM column address strobe (active LOW)
V_{DD}	66	supply		supply voltage for pad ring
RASN	67	output/3-state	3	DRAM row address strobe (active LOW)
WEN	68	output/3-state	3	DRAM write enable (active LOW)
OEN	69	output/3-state	3	DRAM chip select (active LOW)
V_{SS}	70	ground	-	ground for pad ring
YUV0	71	input	_	video input signal bit 0 (LSB)
YUV1	72	input	_	video input signal bit 1
YUV2	73	input	-	video input signal bit 2
YUV3	74	input	_	video input signal bit 3
V _{SSCO}	75	ground	_	ground for core logic
V _{DDCO}	76	supply	-	supply voltage for core logic
V _{SSCO}	77	ground		ground for core logic
V _{DDCO}	78	supply		supply voltage for core logic
V _{SSCO}	79	ground	_	ground for core logic

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V _{DDCO}	80	supply	_	supply voltage for core logic
V _{SSCO}	81	ground	_	ground for core logic
V _{DDCO}	82	supply	_	supply voltage for core logic
V _{SSCO}	83	ground	_	ground for core logic
YUV4	84	input	_	video input signal bit 4
YUV5	85	input	-	video input signal bit 5
YUV6	86	input	_	video input signal bit 6
YUV7	87	input		video input signal bit 7 (MSB)
V _{DD}	88	supply	_	supply voltage for pad ring
FID	89	input	_	odd/even ?eld identi?cation
HSYNC	90	input	_	horizontal reference signal
VSYNC	91	input	_	vertical reference signal
V _{SS}	92	ground	_	ground for pad ring
VCLK	93	input	_	video clock input (27 MHz)
V_{DD}	94	supply	_	supply voltage for pad ring
V _{SS}	95	ground	1	ground for pad ring
RESETN	96	input	-	hard reset input (active LOW)
MAD	97	input	_	module address (I ² C-bus)
SDA	98	input/open drain output	6	serial data input/output (I ² C-bus)
SCL	99	input/open drain output	_	serial clock input (I ² C-bus)
V_{DD}	100	supply	_	supply voltage for pad ring
MEM_ST	101	output/3-state	3	do not use in the application (reserved)
FAD_RWN	102	input	_	ASIP port data read/write
FAD_EN	103	input	_	ASIP port data enable
FAD_RDYN	104	open drain output	3	ASIP port data ready (active LOW)
V _{SS}	105	ground	_	ground for pad ring
GPIO0	106	input/output	3	ASIP port data bit 0 (LSB)
GPIO1	107	input/output	3	ASIP port data bit 1
GPIO2	108	input/output	3	ASIP port data bit 2
GPIO3	109	input/output	3	ASIP port data bit 3
V_{DD}	110	supply	_	supply voltage for pad ring
GPIO4	111	input/output	3	ASIP port data bit 4
GPIO5	112	input/output	3	ASIP port data bit 5
GPIO6	113	input/output	3	ASIP port data bit 6
GPIO7	114	input/output	3	ASIP port data bit 7
V _{SS}	115	ground	_	ground for pad ring
GPIO8	116	input/output	3	ASIP port data bit 8
GPIO9	117	input/output	3	ASIP port data bit 9
GPIO10	118	input/output	3	ASIP port data bit 10
GPIO11	119	input/output	3	ASIP port data bit 11 (MSB)

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
V_{DD}	120	supply	_	supply voltage for pad ring
LRQN	121	open drain output	3	output port lower watermark interrupt request (active LOW)
URQN	122	open drain/3-state	3	output port upper watermark interrupt request (active LOW)
DTACK_RDY	123	open drain output	3	output port data transfer acknowledge/ready/request
I_MN	124	input	_	output port Intel/Motorola bus style selection input (active LOW); with internal pull-up resistor
CSN	125	input	_	output port chip select for external address mode (active LOW); with internal pull-up resistor
V_{DDCO}	126	supply		supply voltage for core logic
V _{SSCO}	127	ground		ground for core logic
V_{DDCO}	128	supply		supply voltage for core logic
V _{SSCO}	129	ground	-	ground for core logic
V _{DDCO}	130	supply	-	supply voltage for core logic
V _{SSCO}	131	ground	-	ground for core logic
V_{DDCO}	132	supply	_	supply voltage for core logic
V _{SSCO}	133	ground	-	ground for core logic
V_{DDCO}	134	supply	_	supply voltage for core logic
AS_ALE	135	input	-	output port address strobe/address latch enable
DS_RDN	136	input	_	output port data strobe/read
V _{SS}	137	ground	_	ground for pad ring
AD15	138	input/output	3	output port multiplexed address/data line bit 15 (MSB)
AD14	139	input/output	3	output port multiplexed address/data line bit 14
AD13	140	input/output	3	output port multiplexed address/data line bit 13
AD12	141	input/output	3	output port multiplexed address/data line bit 12
V_{DD}	142	supply		supply voltage for pad ring
AD11	143	input/output	3	output port multiplexed address/data line bit 11
AD10	144	input/output	3	output port multiplexed address/data line bit 10
AD9	145	input/output	3	output port multiplexed address/data line bit 9
AD8	146	input/output	3	output port multiplexed address/data line bit 8
V _{SS}	147	ground	_	ground for pad ring
AD7	148	input/output	3	output port multiplexed address/data line bit 7/data bus bit 7 (MSB)
AD6	149	input/output	3	output port multiplexed address/data line bit 6/data bus bit 6
AD5	150	input/output	3	output port multiplexed address/data line bit 5/data bus bit 5
AD4	151	input/output	3	output port multiplexed address/data line bit 4/data bus bit 4
V_{DD}	152	supply	-	supply voltage for pad ring
AD3	153	input/output	3	output port multiplexed address/data line bit 3/data bus bit 3
AD2	154	input/output	3	output port multiplexed address/data line bit 2/data bus bit 2
AD1	155	input/output	3	output port multiplexed address/data line bit 1/data bus bit 1
AD0	156	input/output	3	output port multiplexed address/data line bit 0 (LSB)/data bus bit 0 (LSB)

157 158		(mA)	DESCRIPTION
150	ground	<u> </u>	ground for pad ring
136	output	3	boundary scan test data output; pin not active during normal operation; with 3-state output; note 2
159	input	_	boundary scan test reset; pin must be set to LOW for normal operation; with internal pull-up resistor; notes 2 and 3
160	input	_	boundary scan test clock; pin must be set to LOW during normal operation; with internal pull-up resistor; note 2
161	input	-	boundary scan test mode select; pin must ?oat or set to HIGH during normal operation; with internal pull-up resistor; note 2
162	supply	_	supply voltage for core logic
163	input	-	boundary scan test data input; pin must ?oat or set to HIGH during normal operation; with internal pull-up resistor; note 2
164	input	-	test mode for the internal RAMs; pin must be set to LOW during normal operation
165	input	_	test mode; pin must be set to LOW during normal operation
166	supply		supply voltage for pad ring
167	input/output	3	DRAM data interface bit 0 (LSB)
168	input/output	3	DRAM data interface bit 1
169	input/output	3	DRAM data interface bit 2
170	input/output	3	DRAM data interface bit 3
171	ground	 	ground for pad ring
172	input/output	3	DRAM data interface bit 4
173	input/output	3	DRAM data interface bit 5
174	input/output	3	DRAM data interface bit 6
175	input/output	3	DRAM data interface bit 7
176	supply	-	supply voltage for pad ring
177	ground	_	ground for core logic
178	supply	<u> </u>	supply voltage for core logic
179	ground		ground for core logic
180	supply	-	supply voltage for core logic
181	ground	-	ground for core logic
182	supply	_	supply voltage for core logic
183		_	ground for core logic
184	_	 	reserved pin; do not connect
185	input/output	3	DRAM data interface bit 8
186	input/output	3	DRAM data interface bit 9
187		3	DRAM data interface bit 10
		3	DRAM data interface bit 11
		 	ground for pad ring
		 	DRAM data interface bit 12
			DRAM data interface bit 13
	160 161 162 163 164 165 166 167 168 169 170 171 172 173 174 175 176 177 180 181 182 183 184 185 186	160 input 161 input 162 supply 163 input 164 input 165 input 166 supply 167 input/output 169 input/output 170 input/output 171 ground 172 input/output 173 input/output 174 input/output 175 input/output 176 supply 177 ground 178 supply 179 ground 180 supply 181 ground 182 supply 183 ground 184 – 185 input/output 186 input/output 187 input/output 188 input/output 189 ground 189 ground	160 input - 161 input - 162 supply - 163 input - 164 input - 165 input - 166 supply - 167 input/output 3 168 input/output 3 170 input/output 3 171 ground - 172 input/output 3 173 input/output 3 174 input/output 3 175 input/output 3 176 supply - 179 ground - 180 supply - 181 ground - 182 supply - 183 ground - 184 - - 185 input/output 3 186 input/output 3 187 input/output 3 188 input/output

SYMBOL	PIN	INPUT/OUTPUT ⁽¹⁾	I _{max} (mA)	DESCRIPTION
DATA14	192	input/output	3	DRAM data interface bit 14
DATA15	193	input/output	3	DRAM data interface bit 15
V_{DD}	194	supply	_	supply voltage for pad ring
DATA16	195	input/output	3	DRAM data interface bit 16
DATA17	196	input/output	3	DRAM data interface bit 17
DATA18	197	input/output	3	DRAM data interface bit 18
DATA19	198	input/output	3	DRAM data interface bit 19
V _{SS}	199	ground	_	ground for pad ring
DATA20	200	input/output	3	DRAM data interface bit 20
DATA21	201	input/output	3	DRAM data interface bit 21
DATA22	202	input/output	3	DRAM data interface bit 22
DATA23	203	input/output	3	DRAM data interface bit 23
V_{DD}	204	supply	_	supply voltage for pad ring
DATA24	205	input/output	3	DRAM data interface bit 24
DATA25	206	input/output	3	DRAM data interface bit 25
DATA26	207	input/output	3	DRAM data interface bit 26
DATA27	208	input/output	3	DRAM data interface bit 27

Notes

- 1. All input, I/O (in input mode), output (in 3-state mode) and open drain output pins are 5.0 V tolerant.
- 2. In accordance with the "IEEE 1149.1" standard.
- 3. Special functionality of pin TRST:
 - a) For board designs without boundary scan implementation, pin TRST must be connected to ground.
 - b) Pin TRST provides easy initialization of the internal BST circuit. By applying a LOW it can be used to force the internal Test Access Port (TAP) controller to the Test-Logic-Reset state (normal operation) at once.

The 208 pins are divided in following groups:

Video input port (11 pins):

8 data pins

3 control pins.

Data output port (23 pins):

16 data pins

7 control pins.

GPIO port (15 pins):

12 data pins

3 control pins.

DRAM (77 pins):

64 data pins

9 address pins

4 control pins.

Others (14 pins):

1 video clock input pin

3 pins related to the I2C-bus

1 pin for reset control

7 pins for test purposes

1 pin not connected

1 pin for internal test purposes.

Supply (68 pins):

16 core supply pins

18 I/O cell supply pins

16 core ground pins

18 I/O cell ground pins.

SAA7118

FEATURES

The SAA7118 is a video capture device for application at the image port of VGA controller, with following feature high lights:

Video Acquisition/ Clock

Up to sixteen analog CVBS, split as desired (All of the CVBS inputs optionally can be used to convert VSB

Up to eight analog Y+C inputs, split as desired

Up to four analog component inputs, with embedded or separate sync, split as desired

Four on-chip anti-aliasing filters in front of the ADC's

Automatic Clamp Control (ACC) for CVBS, Y and C (or VSB) and component signal

Switchable white Peak Control

Four 9 Bit Low Noise CMOS analog-to-digital converters at two-fold ITU-656 oversampling (27 MHz)

Digitized CVBS or Y+C-signals are available on the expansion port

Fully programmable static gain or automatic gain control, matching to the particular signal properties

On-Chip Line Locked Clock Generation according ITU601

Requires only one crystal (32.11 or 24.576 MHz) for all

Horizontal and vertical Sync Detection

Video Decoder

Digital PLL for Synchronization and Clock Generation from all Standards and Non-Standard Video Sources e.g. consumer grade VTR

Digital PLL for Synchronization and Clock Generation from all Standards and Non- Standard Video Sources e.g. consumer grade VTR

Automatic detection of any supported colour standard Luminance and chrominance signal processing for PAL BGDHIN, Combination-PAL N, PAL M, NTSC M, NTSC-Japan, NTSC 4.43 and SECAM

Adaptive 2/4-line comb filter for two dimensional chrominance/luminance-separation, also with VTR signals

- Increased Luminance and Chrominance Bandwidth for all PAL and NTSC-standards
- Reduced cross colour and cross luminance artefacts PAL delay line for correcting PAL phase errors

Brightness Contrast Saturation (BCS)- adjustment, separately for composite and baseband signals

User programmable sharpness control

Fast Blanking between component inputs and a CVBS input through a dedicated pin

Detection of copy-protected signals acc. to the Macrovision standard, indicating level of protection

Independent Gain and Offset - adjustment for raw data path

Component Video Processing

Synchronous Component Video (RGB) input via fast blanking, YCbCr input

Digital matrix

Video Scaler

Horizontal and Vertical Down-Scaling and Up-Scaling to randomly sized windows

Horizontal and Vertical Scaling range: variable zoom to 1/64 (icon)

(Note: H and V zoom are restricted by the transfer data

Anti-Alias- and Accumulating Filter for Horizontal Scaling

Vertical Scaling with Linear Phase Interpolation and Accumulating Filter for Anti-Aliasing (6 bit phase accuracy)

Horizontal Phase Correct Up- and Down-Scaling for improved signal quality of scaled data, especially for compression and video phone applications, with 6 bit phase accuracy (1.2 nsec step width)

Two independent programming sets for scaler part, to define two "ranges" per field or sequences over frames

Fieldwise switching between Decoder-part and Expansion port (X-port) input

Brightness, contrast and saturation controls for scaled outputs

VBI-Data Decoder and Slicer

versatile VBI-data decoder, slicer, clock regeneration and byte synchronization

e.g. for WST, NABST, Close Caption, WSS, etc.

Audio Clock Generation

Generation of a field locked Audio Master Clock to support a constant number of audio clocks per video field

SAA7118

Generation of an audio serial and left/right (channel) clock signal

Digital I/O Interfaces

Real Time signal port (R - port), incl. continuous line locked reference clock and real time status information supporting RTC level 3.1 (refer to external document "RTC Functional Specification" for details)

Bidirectional Expansion Port (X - port) with half duplex functionality (D1), 8-bit YCbCr

- output from Decoder part, real time and unscaled, or
- input to Scaler part, e.g. video from MPEG-decoder (extension to 16 bit possible)

Video Image port (I - port) configurable for 8 - bit data (extension to 16 bit possible) in Master Mode (own clock), or Slave Mode (external clock), with auxiliary timing and hand shake signals

Discontinuous data streams supported

32-word * 4 Byte FIFO register for video output data 28-word * 4 Byte FIFO register for decoded VBI output

Scaled 4:2:2, 4:1:1, 4:2:0, 4:1:0 YCbCr output Scaled 8-bit luminance only and raw CVBS data output sliced, decoded VBI data output

Miscellaneous

Power On Control

5 V tolerant digital inputs and I/O ports

Software controlled power saving stand-by modes supported

Programming via serial I²C-bus, full read-back ability by an external controller, bit rate up to 400 kbit/s

Boundary Scan Test circuit complies to the IEEE Std. 1149.b1 -1994

BGA156 package

APPLICATIONS

Multimedia

Digital Television

Image Processing

Video Phone

PC- Editing cards

PC- Tuner cards

GENERAL DESCRIPTION

Philips X-VIP is a new Multistandard Comb Filter Video Decoder chip with additional component processing, providing high quality, optionally scaled, video.

The SAA7118 is a combination of a four channel analog preprocessing circuit including source selection. anti-aliasing filter and A/D-converter, an automatic clamp and gain control, a Clock Generation Circuit (CGC), a Digital Multi Decoder Standard containing two-dimensional chrominance/luminance separation by an adaptive comb filter and a high performance scaler, including variable horizontal and vertical up and down scaling and a Brightness- Contrast- Saturation- Control

It is a highly integrated circuit for Desktop Video and similar applications. The decoder is based on the principle of line-locked clock decoding and is able to decode the colour of PAL, SECAM and NTSC signals into ITU-601 compatible colour component values. The SAA7118 accepts as analog inputs CVBS or S-Video (Y+C) from TV or VCR sources, including weak and distorted signals, as well as baseband component signals YCbCr or RGB. An expansion port (X-port) for digital video (bi-directional half duplex, D1 compatible) is also supported to connect to MPEG or video phone codec. At the so called image port (I-port) the 7118 supports 8 (16) bit wide output data with auxiliary reference data for interfacing to VGA controllers.

The target application for SAA7118 is to capture and optionally scale video images, to be provided as digital video stream through the image port of a VGA controller. for capture to system memory, or just to provide digital baseband video to any picture improvement processing.

SAA7118 also provides means for capturing the serially coded data in the vertical blanking interval (VBI-data). Two principal functions are available:

- to capture raw video samples, after interpolation to the required output data rate, via the scaler and
- a versatile data slicer (data recovery) unit.

SAA7118 incorporates also a field locked audio clock generation. This function ensures that there is always the same number of audio samples associated with a field, or a set of fields. This prevents the loss of sychronization between video and audio, during capture or playback.

All of the A/D- converters may be used to digitize a VSB signal for further for further decoding; a dedicated output port and a selectable VSB clock input is provided.

The circuit is controlled via I2C-bus (full write / read capability for all programming registers, bit rate up to 400 kbits/s)

SAA7118

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DDx}	digital supply voltage	3.0	3.3	3.6	V
V _{DDCx}	digital core supply voltage	3.0	3.3	3.6	V
V_{DDA}	analog supply voltage	3.1	3.3	3.5	V
T _{amb}	mb ambient temperature		-	70	°C
P _{A+D}	analog and digital power dissipation ⁽¹⁾	-	t.b.d.	-	W

Note

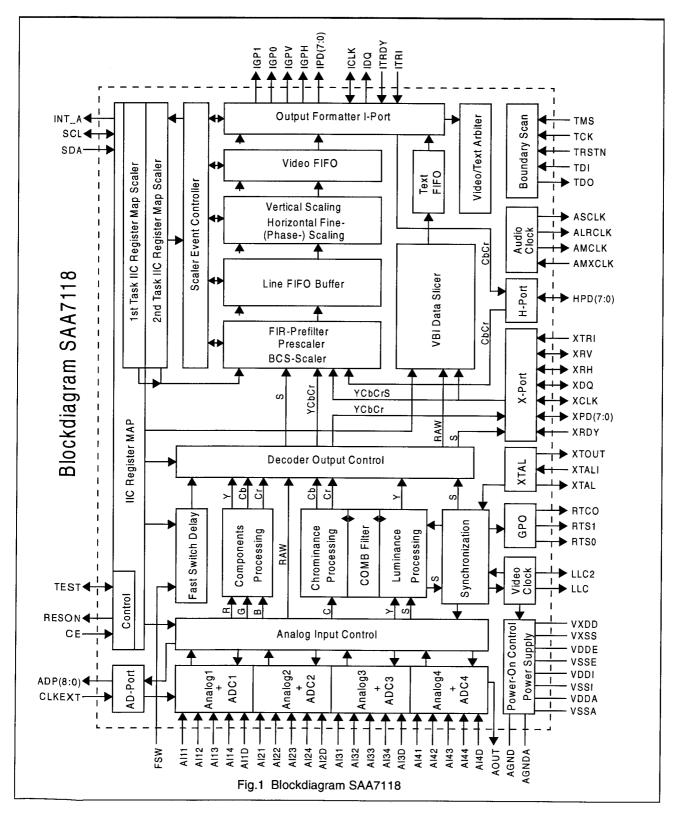
1. Power consumption is measured in CVBS-input mode (only one ADC active) and 8 bit image port output mode, expansion port is tristated

5 ORDERING AND PACKAGE INFORMATION

EXTENDED TYPE	PACKAGE					
NUMBER	PINS	PIN POSITION	MATERIAL	CODE		
SAA7118	156	BGA156	Plastic	SOT 472-1(BB3)		

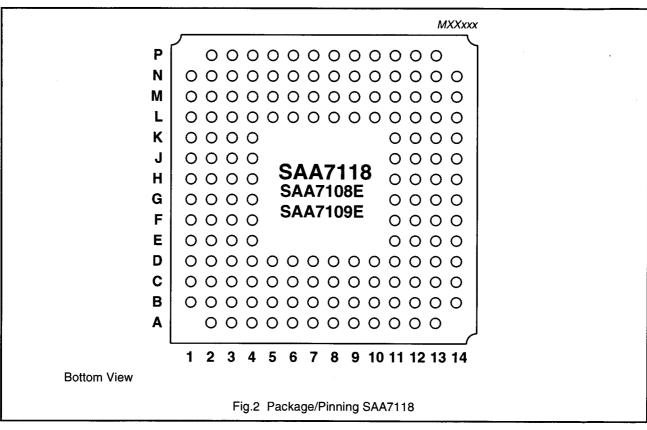
SAA7118

6 SYSTEM BLOCK DIAGRAM



SAA7118

PINNING AND CONFIGURATION



Pinning List

Table 1 Pinning List SAA7118

PIN	NAME	TYPE	DESCRIPTION				
A02	XTOUT	0	Crystal oscillator output signal				
A03	XTAL	0	Connect output pin for quartz				
A04	vxss	Р	round for crystal oscillator				
A05	TDO	0	est Data Output for Boundary Scan Test (2)				
A06	XRDY	0	atus flag or ready signal from scaler				
A07	XCLK	I/O	lock I/O expansion port				
A08	XPD0	I/O	SB of expansion port bus				
A09	XPD2	1/0	ISB-5 of expansion port bus				
A10	XPD4	1/0	SB-3 of expansion port bus				
A11	XPD6	I/O	B-1 of expansion port bus				
A12	TEST5	l/pu	Scan test input; do not connect				
A13	TEST3	l/pu	Scan test input; do not connect				
B01	Al41	I	alog input #41				
B02	RES1	0	eserved pin for future extensions or testing, do not connect				
B03	VXDD	Р	Supply for crystal oscillator				

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PIN	NAME	TYPE	DESCRIPTION			
B04	XTALI	ı	Connect input pin for quartz			
B05	TDI	l/pu	Test Data Input for Boundary Scan Test (with internal pull-up) (2)			
B06	TCK	I/pu	Test Clock for Boundary Scan Test (with internal pull-up) (2)			
B07	XDQ	1/0	Data qualifier for expansion port			
B08	XPD1	1/0	MSB-6 of expansion port bus			
B09	XPD3	I/O	MSB-4 of expansion port bus			
B10	XPD5	I/O	MSB-2 of expansion port bus			
B11	XTRI	I	X-port output control signal; effects (XPD[7:0], XRH, XRV, XDQ and XCLK)			
B12	TEST4	0	Scan test output; do not connect			
B13	RES2	NC	Reserved pin for future extensions or testing, do not connect			
B14	RES3	NC	Reserved pin for future extensions or testing, do not connect			
C01	VSSA4	Р	Ground for analog input Al4x			
C02	AGND	Р	Analog Signal Ground			
C03	RES4	NC	eserved pin for future extensions or testing, do not connect			
C04	RES5	NC	eserved pin for future extensions or testing, do not connect			
C05	VDDE1	Р	Digital supply peripheral cells			
C06	TRSTN	l/pu	Test ReSeT Not for Boundary Scan Test (with internal pull-up) (1)			
C07	XRH	1/0	Horizontal reference expansion-port			
C08	VDDI1	Р	Digital supply core			
C09	VDDE2	Р	Digital supply peripheral cells			
C10	VDDI2	Р	Digital supply core			
C11	XPD7	1/0	MSB of expansion port bus			
C12	RES6	NC	Reserved pin for future extensions or testing, do not connect			
C13	RES7	NC	Reserved pin for future extensions or testing, do not connect			
C14	TEST2	l/pu	Scan test input; do not connect			
D01	Al43	I	Analog input #43			
D02	Al42	1	Analog input #42			
D03	Al4D	1/0	Differential input for Al4x			
D04	VDDA4	Р	Supply for analog input Al4x			
D05	VSSE1	Р	Digital ground peripheral cells			
D06	TMS	l/pu	Test Mode Select for Boundary Scan Test or Scan Test (with internal pull-up) (2)			
D07	VSSI1	Р	Digital ground core (Substrate connection)			
D08	XRV	1/0	Vertical reference for expansion-port			
D09	VSSE2	Р	Digital ground peripheral cells			
D10	VSSI2	Р	Digital ground core			
D11	VSSE3	Р	Digital ground peripheral cells			
D12	VDDE3	Р	Digital supply peripheral cells			
D13	TEST1	l/pu	Scan test input; do not connect			
D14	HPD0	I/O	LSB of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port			
E01	Al44	1	Analog input #44			

SAA7118

PIN	NAME	TYPE	DESCRIPTION			
E02	VDDA4A	Р	Supply for analog input Al4x			
E03	Al31	I	Analog input #31			
E04	VSSA3	Р	Ground for analog input Al3x			
E11	HPD1	I/O	MSB-6 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port			
E12	HPD3	I/O	MSB-4 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port			
E13	HPD2	I/O	MSB-5 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port			
E14	HPD4	I/O	MSB-3 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port			
F01	Al3D	I/O	Differential input for Al3x			
F02	Al32	I	Analog input #32			
F03	Al33	ı	Analog input #33			
F04	VDDA3	Р	Supply for analog input Al3x			
F11	VSSI3	P	Digital ground core			
F12	VDD13	Р	Digital supply core			
F13	HPD5	1/0	MSB-2 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port			
F14	HPD6	1/0	MSB-1 of H-port bus, extended CbCr input for X-port, extended CbCr output for I-port			
G01	Al34	ı	Analog input #34			
G02	VDDA3A	Р	Supply for analog input Al3x			
G03	Al22	İ	Analog input #22			
G04	Al21	ı	Analog input #21			
G11	VSSE4	Р	Digital ground peripheral cells			
G12	IPD1	0	MSB-6 of Image port bus			
G13	HPD7	1/0	MSB of H-port bus, extended CbCr input for X-port, extended CbCr ₀utput for I-port			
G14	IPD0	0	LSB of Image port bus			
H01	Al2D	I/O	Differential input for Al2x			
H02	Al23	1	Analog input #23			
H03	VSSA2	Р	Ground for analog input Al2x			
H04	VDDA2	Р	Supply for analog input Al2x			
H11	IPD2	0	MSB-5 of Image port bus			
H12	VDDE4	Р	Digital supply peripheral cells			
H13	IPD4	0	MSB-3 of Image port bus			
H14	IPD3	0	MSB-4 of Image port bus			
J01	VDDA2A	P	Supply for analog input Al2x			
J02	Al11	ı	Analog input #11			
J03	Al24	ı	Analog input #24			
J04	VSSA1	Р	Ground for analog input Al1x			

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PIN	NAME	TYPE	DESCRIPTION			
J11	VSSI4	Р	Digital ground core			
J12	VDDI4	Р	Digital supply core			
J13	IPD6	0	MSB-1 of Image port bus			
J14	IPD5	0	MSB-2 of Image port bus			
K01	Al12	1	Analog input #12			
K02	Al13	ı	Analog input #13			
K03	Al1D	1/0	Differential input for Al1x			
K04	VDDA1	P	Supply for analog input Al1x			
K11	IPD7	0	MSB of Image port bus			
K12	IGPH	0	Multi purpose horizontal reference signal			
K13	IGP1	0	General purpose signal #1			
K14	IGPV	0	Multi purpose vertical reference signal			
L01	VDDA1A	Р	Supply for analog input Al1x			
L02	AGNDA	Р	Analog signal ground connection			
L03	Al14	1	Analog input #14			
L04	VSSE5	Р	Digital ground peripheral cells			
L05	VSSI5	Р	Digital ground core			
L06	ADP6	0	MSB-2 of Direct A/D-converted output bus (VSB)			
L07	ADP3	0	MSB-5 of Direct A/D-converted output bus (VSB)			
L08	VSSE6	Р	Digital ground peripheral cells			
L09	VSSI6	Р	Digital ground core			
L10	RTCO	O/st/pd (3)	RTC output; strap to LOW (4k7) for first I ² C slave address 42h strap to HIGH (4k7) for second I ² C slave address 40h			
L11	VSSE7	Р	Digital ground peripheral cells			
L12	ITRI	1/0	Image-port control signal, effects all Image port pins			
L13	IDQ	0	Data qualifier for image port			
L14	IGP0	0	General purpose signal #0			
M01	AOUT	0	Analog test output (not for use in application)			
M02	VSSA0	Р	Ground for internal clock generator			
M03	VDDA0	Р	Supply for internal clock generator			
M04	VDDE5	Р	Digital supply peripheral cells			
M05	VDDI5	Р	Digital supply core			
M06	ADP7	0	MSB-1 of Direct A/D-converted output bus (VSB)			
M07	ADP2	0	MSB-6 of Direct A/D-converted output bus (VSB)			
M08	VDDE6	Р	Digital supply peripheral cells			
M09	VDDI6	Р	Digital supply core			
M10	RTS0	0	Real time status or sync information			
M11	VDDE7	Р	Digital supply peripheral cells			
M12	AMXCLK	I	Audio Master External clock input			

SAA7118

PIN	NAME	TYPE	DESCRIPTION
M13	FSW	l/pd	Fast Switch (Blanking), with internal pull-down, inserts component inputs into CVBS signal
M14	ICLK	1/0	Clock output signal for image-port, LCLK of LPB image port mode, or optional asynchronous backend clock input
N01	RES8	NC	Reserved pin for future extensions or testing, do not connect
N02	RES9	l/pu	Reserved pin for future extensions or testing, do not connect
N03	RES10	I/pd	Reserved pin for future extensions or testing, do not connect
N04	CE	l/pu	Chip Enable or Reset with internal pull-up
N05	LLC2	0	Line-locked clock at half frequency (13.5 MHz nominal)
N06	CLKEXT	ı	External clock input intended for A/D-conversion of VSB signals (36 MHz)
N07	ADP5	0	MSB-3 of Direct A/D-converted output bus (VSB)
N08	ADP0	0	LSB of Direct A/D-converted output bus (VSB)
N09	SCL	I	I ² C Serial Clock
N10	RTS1	0	Real time status or sync information
N11	ASCLK	0	Audio serial clock
N12	ITRDY	Ī	Target Ready for image port bus
N13	RES11	NC	Reserved pin for future extensions or testing, do not connect
N14	RES12	NC	Reserved pin for future extensions or testing, do not connect
P02	RES13	1/0	Reserved pin for future extensions or testing, do not connect
P03	EXMCLR	l/pd	External Mode Clear, with internal pull-down
P04	LLC	0	Line-locked clock (27 MHz nominal)
P05	RESON	0	Reset Output Not signal
P06	ADP8	0	MSB of Direct A/D-converted output bus (VSB)
P07	ADP4	0	MSB-4 of Direct A/D-converted output bus (VSB)
P08	ADP1	0	MSB-7 of Direct A/D-converted output bus (VSB)
P09	INT_A	O/od	I ² C interrupt flag (Low if any enabled status bit has changed)
P10	SDA	I/O/od	I ² C Serial Data
P11	AMCLK	0	Audio Master clock, must be less than half the crystal clock frequency
P12	ALRCLK	O/st/pd	Audio left/right clock, strap to LOW (4k7) for 24.576 MHz crystal strap to HIGH (4k7) for 32.11 MHz crystal (3)
P13	TEST0	l/pu	Scan test input; do not connect

TYPE description:

I=input, O=output, P=power, NC=not connected, st=strapping, pu=pull-up, pd=pull-down, od=open drain

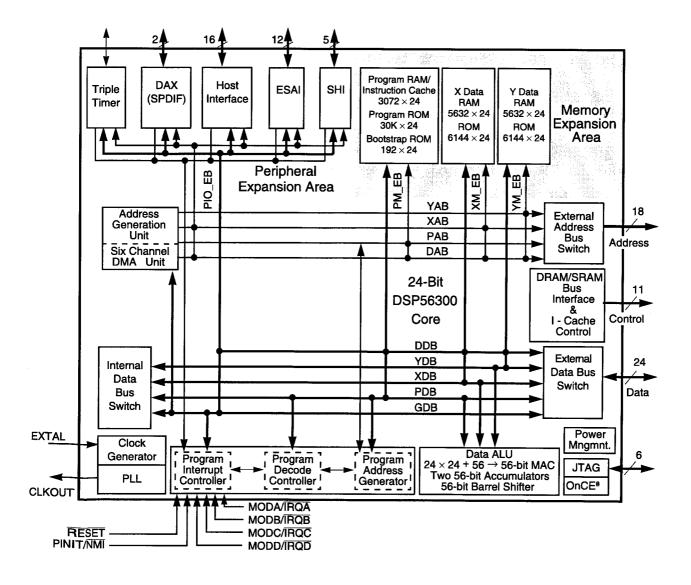
- 1. This pin provides easy initialization of BST circuitry. TRSTN can be used to force the TAP (Test Access Port) controller to the Test-Logic-Reset state (normal operation) at once
- 2. According to the IEEE1149.b1-1994 standard the pads TDI and TMS are input pads with a internal pull-up transist or and TDO a tri-state output pad. TCK, TRSTN are also built with internal pile-up
- 3. Strapping remark: If the strapping pin is unused, the internal pull-down resistor is sufficient for strap function. If pin is used in an application, an external strapping resistor (4,7k) is necessary to get a certain strap function.

9.9.9 IC7703: DSP56362

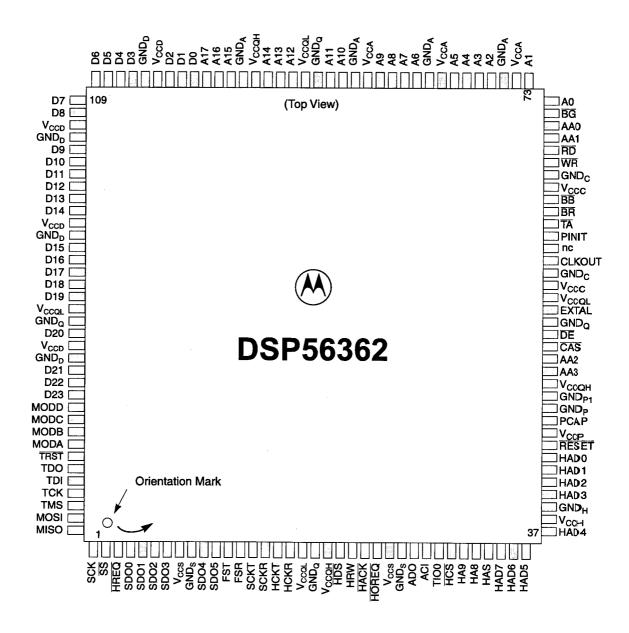
DSP56362

24-BIT AUDIO DIGITAL SIGNAL PROCESSOR

Motorola designed the DSP56362 to support digital audio applications requiring digital audio compression and decompression, sound field processing, acoustic equalization, and other digital audio algorithms. The DSP56362 uses the high performance, single-clock-per-cycle DSP56300 core family of programmable CMOS digital signal processors (DSPs) combined with the audio signal processing capability of the Motorola Symphony^a DSP family, as shown in Figure 1. This design provides a two-fold performance increase over MotorolaOs popular Symphony family of DSPs while retaining code compatibility. Significant architectural enhancements include a barrel shifter, 24-bit addressing, instruction cache, and direct memory access (DMA). The DSP56362 offers 80/100 million instructions per second (MIPS) using an internal 80/100 MHz clock at 3.3 V.



SIGNAL DESCRIPTION



PIN NUMBER	SIGNAL NAME	ТҮРЕ	SIGNAL DESCRIPTION
1	SCK/SCL	ľO	SPI Serial Clock/I ² C Serial Clock
2	SS/HA2	I	SPI Slave Select/I ² C Slave Address 2
3	HREQ	I/O	Host Request
4	SDO0/PC11	I/O	Serial Data Output1/Port C10
5	SDO1/PC10	I/O	Serial Data Output0/Port C11
6	SDO2/SDI3/PC9	1/0	Serial Data Output2/Serial Data Input3/Port C9
7	SDO3/SDI2/PC8	1/0	Serial Data Output3/Serial Data Input2/Port C8
8	V _{CCS}	I	SHI, ESAI, DAX and Timer Power
9	GNDs	_	SHI, ESAI, DAX and Timer Ground
10	SDO4/SDI1/PC7	I/O	Serial Data Output4/Serial Data Input1/Port C7
11	SDO5/SDI0/PC6	I/O	Serial Data Output5/Serial Data Input0/Port C6
12	FST/PC4	I/O	Frame Sync for Transmitter/Port C4
13	FSR/PC1	1/0	Frame Sync for Receiver/Port C1
14	SCKT/PC3	I/O	Transmitter Serial Clock/Port C3
15	SCKR/PC0	I/O	Receiver Serial Clock/Port C0
16	HCKT/PC5	I/O	High Frequency Clock for Transmitter/Port C5
17	HCKR/PC2	I/O	High Frequency Clock for Receiver/Port C2
18	V _{CCQL}	I	Quiet Core Low Power
19	GND _Q	1	Quiet Ground
20	V _{CCQH}	I	Quiet External High Power
21	HDS/HWR/PB12	I/O	Host Data Strobe/Host Write Data/Port B12
22	HRW/HRD/PB11	I/O	Host Read Write/Host Read Data/Port B11
23	HACK/HRRQ/PB 15	I/O	
24	HOREQ/HTRQ/PB 14	I/O	Host Acknowledge/Receive Host Request Host Request/Transmit Host Request/Port B14
25	V _{CCS}	I	SHI, ESAI, DAX and Timer Power
26	GND _S	1	SHI, ESAI, DAX and Timer Ground
27	ADO/PD1	I/O	Digital Audio Data Output/Port D1
28	ACI/PD0	I/O	Audio Clock Input/Port D0
29	TIO0	I/O	<u> </u>
30	HCS/HA10/PB13	I/O	Timer 0 Schmitt-Trigger Input/Output Host Chip Select/Host Address10/Port B13
31	HA2/HA9/PB10	I/O	
32	HA1/HA8/PB9	I/O	Host Address Input2/Host Address9/Port B10 Host Address Input1/Host Address8/Port B9
33	HA0/HAS/PB8	I/O	
33	H7/HAD7/PB7	I/O	Host Address Input0/Host Address Strobe/Port B8 Host Data7/Host Address7/Port B7
35	H6/HAD6/PB6	I/O	
36			Host Data6/Host Address6/Port B6
37	H5/HAD5/PB5	I/O	Host Data5/Host Address5/Port B5
	H4/HAD4/PB4	I/O	Host Data4/Host Address4/Port B4
38 39	CND	I	Host Power Host Ground
	GND _H	T/O	
40 41	H3/HAD3/PB3	I/O	Host Data3/Host Address3/Port B3
	H2/HAD2/PB2	I/O	Host Data2/Host Address2/Port B2
42	H1/HAD1/PB1	I/O	Host Data1/Host Address1/Port B1
43	H0/HAD0/PB0	I/O	Host Data0/Host Address0/Port B0
44	RESET	I	Reset
45	V _{CCP}	I	PLL Power
46	PCAP	I	PLL Capacitor
47	GND _P		PLL Ground
48	GND _{P1}	7	PLL Ground 1
49	V _{CCQH}	I	Quiet External High Power
50	AA3/RAS3	0	Address Attribute3/Row Address Strobe 3
51	AA2/RAS2	0	Address Attribute2/Row Address Strobe 2
<u>52</u>	CAS	0	Column Address Strobe
53	DE	I	Debug Event
54	GND _Q		Quiet Ground
55	EXTAL	I	External Clock Input

PIN NUMBER	SIGNAL NAME	TYPE	SIGNAL DESCRIPTION
111	V _{CCD}	I	Data Bus Power
112	GND_D		Data Bus Ground
113	D9	I/O	Data Bus
114	D10	I/O	Data Bus
115	D11	I/O	Data Bus
116	D12	I/O	Data Bus
117	D13	I/O	Data Bus
118	D14	I/O	Data Bus
119	V_{CCD}	I	Data Bus Power
120	GND_D		Data Bus Ground
121	D15	I/O	Data Bus
122	D16	I/O	Data Bus
123	D17	I/O	Data Bus
124	D18	I/O	Data Bus
125	D19	I/O	Data Bus
126	V_{CCQL}	I	Quiet Core Low Power
127	GND ₀		Quiet Ground
128	D20	I/O	Data Bus
129	V _{CCD}	I	Data Bus Power
130	GND_D		Data Bus Ground
131	D21	I/O	Data Bus
132	D22	I/O	Data Bus
133	D23	I/O	Data Bus
134	MODD/IRQD	I	Mode Select D/External Interrupt Request D
135	MODC/IRQC	I	Mode Select C/External Interrupt Request C
136	MODB/IRQB	I	Mode Select B/External Interrupt Request B
137	MODA/IRQA	I	Mode Select A/External Interrupt Request A
138	TRST	I	Test Reset
139	TDO	0	Test Data Output
140	TDI	I	Test Data Input
141	TCK	Ī	Test Clock
142	TMS	I	Test Mode Select
143	MOSI/HA0	I/O	SPI Master-Out-Slave-In/I ² C Slave address 0
144	MISO/SDA		SPI Master-In-Slave-Out/I ² C Data and acknowledge

9.9.10 IC7700: SRAM

CY7C1019V33

Features

- · High speed
 - $-t_{AA} = 12, 15, 20 \text{ ns}$
- V_{CC} = 3.3V ± 10%
- · Low active power
 - -432 mW (max.)
 - -288 mW (L version)
- Low CMOS standby power
 - -18 mW (max.)
 - 7.2 mW (L version)
- 2.0V Data Retention
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with CE₁, CE₂, and OE options

Functional Description

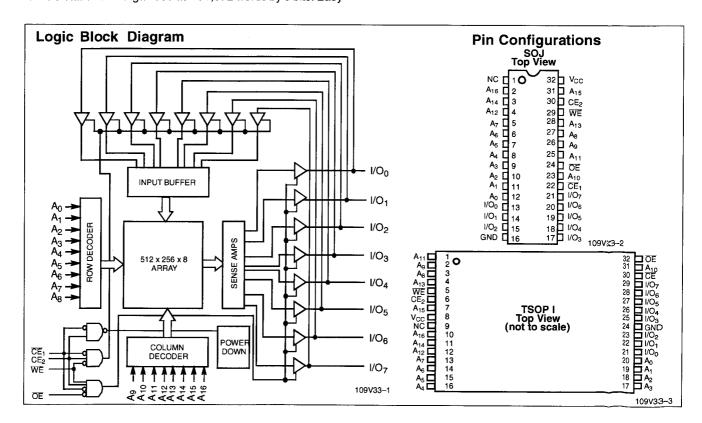
The CY7C109V33/CY7C1009V33 is a high-performance CMOS static RAM organized as 131,072 words by 8 bits. Easy

memory expansion is provided by an active LOW chip enable (CE₁), an active HIGH chip enable (CE₂), an active LOW output enable (OE), and three-state drivers. Writing to the device is accomplished by taking chip enable one (CE1) and write enable (WE) inputs LOW and chip enable two (CE2) input HIGH. Data on the eight I/O pins (I/O $_0$ through I/O $_7$) is then written into the location specified on the address pins (A₀ through A₁₆).

Reading from the device is accomplished by taking chip enable one (\overline{CE}_1) and output enable (\overline{OE}) LOW while forcing write enable (WE) and chip enable two (CE2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O₀ through I/O₇) are placed in a high-impedance state when the device is deselected (CE₁ HIGH or CE₂ LOW), the outputs are disabled (OE HIGH), or during a write operation (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW).

The CY7C109V33 is available in standard 32-pin, 400-mil-wide SOJ package. The CY7C1009V33 is available in a 32-pin, 300-mil-wide SOJ package. The CY7C1009V33 and CY7C109V33 are functionally equivalent in all other respects.



9.10 IC's Divio

9.10.1 IC7101: 58PDI1394P11A

3-port physical layer interface

PDI1394P11A

1.0 FEATURES

- 3 cable interface ports
- Supports 100Mb/s and 200Mb/s transfers
- Interfaces to any 1394 standard Link Layer Controller
- 5V tolerant I/Os with Bus Hold Circuitry
- Single 3.3V supply voltage
- Arbitrated (short) Bus Reset (1394a feature)
- Fully compatible with existing 100 Mbps Phys on the market
- Prevents a TpBias voltage driven into a non-powered PDI1394P11A from erroneously powering up the part

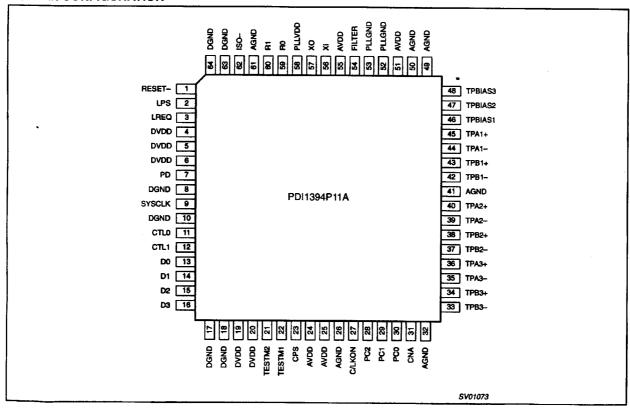
2.0 DESCRIPTION

The Philips Semiconductors PDI1394P11A is an IEEE1394-1995 compliant Physical Layer interface. The PDI1394P11A provides the analog physical layer functions needed to implement a three port node in a cable-based IEEE 1394-1995 network. Additionally, the device manages bus initialization and arbitration cycles, as well as transmission and reception of data bits. The Link Layer Controller interface is compatible with both 3V and 5V Link Controllers. While providing a maximum transmission data rate of 200 Mb/s, the PDI1394P11A is compatible with current 100 Mb/s Physical Layer ICs. The PDI1394P11A is available in the LQFP64 package.

3.0 ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
64-pin plastic LQFP	0°C to +70°C	PDI1394P11A BD	PD1394P11A BD	SOT314-2

PIN CONFIGURATION



5.0 PIN DESCRIPTION

PIN NUMBER	PIN SYMBOL	VO	NAME AND FUNCTION
1	RESET-	l*	Phy reset, active LOW
2	LPS	1*	Link Layer Controller (LLC) power status
3	LREQ	1*	Link request from controller
4	DVDD	1*	Should be connected to the LLC V _{DD} supply when a 5V LLC is connected to the Phy, and should be connected to the Phy DVDD when a 3V LLC is used.
5, 6, 19, 20	DVDD	1	Digital circuit power
7	PD	1*	Device power down input
8, 10, 17, 18, 63, 64	DGND	-	Digital circuit ground
9	SYSCLK	0,	49.152 MHz clock to link controller
11, 12	CTL[0:1]	1/0*	Link interface bi-directional control signals
13, 14, 15, 16	D[0:3]	1/0*	Link interface bi-directional data signals
22, 21	TESTM[1:2]	1.	Test/Mode Control pins 11 =1394–1995 mode 10 = 1394a mode 00/01 = Reserved
23	CPS	1	Cable power status
24, 25, 51, 55	AVDD	-	Analog circuit power
26, 32, 41, 49, 50, 61	AGND	-	Analog circuit ground
27	C/LKON	1/0*	Bus/Isochronous Resource Manager capable input, or LINK-ON signal output
30, 29, 28	PC[0:2]	1*	Power class bits 0 through 2 inputs
31	CNA	0*	Cable Not Active output
36, 40, 45	TPA[1:3]+	1/0	Port n cable pair A, positive signal
35, 39, 44	TPA[1:3]-	1/0	Port n cable pair A, negative signal
34, 38, 43	TPB[1:3]+	1/0	Port n cable pair B, positive signal
33, 37, 42	TPB[1:3]-	1/0	Port n cable pair B, negative signal
46, 47, 48	TPBIAS[1:3]	0	Cable termination voltage supplies
52, 53	PLLGND	-	PLL circuit ground
54	FILTER	1/0	PLL external filter capacitor
56	XI	1	Crystal oscillator connection
57	хо	0	Crystal oscillator connection
58	PLLVDD	-	PLL circuit power
59, 60	R[0:1]	T -	External current setting resistor
62	ISO-	l*	Link interface isolation status input

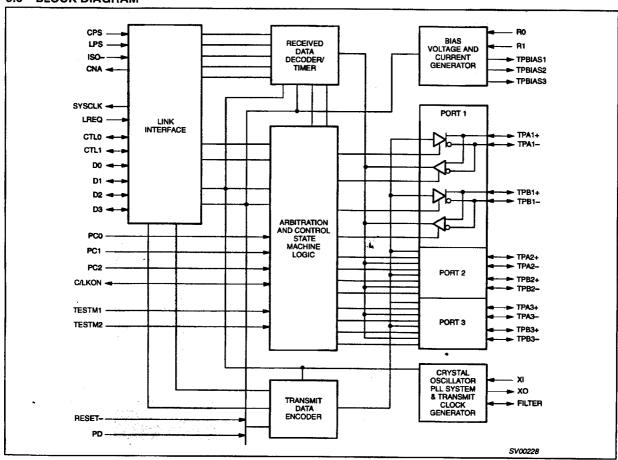
NOTE:
* Indicates 5V tolerant structure.

3-port physical layer interface

DVDR1000 /0x1 /691

PDI1394P11A

6.0 **BLOCK DIAGRAM**



7.0 FUNCTIONAL SPECIFICATION

The PDI1394P11A is an IEEE1394-1995 High Performance Serial Bus Specification compliant physical layer interface device. It provides an interface between an attached link layer controller and three 1394 cable interface ports. In addition to the interface function, the PDI1394P11A performs bus initialization and arbitration functions as well as monitoring line conditions and connection

7.1 Clocking

The PDI1394P11A utilizes a stable internal reference clock of 196.608 MHz. The reference clock is generated using an external 24.576 MHz crystal and an internal Phase Locked Loop (PLL). The PLL clock is divided down to 49.152 MHz and 98.304 MHz clock signals. The 49.152 MHz clock is used for internal logic and provided as an output to clock a link layer controller. The 196,608 MHz and 98.304 MHz clocks are used for synchronization of the transmitted strobe and data information.

7.2 Port Interfaces

The PDI1394P11A provides the transceiver functions needed to implement a three port node in a cable-based 1394 network. Each cable port incorporates two differential line transceivers. In addition to transmission and reception of packet data, the line transceivers

monitor conditions on the cable to determine connection status, data speed, and bus arbitration states.

The PDI1394P11A receives data to be transmitted over the bus from two or four parallel data paths to the Link Controller, D[0:3]. These data paths are latched and synchronized with the 49.152 MHz clock. The parallel bit paths are combined serially, encoded and transmitted at either 98.304 Mb/s or 196.608 Mb/s, depending whether the transaction is a 100 Mb/s or 200 Mb/s transfer. respectively. The transmitted data is encoded as data-strobe information, with the data information being transmitted on the TPB cable pairs and the strobe information transmitted on the TPA cable pairs.

During packet reception the TPA and TPB transmitters of the receiving cable port are disabled, and the receivers for that port are enabled. The encoded data information is received on the TPA cable pair and the strobe information is received on the TPB cable pair. The combination of the data and strobe signals is decoded to recover the receive clock signal and the serial data stream. The serial data stream is converted to two or four parallel bit streams, resynchronized to the internal 49.152 MHz clock and sent to the

3-port physical layer interface

PDI1394P11A

associated link controller. The received data is also transmitted out the other active cable ports.

The cable status, bus initialization and arbitration states are monitored through the cable interface using differential comparators. The outputs of these comparators are used by internal logic to determine cable and arbitration status. The TPA channel monitors the incoming cable common-mode voltage value during arbitration to determine the speed of the next packet transmission. The TPB channel monitors the incoming cable common-mode voltage for the

presence of the remotely supplied twisted-pair bias voltage, indicating the cable connection status.

The PDI1394P11A provides a nominal 1.85 V for driver load termination. This bias voltage, when seen through a cable by a remote receiver, is used to sense the presence of an active connection. The value of this bias voltage has been chosen to allow inter-operability between transceiver chips operating from either 5 V nominal supplies, or 3.3 V nominal supplies. This bias voltage source should be stabilized by using an external filter capacitor. When not powered, the PDI1394P11A prevents the bias voltage from erroneously powering up the part as is seen in some other Phys.

8.0 RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITION		T			
SIMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT	
V_{DD}	DC supply voltage	Source/non-source power node	2.7	3.3	3.6	V	
V _{IH}	High level input voltage	CMOS inputs	2.0		5.5	V	
V _{IL}	Low level input voltage	CMOS inputs			0.8	٧	
V _{ID-100}	Differential input voltage	Cable inputs, 100Mbit operation	142		260	mV	
V _{ID-200}	Differential input voltage	Cable inputs, 200Mbit operation	132		260	mV	
V _{ID-ARB}	Differential input voltage	Cable inputs, during arbitration	171		262	mV	
V	V _{IC-100} Common mode voltage	TPB cable inputs, 100Mbit or speed signaling OFF, source power node	1.165		2.515		
VIC-100 Common mode		TPB cable inputs, 100Mbit or speed signaling OFF, non-source power node	1.165		2.015	V	
V	P Common mode voltage	TPB cable inputs, 200Mbit or speed signaling, source power node	0.935		2.515		
V _{IC-200SP}	Common mode voltage	TPB cable inputs, 200Mbit or speed signaling, non-source power node	0.935		2.015	٧	
	Receive input jitter	TPA, TPB cable inputs, 100Mbit operation			±1.08	ns	
	neceive input jitter	TPA, TPB cable inputs, 200Mbit operation			±0.5	ns	
	December in such about	Between TPA and TPB cable inputs, 100Mbit operation			±0.8	ns	
	Receive input skew	Between TPA and TPB cable inputs, 200Mbit operation	*****		±0.55	ns	
1. //.	Outrout oursest 1 //	SYSCLK	-16		16		
IOF/IOH	Output current, I _{OL} /I _{OH}	Control, Data, CNA, C/LKON	-12		12	mA	
lo	Output current	TPBIAS outputs	-3		1.3	mA	
f _{XTAL}	Crystal frequency	Parallel resonant fundamental mode crystal	24.5735	24.576	24.5785	MHz	
T _{amb}	Operating ambient temperature range in free air		0		+70	°C	

9.10.2 IC7103: PDI1394L21

1394 full duplex AV link layer controller

PDI1394L21

1.0 FEATURES

- IEEE 1394-1995 Standard Link Layer Controller
- Hardware Support for the IEC61883 International Standard of Digital Interface for Consumer Electronics
- Interface to any IEEE 1394-1995 Physical Layer Interface
- 5V Tolerant I/Os
- Single 3.3V supply voltage
- Full-duplex isochronous operation
- Operates with 400/200/100 Mbps physical layer devices
- Dual 4K Byte FIFOs for isochronous data
- Supports single capacitor isolation mode and IEEE 1394–1995, Annex J. isolation
- 4-field deep SYT buffer added to enhance real-time isochronous synchronization using the AVFSYNC pin
- Generates its own AV port clocks under software control. Select one of three frequencies: 24.576, 12.288, or 6.144 MHz

2.0 DESCRIPTION

The PDI1394L21, Philips Semiconductors Full Duplex 1394 Audio/Video (AV) Link Layer Controller, is an IEEE 1394-1995 compliant link layer controller featuring 2 embedded AV layer interfaces. The AV layers are designed to pack and un-pack application data packets for transmission over the IEEE 1394 bus using isochronous data transfers. Because of its full duplex architecture, the PDI1394L21 is capable of receiving and transmitting isochronous data during the same bus cycle. Two 8 bit AV ports, each with its own buffer (FIFO), receive and output isochronous data for transmission and reception of bus packets. Each port can be configured to receive or transmit, however, the other port always performs the opposite function. Half duplex operation is also permitted.

The application data is packetized according to the IEC 61883 International Standard of Interface for Consumer Electronic Audio/Video Equipment. Both AV layer interfaces are byte-wide ports capable of accommodating various MPEG-2 and DVC codecs. An 80C51 compatible byte-wide host interface is provided for internal register configuration as well as performing asynchronous data transfers.

The PDI1394L21 is powered by a single 3.3V power supply and the inputs and outputs are 5V tolerant. It is available in the LQFP100 and TQFP100 packages.

3.0 QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25$ °C

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Functional supply voltage range		3.0	3.3 `	3.6	V
I _{DD}	Supply current @ V _{DD} = 3.3V	Operating		75		mA
SCLK	Device clock		49.147	49.152	49.157	MHz

4.0 ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
100-pin plastic LQFP100	0°C to +70°C	PDI1394L21BE	PDI1394L21BE	SOT407 AB15
100-pin plastic TQFP100	0°C to +70°C	PDI1394L21BP	PDI1394L21BP	SOT386 BB2

NOTE:

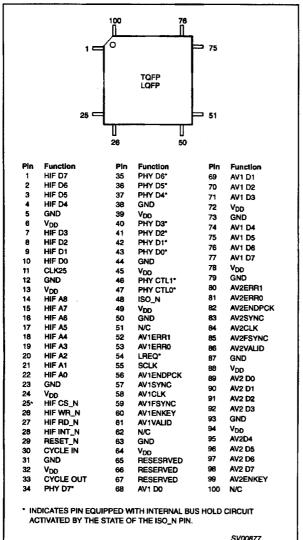
This datasheet is subject to change. Please visit our internet website www.semiconductors.philips.com/1394 for latest changes.

1

1394 full duplex AV link layer controller

PDI1394L21

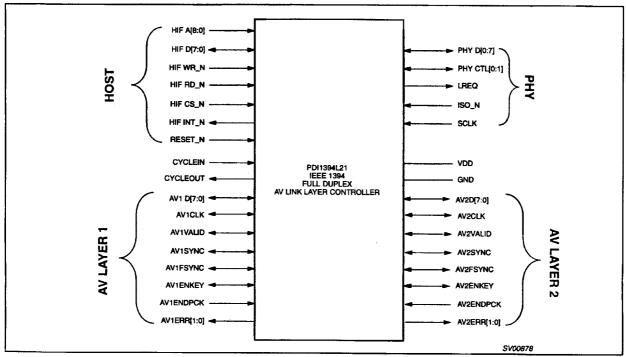
5.0 PIN CONFIGURATION



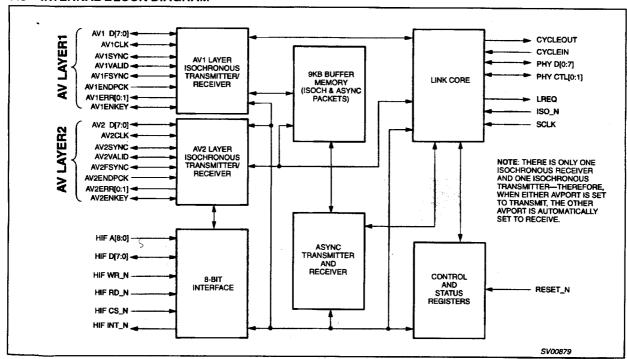
1394 full duplex AV link layer controller

PDI1394L21

FUNCTIONAL DIAGRAM



INTERNAL BLOCK DIAGRAM



P89C51RB2/P89C51RC2/ P89C51RD2

DESCRIPTION

The P89C51RB2/RC2/RD2 device contains a non-volatile 16kB/32kB/64kB Flash program memory that is both parallel programmable and serial In-System and In-Application Programmable. In-System Programming (ISP) allows the user to download new code while the microcontroller sits in the application. In-Application Programming (IAP) means that the microcontroller fetches new program code and reprograms itself while in the system. This allows for remote programming over a modem link. A default serial loader (boot loader) program in ROM allows serial In-System programming of the Flash memory via the UART without the need for a loader in the Flash code. For In-Application Programming, the user program erases and reprograms the Flash memory by use of standard routines contained in ROM.

This device executes one machine cycle in 6 clock cycles, hence providing twice the speed of a conventional 80C51. An OTP configuration bit lets the user select conventional 12 clock timing if desired.

This device is a Single-Chip 8-Bit Microcontroller manufactured in advanced CMOS process and is a derivative of the 80C51 microcontroller family. The instruction set is 100% compatible with the 80C51 instruction set.

The device also has four 8-bit I/O ports, three 16-bit timer/event counters, a multi-source, four-priority-level, nested interrupt structure, an enhanced UART and on-chip oscillator and timing circuits.

The added features of the P89C51RB2/RC2/RD2 makes it a powerful microcontroller for applications that require pulse width modulation, high-speed I/O and up/down counting capabilities such as motor control.

FEATURES

80C51 Central Processing Unit

On-chip Flash Program Memory with In-System Programming (ISP) and In-Application Programming (IAP) capability

Boot ROM contains low level Flash programming routines for downloading via the UART

Can be programmed by the end-user application (IAP)

6 clocks per machine cycle operation (standard)

12 clocks per machine cycle operation (optional)

Speed up to 20 MHz with 6 clock cycles per machine cycle (40 MHz equivalent performance); up to 33 MHz with 12 clocks per machine cycle

Fully static operation

RAM expandable externally to 64 kB

4 level priority interrupt

7 interrupt sources

Four 8-bit I/O ports

Full-duplex enhanced UART

- ± Framing error detection
- Automatic address recognition

Power control modes

- ± Clock can be stopped and resumed
- ± idle mode
- ± Power down mode

Programmable clock out

Second DPTR register

Asynchronous port reset

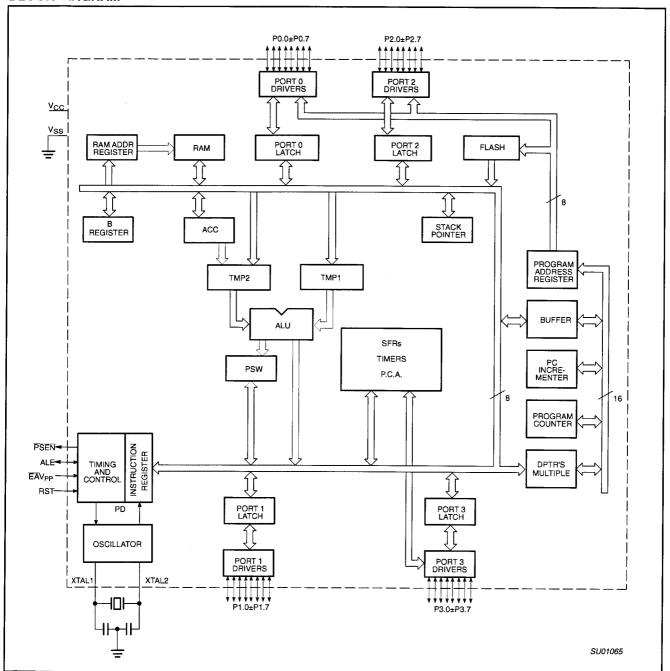
Low EMI (inhibit ALE)

Programmable Counter Array (PCA)

- ± PWM
- ± Capture/compare

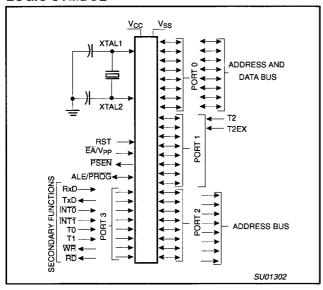
P89C51RB2/P89C51RC2/ P89C51RD2

BLOCK DIAGRAM



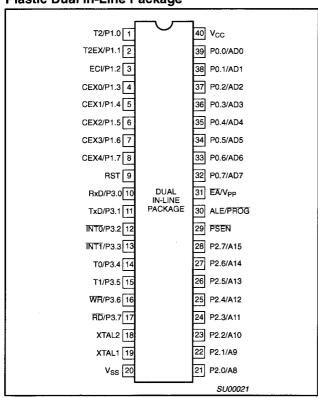
P89C51RB2/P89C51RC2/ P89C51RD2

LOGIC SYMBOL

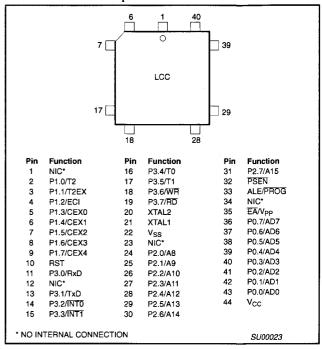


PINNING

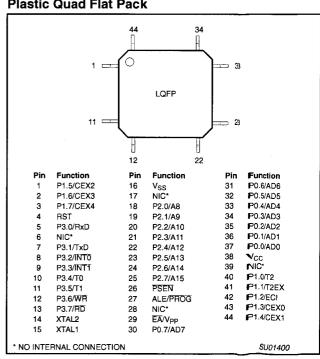
Plastic Dual In-Line Package



Plastic Leaded Chip Carrier



Plastic Quad Flat Pack



P89C51RB2/P89C51RC2/ P89C51RD2

PIN DESCRIPTIONS

MNEMONIC	Р	IN NUMBE	R	TYPE	NAME AND FUNCTION
MINEMONIC	PDIP	PLCC	LQFP] ' ' ' ' '	NAME AND FUNCTION
V_{SS}	20	22	16	1	Ground: 0 V reference.
V _{CC}	40	44	38	1	Power Supply: This is the power supply voltage for normal, idle, and power-down operation.
P0.0±0.7	39±32	43±36	37±30	I/O	Port 0: Port 0 is an open-drain, bidirectional I/O port. Port 0 pins that have 1s written to them float and can be used as high-impedance inputs. Port 0 is also the multiplexed low-order address and data bus during accesses to external program and data memory. In this application, it uses strong internal pull-ups when emitting 1s.
P1.0±P1.7	1±8	2±9	40±44, 1±3	I/O	Port 1: Port 1 is an 8-bit bidirectional I/O port with internal pull-ups on all pins except P1.6 and P1.7 which are open drain. Port 1 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 1 pins that are externally pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}).
					Alternate functions for 89C51RB2/RC2/RD2 Port 1 include:
	1	2	40	I/O	T2 (P1.0): Timer/Counter 2 external count input/Clockout (see Programmable Clock-Out)
	2	3	41	- 1	T2EX (P1.1): Timer/Counter 2 Reload/Capture/Direction Control
	3	4	42	F	ECI (P1.2): External Clock Input to the PCA
	4	5	43	1/0	CEX0 (P1.3): Capture/Compare External I/O for PCA module 0
	5	6	44	1/0	CEX1 (P1.4): Capture/Compare External I/O for PCA module 1
	6	7	1	1/0	CEX2 (P1.5): Capture/Compare External I/O for PCA module 2
	7	8	2	1/0	CEX3 (P1.6): Capture/Compare External I/O for PCA module 3
	8	9	3	1/0	CEX4 (P1.7): Capture/Compare External I/O for PCA module 4
P2.0±P2.7	21±28	24±31	18±25	I/O	Port 2: Port 2 is an 8-bit bidirectional I/O port with internal pull-ups. Port 2 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 2 pins that are externally being pulled low will source current because of the internal pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @DPTR). In this application, it uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOV @Ri), port 2 emits the contents of the P2 special function register.
					P2.7 must be a ^a l ^o to program and erase the device.
P3.0±P3.7	10±17	11, 13±19	5, 7±13	I/O	Port 3: Port 3 is an 8-bit bidirectional I/O port with internal pull-ups. Port 3 pins that have 1s written to them are pulled high by the internal pull-ups and can be used as inputs. As inputs, port 3 pins that are externally being pulled low will source current because of the pull-ups. (See DC Electrical Characteristics: I _{IL}). Port 3 also serves the special features of the 89C51RB2/RC2/RD2, as listed below:
	10	11	5	ı	RxD (P3.0): Serial input port
	11	13	7	0	TxD (P3.1): Serial output port
	12	14	8	ı	INTO (P3.2): External interrupt
	13	15	9	ı	INT1 (P3.3): External interrupt
	14	16	10	1	T0 (P3.4): Timer 0 external input
	15	17	11	1	T1 (P3.5): Timer 1 external input
	16	18	12	0	WR (P3.6): External data memory write strobe
	17	19	13	0	RD (P3.7): External data memory read strobe
RST	9	10	4	I	Reset: A high on this pin for two machine cycles while the oscillator is running, resets the device. An internal resistor to V_{SS} permits a power-on reset using only an external capacitor to V_{CC} .
ALE	30	33	27	0	Address Latch Enable: Output pulse for latching the low byte of the address during an access to external memory. In normal operation, ALE is emitted twice every machine cycle, and can be used for external timing or clocking. Note that one ALE pulse is skipped during each access to external data memory. ALE can be disabled by setting SFR auxiliary.0. With this bit set, ALE will be active only during a MOVX instruction.

P89C51RB2/P89C51RC2/ P89C51RD2

MNEMONIC	Р	PIN NUMBER		TYPE	NAME AND FUNCTION		
MINEMONIC	PDIP	PLCC	LQFP	1175	NAME AND FUNCTION		
PSEN	29	32	26	0	Program Store Enable: The read strobe to external program memory. When executing code from the external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory. PSEN is not activated during fetches from internal program memory.		
ĒĀ/V _{PP}	31	35	29	l	External Access Enable/Programming Supply Voltage: EA must be externally held low to enable the device to fetch code from external program memory locations. If EA is held high, the device executes from internal program memory. The value on the EA pin is latched when RST is released and any subsequent changes have no effect. This pin also receives the programming supply voltage (V _{PP}) during Flash programming.		
XTAL1	19	21	15	ı	Crystal 1: Input to the inverting oscillator amplifier and input to the internal clock generator circuits.		
XTAL2	18	20	14	0	Crystal 2: Output from the inverting oscillator amplifier.		

To avoid a latch-up o effect at power-on, the voltage on any pin (other than V_{PP}) must not be higher than V_{CC} + 0.5 V or less than V_{SS} ± 0.5 V.

9.10.4 IC7307; IC7308: CY2071AS

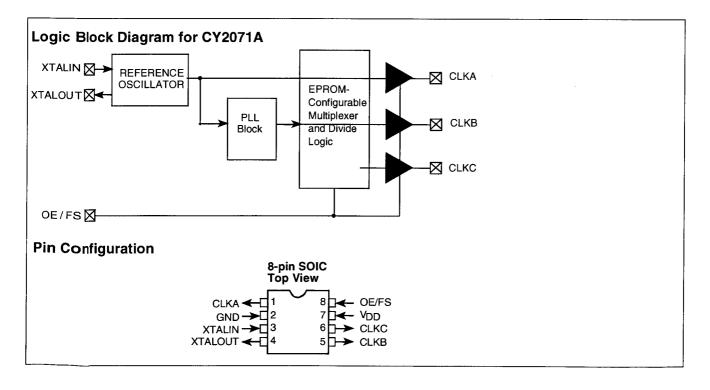
CY2071A

EPROM Programmable Clock Generator

Features	Benefits
Single phase-locked loop architecture	Generates a custom frequency from an external source
EPROM programmability	Easy customization and fast turnaround
Factory-programmable (CY2071A, CY2071AI) or field-programmable (CY2071AF, CY2071AFI) device options	Programming support available for all opportunities
Up to three configurable outputs	Generates three related frequencies from a single device
Low-skew, low-jitter, high-accuracy outputs	Meets critical industry standard timing requirements
Internal loop filter	Alleviates the need for external components
Power management (OE)	Supports low-power applications
Frequency select options	3 outputs with 2 user selectable frequencies
Configurable 5V or 3.3V operation	Supports industry standard design platforms
8-pin 150-mil SOIC package	Industry-standard packaging saves on board space

Selector Guide

Part Number	Outputs	Input Frequency Range	Output Frequency Range	Specifics
CY2071A	3	10 MHz–25 MHz (external crystal) 1 MHz–30 MHz (reference clock)	500 kHz-130 MHz (5V) 500 kHz-100 MHz (3.3V)	Factory Programmable Commercial Temperature
CY2071AI	3	10 MHz-25 MHz (external crystal) 1 MHz-30 MHz (reference clock)	500 kHz-100 MHz (5V) 500 kHz-80 MHz (3.3V)	Factory Programmable Industrial Temperature
CY2071AF	3	10 MHz-25 MHz (external crystal) 1 MHz-30 MHz (reference clock)	500 kHz-100 MHz (5V) 500 kHz-80 MHz (3.3V)	Field Programmable Commercial Temperature
CY2071AFI	3	10 MHz-25 MHz (external crystal) 1 MHz-30 MHz (reference clock)	500 kHz-90 MHz (5V) 500 kHz-66.6 MHz (3.3V)	Field Programmable Industrial Temperature



Pin Summary

Name	Number	Description
CLKA	1	Configurable Clock Output
GND	2	Ground
XTALIN	3	Reference Crystal Input or External Reference Clock Input
XTALOUT	4	Reference Crystal Feedback
CLKB	5	Configurable Clock Output
CLKC	6	Configurable Clock Output
V_{DD}	7	Voltage Supply
OE/FS	8	Output Control Pin, either Output Enable or Frequency Select Input (Active-HIGH, internal pull-up resistor to ${ m V}_{ m DD}$)

Notes:

- 1. For best accuracy, use a parallel-resonant crystal, $C_1 = 17 \text{ pF}$.
- 2. Float XTALOUT pin if XTALIN is driven by reference clock (as opposed to an external crystal).

Functional Description

The CY2071A is a general-purpose clock synthesizer designed for use in applications such as modems, disk drives, CD-ROM drives, video CD players, games, set-top boxes, and data/telecommunications. The device offers up to three configurable clock outputs in an 8-pin, 150-mil SOIC package and can operate off either a 3.3V or 5V power supply. The on-chip reference oscillator is designed for 10-MHz to 25-MHz crystals. Alternatively, an external reference clock of frequency between 1 MHz and 30 MHz can be used.

The CY2071A has one PLL and outputs three factory-EPROM configurable clocks: CLKA, CLKB, and CLKC. The output clocks can originate either from the PLL or the reference, or selected dividers thereof. Additionally, pin 8 can be configured to be an Output Enable or a Select input.

The CY2071A can replace multiple Metal Can Oscillators (MCO) in a synchronous system, providing cost and board space savings to the manufacturer. Hence, these devices are ideally suited for applications that require multiple, accurate, and stable clocks synthesized from low-cost generators in small packages. A hard-disk drive is an example of such an application. In this case, CLKA drives the PLL in the Read Controller, while CLKB and CLKC drive the MCU and associated sequencers.

CyClocks™ Software

CyClocks is an easy-to-use software application that allows you to configure any one of the EPROM-Programmable Clocks offered by Cypress. You may specify the input frequency, PLL and output frequencies, and different functional options. Please note the output frequency ranges in this data sheet when specifying them in CyClocks to ensure that you stay within the limits. You can download a copy of CyClocks free on the Cypress Semiconductor website at www.cypress.com.

Consider using the CY2081 for applications that require unrelated output frequencies. Consider using the CY2291, CY2292, or CY2907 for applications that require more than three output clocks.

Cypress FTG Programmer

The Cypress Frequency Timing Generator (FTG) Programmer is a portable programmer designed to custom program our family of EPROM Field Programmable Clock Devices. The FTG programmers connect to a PC serial port and allow users of CyClocks software to quickly and easily program any of the CY2291F, CY2292F, CY2071AF, and CY2907F devices. The ordering code for the Cypress FTG Programmer is CY3670.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage	0.5V to +7.0V
DC Input Voltage	-0.5V to V _{DD} +0.5V
Storage Temperature	–65°C to +150°C
Max. Soldering Temperature (10 sec)	260°C
Junction Temperature	150°C
Static Discharge Voltage(per MIL-STD-883, Method 3015)	>2000V



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NW701

DV-SD CODEC Data Sheet

Enhanced "Blue Book" Features

- Fully "Blue Book" DV-SD Compliant
- Optional Low Data-Rate Modes: 3.0, 2.4, 1.8, 1.5, and 1.0 Mbytes /sec (for IDE disk drive compatibility)
- Double Clock Option: Capable of operation up to 54 MHz for dual stream applications.

Comprehensive Video and Audio I/O

- NTSC (4:1:1) and PAL (4:2:0) processing
- Integrated multi-tap video filter for 4:2:2 to 4:1:1 or 4:2:2 to 4:2:0 conversions
- Synchronous and "Handshake" Modes
- Glue-less connection to ITU-R-656 (8-bit) video bus
- Popular I2S audio interface
- 48, 44.1 and 32 kHz (12 and 16 bit) audio support

Low Power, Small Footprint

- Low Power Consumption: 0.4W at 27Mhz
- Power Down Mode (60 μW power)
- 3.3V Operating Voltage
- 0.35 Micron, 4 Level Metal Process
- Requires only one 256K x 32 EDO DRAM (Shuffle Memory)
- 160 Pin LQFP (20 x 20 x 1.4 mm) package

High Quality, Low Cost

- ISO9001 Quality Fab
- Extensive design verification

Integrated Solution

- Video I/O and Video Compression
- Audio I/O processing
- Full AUX Code support
- Integrated Shuffle Memory logic
- Glue-less interface to EDO DRAM

Simple Host Bus Connection

- One 16-Bit Asynchronous Host Bus Interface
- Multiplexed Address / Data Bus
- Register and "DV FIFO" access
- 512 Byte DV FIFO for ease of system integration
- Simple Register Programming
- 3 Interrupt pins for system control
- High Speed (33 Mbytes/sec) throughput

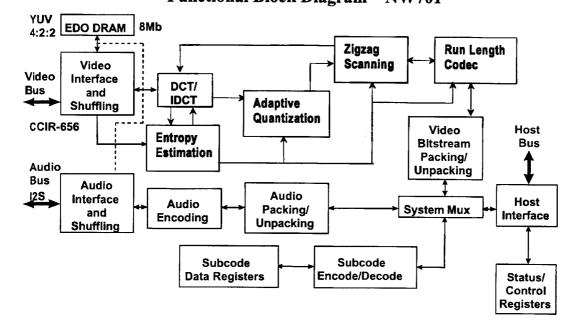
Comprehensive Application Support

- Full Applications Support
- Hardware Reference (demo board)
- Board schematics, layout, and Gerber files
- Telephone and e-mail support
- SDK (Software Developer Kit) for chip and demo board available, both source and object code
- Developer CD includes hardware and software support

Glue-less Connections

- Connects directly to decoders, encoder, audio CODECs
- Direct connection to Philips SAA7146A PCI Bridge

Functional Block Diagram - NW701



Section 1: Overview

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NW701 - DV CODEC: Functional Block Description

Video Interface/Shuffling:

This block provides glue-less connection to industry standard CCIR-656 compatible video bus. Processing of NTSC (4:1:1) and PAL (4:2:0) is perform by this block. Filtering from 4:2:2 down to 4:1:1 or 4:2:0 is perform using multi-tap video filters for maintaining "best" overall picture

To obtain stable quantization for best overall performance, shuffling of Macro blocks are perform using an external memory (256x32 EDO DRAM). Shuffling is required to even out the data in the video image so that there is an even flow for the compression logic to achieve maximum performance.

DCT/IDCT – Discrete Cosine Transform / Inverse Discrete Cosine Transform

This block takes video stream, divided in 8x8 pixel blocks (Macro Block-MB), and performs fast DCT/IDCT operation. The Pixels informations in each block are converted from the "space" domain to "frequency" domain in DCT process in exact reverse in IDCT process.

Encoder Decision Block

To improve coding efficiency, selection is made between 8x8 and/or 2x4x8 DCT modes. Generally, 8x8 mode works best when a video stream contains fields with very small difference. 2x4x8 mode is selected for the opposite condition - namely, for fields containing large difference. 2x4x8 mode includes two 4x8-macro blocks - one MB is the sum of two fields and other is the difference between two fields.

Entropy Estimation

To improve coding efficiency, selection is made between 8x8 and 2x4x8 DCT modes based on the entropy calculation in each block. Class numbers are chosen according the maximum AC coefficients in DCT. These informations are critical to achieve the best quality possible.

Adaptive Quantization

Higher compression is achieved when many DCT AC coefficients are close to Zero. In order to achieve 5:1 compression ration, as specified by the DV standard, the adaptive quantization module will select the best quantization weighting coefficients based on the class number and best-fit bit stream during the selection process.

Zigzag Scanning

This process roughly approximates the selection from "low-frequency" coefficients to "high-frequency" coefficients.

Run Length Codec

The Run Length Coder (RLC) will further compress the bit stream after zigzag scanning by encoding the quantized coefficients and representing consecutive zero coefficients as "another" symbol. The Run Length Decoder (RLD) will restore the zeroes and amplitudes encoded in the bit

Video Packing/Unpacking

This is a final stage for compression, which packs the encoded video data as specified by the DV standard. Or it works as the first stage during the decompression mode to extract video from the DIF stream.

Audio Blocks

This block provides glue-less interface to an industry standard I2S bus for an external Audio CODEC. Furthermore, Audio shuffling and audio bit conversion from 16-bit 12-bit audio are also processed in these blocks.

System MUX

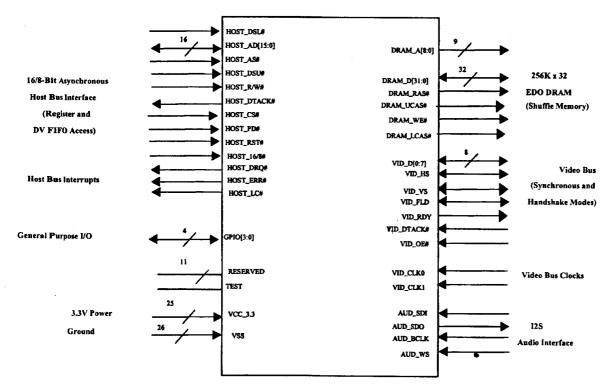
This block provides multiplexing and de-multiplexing of Video, Audio, and subcode DIFs into a legal DV DIF bit streams as specified in "bluebook" - DV standard.

Section 1: Overview

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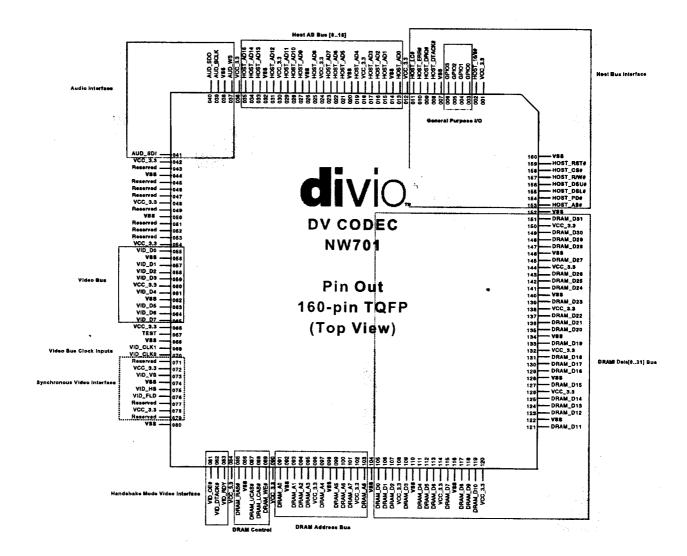
Figure 10: Functional Pin Diagram





Section 1: Overview

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Section 2: Pin Definition

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Pin Numbers in Numerical Sequence

Pin#	Name	Pin#			Name	Pin#	Name
1	VCC_3.3	41	VCC_3.3	81	VID_OE#	121	DRAM_D11
2	HOST_16/8#	42	AUD_SDI	82	VID_DTACK	122	vss ·
3	GPIO0	43	Reserved	83	VID_RDY	123	DRAM_D12
4	GPIO1	44	VSS	84	VCC_3.3	124	DRAM_D13
5	GPIO2	45	Reserved	85	DRAM_RAS#	125	DRAM_D14
6	GPIO3	46	Reserved	86	VSS	126	VCC_3.3
7	VSS	47	Reserved	87	DRAM_UCAS#	127	DRAM_D15
8	HOST_DTACK#	48	VCC_3.3	88	DRAM_LCAS#	128	vss
9	HOST_DRQ#	49	Reserved	89	DRAM_WE#	129	DRAM_D16
10	HOST_ERR#	50	VSS	90	VCC_3.3	130	DRAM_D17
11	HOST_LC#	51	Reserved	91	DRAM_A0	131	DRAM_D18
12	VCC_3.3	52	Reserved	92	VSS	132	VCC_3.3
13	HOST_AD0	53	Reserved	93	DRAM_A1	133	DRAM_D19
14	VSS	54	VCC_3.3	94	DRAM_A2	134	VSS
15	HOST_AD1	55	VID_D0	95	DRAM_A3	135	DRAM_D20
16	HOST_AD2	56	vss	96	VCC_3.3	136	DRAM_D21
17	HOST_AD3	57	VID_DI	97	DRAM_A4	137	DRAM_D22
18	VCC_3.3	58	VID_D2	98	VSS	138	VCC_3.3
19	HOST_AD4	59	VID_D3	99	DRAM_A5	139	DRAM_D23
20	VSS	60	VCC_3.3	100	DRAM_A6	140	VSS
21	HOST_AD5	61	VID_D4	101	DRAM_A7	141	DRAM_D24
22	HOST_AD6	62	VSS	102	VCC_3.3	142	DRAM_D25
23	HOST_AD7	63	VID_D5	103	DRAM_A8	143	DRAM_D26
24	VCC_3.3	64	VID_D6	104	vss	144	VCC_3.3
25	HOST_AD8	65	VID_D7	105	DRAM_D0	145	DRAM_D27
26	VSS	66	VCC_3.3	106	DRAM_D1	146	VSS
. 27	HOST_AD9	67	TEST	107	DRAM_D2	147	DRAM_D28
28	HOST_AD10	68	VSS	108	VCC_3.3	148	DRAM_D29
29	HOST_AD11	69	VID_CLK1	109	DRAM_D3	149	DRAM_D30
30	VCC_3.3	70	VID_CLK0	110	VSS	150	VCC_3.3
31	HOST_AD12	71	Reserved	111	DRAM_D4	151	DRAM_D31
32	VSS	72	VCC_3.3	112	DRAM_D5	152	VSS
33	HOST_AD13	73	VID_VS	113	DRAM_D6	153	HOST_AS#
34	HOST_AD14	74	VSS	114	VCC_3.3	154	HOST_PD#
35	HOST_AD15	75	VID_HS	115	DRAM_D7	155	HOST_DSL#
36	VCC_3.3	76	VID_FLD	116	VSS	156	HOST_DSU#
37	AUD_WS	77	Reserved	117	DRAM_D8	157	HOST_R/W#
38	VSS	78	VCC_3.3	118	DRAM_D9	158	HOST_CS#
39	AUD_BCLK	79	Reserved	119	DRAM_D10	159	HOST_RST#
40	AUD_SDO	80	VSS	120	VCC_3.3	160	VSS

9.10.6 IC7506: UDA1334ATS

Low power audio DAC with PLL

UDA1334ATS

FEATURES

1.1 General

- 2.4 to 3.6 V power supply voltage
- On-board PLL to generate the internal system clock:
 - Operates as an asynchronous DAC, regenerating the internal clock from the WS signal (called audio mode)
 - Generates audio related system clock (output) based on 32, 48 or 96 kHz sampling frequency (called video mode).
- Integrated digital filter plus DAC
- Supports sample frequencies from 16 to 100 kHz in asynchronous DAC mode
- · No analog post filtering required for DAC
- Easy application
- · SSOP16 package.

Multiple format data interface

- I²S-bus and LSB-justified format compatible
- 1fs input data rate.

DAC digital features

- Digital de-emphasis for 44.1 kHz sampling frequency
- · Mute function.

Advanced audio configuration

High linearity, wide dynamic range and low distortion.

PLL system clock generation

- · Integrated low jitter PLL for use in applications in which there is digital audio data present but the system cannot provide an audio related system clock. This mode is called audio mode.
- The PLL can generate 256×48 kHz and 384×48 kHz from a 27 MHz input clock. This mode is called video mode.



BITSTREAM CONVERSION

2 APPLICATIONS

This audio DAC is excellently suitable for digital audio portable application, specially in applications in which an audio related system clock is not present.

3 GENERAL DESCRIPTION

The UDA1334ATS is a single chip 2 channel digital-to-analog converter employing bitstream conversion techniques, including an on-board PLL. The extremely low power consumption and low voltage requirements make the device eminently suitable for use in low-voltage low-power portable digital audio equipment which incorporates a playback function.

The UDA1334ATS supports the I²S-bus data format with word lengths of up to 24 bits and the LSB-justified serial data format with word lengths of 16, 20 and 24 bits.

The UDA1334ATS has basic features such as de-emphasis (44.1 kHz sampling frequency, only supported in audio mode) and mute.

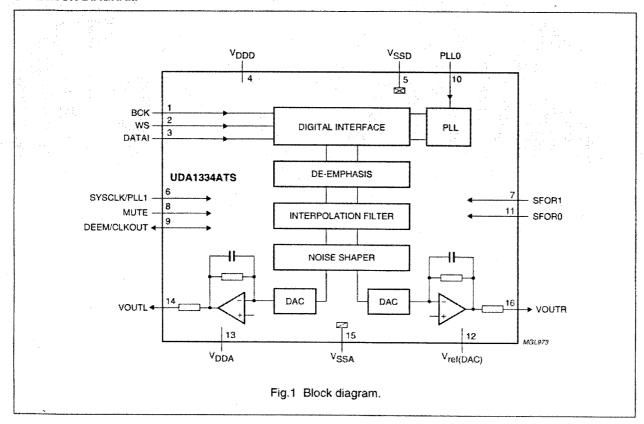
ORDERING INFORMATION

TYPE		PACKAGE					
NUMBER	NAME	DESCRIPTION	VERSION				
UDA1334ATS	SSOP16	plastic shrink small outline package; 16 leads; body width 4.4 mm	SOT:369-1				

Low power audio DAC with PLL

UDA1334ATS

BLOCK DIAGRAM



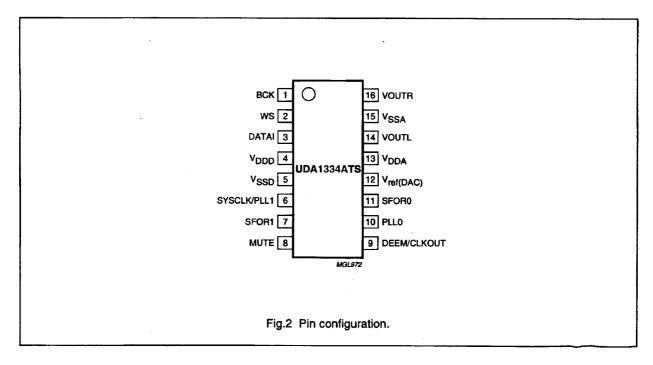
UDA1334ATS

PINNING

SYMBOL	PIN	PAD TYPE	DESCRIPTION
BCK	1	5 V tolerant digital input pad	bit clock input
ws	2	5 V tolerant digital input pad	word select input
DATAI	3	5 V tolerant digital input pad	serial data input
V _{DDD}	4	digital supply pad	digital supply voltage
V _{SSD}	5	digital ground pad	digital ground
SYSCLK/PLL1	6	5 V tolerant digital input pad	system clock input in video mode/PLL mode control 1 input in audio mode
SFOR1	7	5 V tolerant digital input pad	serial format select 1 input
MUTE	8	5 V tolerant digital input pad	mute control input
DEEM/CLKOUT	9	5 V tolerant digital input/output pad	de-emphasis control input in audio mode/clock output in video mode
PLL0	10	3-level input pad; note 1	PLL mode control 0 input
SFOR0	11	digital input pad; note 1	serial format select 0 input
V _{ref(DAC)}	12	analog pad	DAC reference voltage
V _{DDA}	13	analog supply pad	DAC analog supply voltage
VOUTL	14	analog output pad	DAC output left
V _{SSA}	15	analog ground pad	DAC analog ground
VOUTR	16	analog output pad	DAC output right

Note

1. Because of test issues these pads are not 5 V tolerant and both pads should be at power supply voltage level or at a maximum of 0.5 V above that level.



UDA1334ATS

FUNCTIONAL DESCRIPTION

8.1 System clock

The UDA1334ATS incorporates a PLL capable of generating the system clock. The UDA1334ATS can operate in 2 modes:

- It operates as an asynchronous DAC, which means the device regenerates the internal clocks using a PLL from the incoming WS signal. This mode is called audio mode.
- It generates the internal clocks from a 27 MHz clock input, based on 32, 48 and 96 kHz sampling frequencies. This mode is called video mode.

In video mode, the digital audio input is slave, which means that the system must generate the BCK and WS signals from the output clock available at pin CLKOUT of the UDA1334ATS. The digital audio signals should be frequency locked to the CLKOUT signal.

Remarks:

- 1. The WS edge MUST fall on the negative edge of the BCK at all times for proper operation of the digital I/O data interface
- 2. For LSB-justified formats it is important to have a WS signal with a duty factor of 50%.

8.1.1 **AUDIO MODE**

Audio mode is enabled by setting pin PLL0 to LOW. De-emphasis can be activated via pin DEEM/CLKOUT according to Table 5.

In audio mode, pin SYSCLK/PLL1 is used to set the sampling frequency range as given in Table 1.

Table 1 Sampling frequency range in audio mode

SYSCLK/PLL1	SELECTION	
LOW	f _s = 16 to 50 kHz	_
HIGH	f _s = 50 to 100 kHz	_

8.1.2 VIDEO MODE

In video mode, the master clock is a 27 MHz external clock (as is available in video environment). A clock-out signal is generated at pin DEEM/CLKOUT. The output frequency can be selected using pin PLLO. The output frequency is either 12.228 MHz (256 × 48 kHz) with pin PLL0 being at MID level or 18.432 MHz (384 × 48 kHz) with pin PLL0 being HIGH, as given in Table 2.

Table 2 Clock output selection in video mode

PLL0	SELECTION
MID	12.228 MHz clock; note 1
HIGH	18.432 MHz clock; note 2
LOW	audio mode

Notes

- 1. The supported sampling frequencies are: 96, 48 and 24 kHz or 64, 32 and 16 kHz.
- 2. The supported sampling frequencies are: 96, 48 and 24 kHz; 72 and 36 kHz or 32 kHz.

8.2 Interpolation filter

The interpolation digital filter interpolates from 1fs to 64fs by cascading FIR filters (see Table 3).

Table 3 Interpolation filter characteristics

ITEM	CONDITION	VALUE (dB)
Pass-band ripple	Of _s to 0.45f _s	±0.02
Stop band	>0.55f _s	-50
Dynamic range	Of _s to 0.45f _s	>114

Noise shaper

The 5th-order noise shaper operates at 64f_s. It shifts in-band quantization noise to frequencies well above the audio band. This noise shaping technique enables high signal-to-noise ratios to be achieved. The noise shaper output is converted into an analog signal using a Filter Stream DAC (FSDAC).

UDA1334ATS

Filter stream DAC 8.4

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. No post filter is needed due to the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

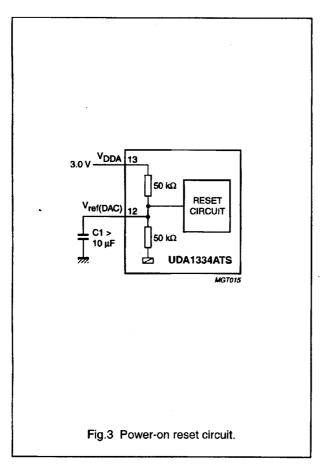
The output voltage of the FSDAC scales proportionally to the power supply voltage.

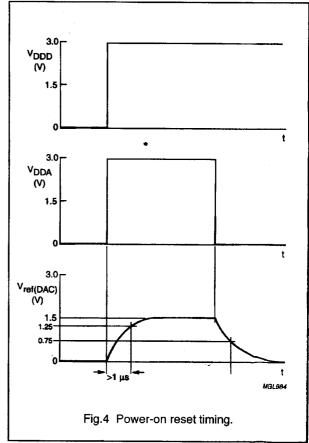
8.5 Power-on reset

The UDA1334ATS has an internal Power-on reset circuit (see Fig.3) which resets the test control block.

The reset time (see Fig.4) is determined by an external capacitor which is connected between pin $V_{ref(DAC)}$ and ground. The reset time should be at least 1 µs for $V_{ref(DAC)}$ < 1.25 V. When V_{DDA} is switched off, the device will be reset again for $V_{ref(DAC)} < 0.75 \text{ V}$.

During the reset time the system clock should be running.





UDA1334ATS

8.6 Feature settings

8.6.1 DIGITAL INTERFACE FORMAT SELECT

The digital audio interface formats (see Fig.5) can be selected via pins SFOR1 and SFOR0 as shown in Table 4.

For the digital audio interface holds that the BCK frequency can be maximum 64 times WS frequency.

The WS signal must change at the negative edge of the BCK signal for all digital audio formats.

Table 4 Data format selection

SFOR1	SFOR0	INPUT FORMAT
LOW	LOW	12S-bus input
LOW	HIGH	LSB-justified 16 bits input
HIGH	LOW	LSB-justified 20 bits input
HIGH	HIGH	LSB-justified 24 bits input

8.6.2 **DE-EMPHASIS CONTROL**

This function is only available in audio mode. In that case, pin DEEM/CLKOUT can be used to activate the digital de-emphasis for 44.1 kHz as given in Table 5.

Table 5 De-emphasis control (audio mode)

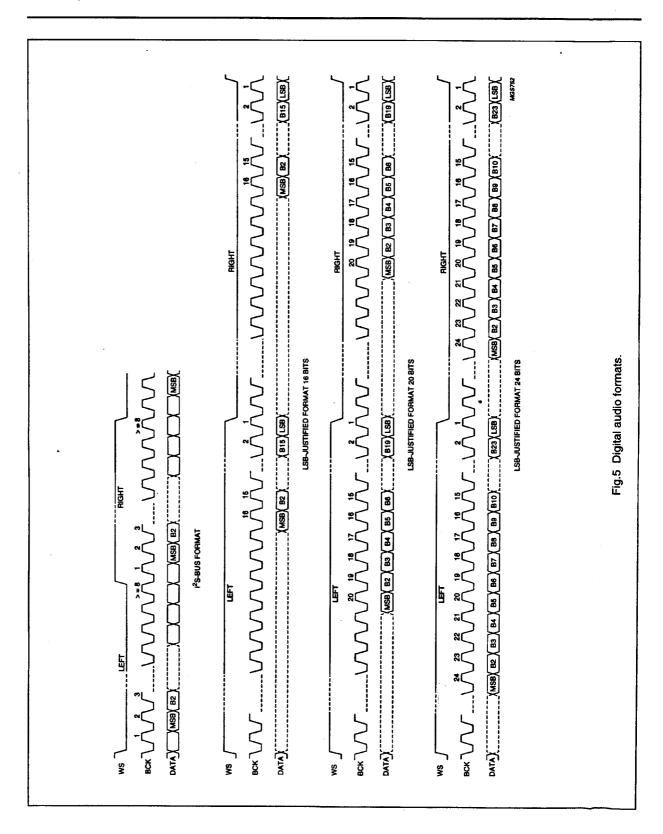
DEEM/CLKOUT	FUNCTION
LOW	de-emphasis off
HIGH	de-emphasis on

8.6.3 MUTE CONTROL

The output signal can be soft muted by setting pin MUTE to HIGH as given in Table 6.

Table 6 Mute control

MUTE	FUNCTION
LOW	mute off
HIGH	mute on



9.11.1 FLI2200

FLI2200

Description

The FLI2200 is a single chip implementation of Faroudja Laboratories' award winning deinterlacing and postprocessing algorithms that produce the highest quality progressive video output from a variety of interlaced video inputs including 525/60 (NTSC) or 625/50 (PAL or SECAM). It uses patented and patent pending motion-adaptive deinterlacing that selects the optimal filtering on a per-pixel basis. This includes detection and proper interleaving of 3:2 and 2:2 pulldown for film-base sources, including continuous monitoring and compensation for bad edits that occur frequently in broadcast material due to poor scene cuts or insertion of commercials. Video material is processed by a set of content-sensitive spatio-temporal filters that adapt to the appropriate direction for smoothest interpolation using the patented Faroudja DCDi™ algorithm. The FLI2200 also includes motion-adaptive cross-color suppression that removes highly objectionable coloration artifacts produced by commonly used video decoders. Its internal processing uses 10 bits per channel to maintain the highest quality. Its inputs and outputs are 10 bits/channel for best quality but also supports 8 bits/channel for more cost-sensitive applications. The FLI2200 requires 4 MB of low cost SDRAM for best quality deinterlacing, but it can also be operated in an optimized intra-field mode without memory for more costsensitive applications. This makes possible the use of a single design for both high-end and low-end applications.

The FLI2200 integrates a number of functions to provide maximum flexibility in a low cost configuration. This includes an on-chip clock generator, SDRAM controller, display controller, input and output color-space converters. It uses a standard 2-wire serial control interface for easy control and access to the registers.

The FLI2200 can be connected without glue logic to the FLI2000 video decoder and FLI2220 Enhancer and OSD Generator to produce the highest quality video pipeline for premium applications. It is also fully compatible with other decoders having a ITU-R BT 656 output format.

Applications

Flat panel TV-LCD, PDP Progressive scan TVs Multimedia front/rear projectors Home Theater Scan Converters Multimedia PCs/Workstations

DCDi™ is a Faroudja trademark

Features

Motion-adaptive cross-color suppression removes artifacts produced by improper Y/C separation in lowcost video decoders

Motion-adaptive video deinterlacing selects optimal filtering on a per-pixel basis

Film-mode for proper handling of 3:2 and 2:2 pulldown material

Bad-edit detection/correction compensates for poor scene cuts and insertions common in broadcast material

Motion-weighted interpolation for video sources produces maximum resolution without introducing motion artifacts

Directional Correlational Deinterlacing (DCDiTM) minimizes jaggies on angled lines

8/10-bit Y/Cb/Cr (D1) (TTU-R BT 656), 16/20-bit Y Cb/Cr (ITU-R BT 601), 24/30-bit RGB or YCbCr/YPbPr interlaced input options

- Supports 525/60 (NTSC), 625/50 (PAL/SECAM)
- ? Accepts up to 1100 pixels/line

8/10-bit, 16/20-bit YUV, 24/30-bit RGB or YCbCr/YPbPr progressive output options

Supports 8- or 10-bit inputs and outputs 10-bit internal processing for highest quality Includes color-space converters at input and output for maximum flexibility

Auto-detection of NTSC/PAL/SECAM inputs

High-order filtering produces smooth chroma output in 4:2:2 to 4:4:4 or 4:4:4 to 4:2:2 conversions

Resolution recovery maximizes output signal-to-noise ratio and dynamic range

Can be operated without glue logic with FLI2000 Video Decoder and FLI2220 Enhancer and OSD Generator ICs to produce highest quality video pipeline

Glue-less interface to most standard video decoders

Built-in display timing generator

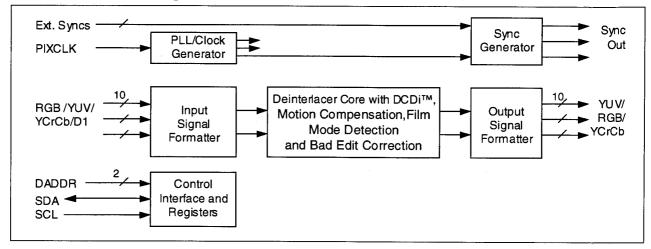
On-chip clock generator eliminates external PLLs

On-chip SDRAM controller

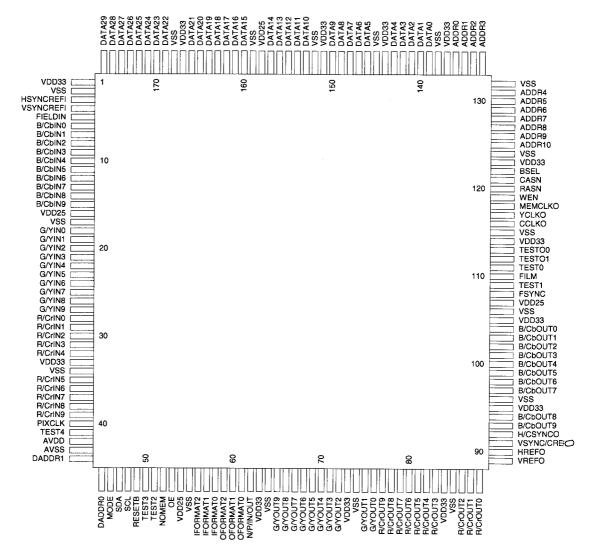
Uses low cost SDRAM as field memory – 4 MB Optimized intra-field operation allows memory-less configuration for lowest cost applications with same design and layout as for high-end applications 2-wire serial control interface for easy control

176-pin TQFP package

Simplified Block Diagram



Pin description



Pin Connections and Functions

Pin#	Name	Description
See list	V _{SS}	Ground connections. Connect to the digital ground plane. Pins: 2, 17, 34, 55, 64, 74, 85, 96, 106, 115, 124, 132, 138, 145, 152, 159, 168
See list	V _{DD33}	Pad Ring digital power connections. Connect to the digital 3.3 volt power supply and decouple to the digital ground plane. Pins: 1, 33, 63, 73, 84, 95, 105, 114, 123, 137, 144, 151, 167
See list	V _{DD25}	Core Logic digital power connections. Connect to the digital 2.5 volt power supply and decouple to the digital ground plane. Pins: 16, 54, 107, 158
43	AV _{SS}	Ground connection for the clock PLL circuits. Connect to the digital ground plane
42	AV _{DD}	Analog power connections for the clock PLL circuit. Connect to a separately decoupled 2.5 volt power supply and decouple directly to the AV_{SS} pin
49	RESETB	Reset. When this input is set low it will reset all the internal registers to the default states. Refer to the section on the control registers for details of these states. The device must be reset after it is powered-up.
53	OE	When this pin is set high the outputs of the FLI2200 will be enabled; when it is set low the outputs will be set into a high-impedance state.
56-58	IFORMAT ₂₋₀	Input signal format control. The settings of these pins set the format of the input signal. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00_H for details.
59-61	OFORMAT ₂₋₀	Output signal format control. The settings of these pins set the format of the output signal. This can be overridden by the OFmtOvr bit, bit 3 in register $07_{\rm H}$, allowing this function to be set or changed via the I^2C bus. Please refer to the description of register $07_{\rm H}$ for details.
44-45	DADDR ₁₋₀	The settings of $DADDR_{1-0}$ allow the device address of the control bus to be programmed to prevent conflict with the other devices connected to the bus. $DADDR_{1-0}$ allow the device address to be set to any of the following values: $C0/C1_H$, $C2/C3_H$, $E0/E1_H$, $E2/E3_H$. Please refer to the section "Control Bus Operation and Protocol" for further information.
46	MODE	When this pin is set low the control bus will operate in the slave mode; allowing the device to programmed from an external controller. When it is set high the FLI2200 will self-program from an external I ² C memory connected to the bus. Please refer to the "Control Bus Operation and Control Protocol" section for more details.
47	SDA	2-wire serial control bus data. Data can be written to the control registers via this pin when it is in the input mode and data can be read from the status registers when it is in the output mode. Refer to the section on the serial port for timing and format details and to the section on the registers for programming information.
48	SCL	2-wire serial control bus clock. When the control port operates in slave mode this pin will be an input and when it operates in the self programming mode it will be an output.
40	PIXCLK	Pixel clock input. This clock is used to drive all the circuits in the FLI2200. An internal PLL is used to upconvert this clock to provide the master clock signal and other clocks used internally. Note that when the FLI2200 is used in the D1 input mode the PIXCLK input should run at the rate of two cycles per pixel (one for luma and one for chroma).
62	N/P/IN/OUT	NTSC/PAL input or output. The default function of this pin is NTSC/PAL signal indicator output. When the input video signal is a 525 line signal this pin will be set high and when it is a 625 line signal the pin is set low. This function of this pin can be programmed to be an input according to the setting of this pin if the NPOp ₁₋₀ bits, bits 5-4 in register $03_{\rm H}$, are set to $00_{\rm H}$, overriding the internal line counter. i.e., it will treat the signal as a 525 line signal when it is set high and a 625 line signal when it is set low.

Pin #	Name	Description
52	NOMEM	No Memory Mode control input. This pin controls the operation of the FLI2200 as follows: When this pin is set low the device is used with external field memories and operates in the full set of deinterlacing modes, i.e., motion adaptive video deinterlacing and full frame film source deinterlacing using 3:2 pulldown detection (2:2 pulldown for 625/50 sources). When this pin is set high the FLI2200 is forced into the intra-field only deinterlacing mode, which requires no external memories, allowing the FLI2200 to be used in low-cost applications where the ultimate video quality is not a requirement. <i>To ensure proper startup of the SDRAMs this pin should be set high during the power-up sequence</i> . This can be overridden by the NMOvr bit, bit 1 in register $05_{\rm H}$, allowing this function to be set or changed via the I ² C bus. Please refer to the description of register $05_{\rm H}$ for details.
27-18	G/YIN ₉₋₀	10-bit green or luminance signal input bus. The mode is set by the IFORMAT ₂₋₀ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00_H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00_H for details. This signal is sampled on the rising edge of PIXCLK.
15-6	B/CbIN ₉₋₀	10-bit blue or Cb chroma signal input bus. The mode is set by the IFORMAT ₂₋₀ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details. Bits 6, 4 and 3 in register 08 _H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr and Y Pb Pr modes the Cb or Pb signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
39-35 32-28	R/CrIN ₉₋₀	10-bit red or Cr chroma signal input bus. The mode is set by the IFORMAT ₂₋₀ pins. This can be overridden by the IFmtOvr bit, bit 3 in register 00 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 00 _H for details. Bits 6, 4 and 3 in register 08 _H specify the busses used in the multiplexed modes. In all cases the signals are sampled on the rising edges of PIXCLK. In the Y Cb Cr mode the Cr signal is sampled on alternate rising edges of PIXCLK in 4:2:2 mode. The frequency of PIXCLK will be 27 MHz in the multiplexed Y/Cb/Cr mode and 13.5 MHz in all other modes. These pins should be tied low when not used.
3	HSYNCREFI	Horizontal sync or reference. The horizontal sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00_H . The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tiedlow; in this case all sync information will be derived from the signal.
4	VSYNCREFI	Vertical sync or reference. The vertical sync or reference of the input signal should be connected to this pin. The function is programmed with bit 4 in register 00_H . The polarity and position of the sync or reference pulse relative to the start of active video are both programmable within a small range. When the FLI2200 is used in the ITU-R BT 601/D1 input mode with embedded syncs (IFormat = 110) this input is not used and should be tied low; in this case all sync information will be derived from the signal.
5	FLDIN	Field identifier input. The field identifier output of the source signal should be connected to this pin. A low setting signifies an even field and a high level signifies an odd field. When bit 4 in register 00_H is set low, the input timing is based on HREF and VREF and this signal is required. When this bit is set high the input timing is based on HSYNC and VSYNC and this signal is generated internally and is not required. When bit 5 in register 06 is set high this signal is also used as the frame boundary identifier for 30 Hz film sources.

Pin#	Name	Description
65-72 75-76	G/YOUT ₉₋₀	Green or luminance output bus. In the RGB mode this output is the Green signal and in the YCbCr mode it is the Y signal. The mode is set by the OFORMAT ₂₋₀ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details. The signal is clocked out on the falling edge of YCLKO.
93-94 97-104	B/CbOUT ₉₋₀	Blue or Cb chrominance output bus. In the RGB mode this output is the Blue signal, in the Y Cb Cr mode it is the Cb signal. The mode is set by the OFORMAT ₂₋₀ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08 _H . The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
77-83 86-88	R/CrOUT ₉₋₀	Red or Cr chrominance output bus. In the RGB mode this output is the Red signal, in the YCbCr mode it is the Cr signal. The mode is set by the OFORMAT ₂₋₀ pins. This can be overridden by the OFmtOvr bit, bit 3 in register 07 _H , allowing this function to be set or changed via the I ² C bus. Please refer to the description of register 07 _H for details. The busses used in the multiplexed modes are set by means of bit 5 in register 08 _H . The signal is clocked out on the falling edge of YCLKO in the RGB and YUV 4:4:4 modes, on the falling edge of YCLKO prior to the next rising edge of CCLKO in the YUV 4:2:2 mode, and on the rising edge of MEMCLKO in the multiplexed YCbCr (pseudo D1) mode.
116	CCLKO	Chroma output sampling clock. This clock is derived from PIXCLK and will be at half the frequency of YCLKO. In 30-bit 4:2:2 output mode the chroma output signals will change on the falling edge of YCLKO prior to the next rising edge this clock.
117	YCLKO	Luma output sampling clock. This clock is derived from PIXCLK and is double the frequency of PIXCLK. In 30-bit and 20-bit output modes the output signals will change on the falling edge of this clock.
89	VREFO	Start of active field or frame indicator. This signal goes high to indicate the first active line in each field or frame and goes low during the vertical blanking interval. The polarity and timing of this signal are programmable.
90	HREFO	Start of active line indicator output. This signal goes high to indicate the first active pixel in each line and goes low during the horizontal blanking interval. The polarity and timing of this signal are programmable.
91	VSYNC/ CREFO	Vertical sync output. This signal provides the vertical sync function for the outputs. Its polarity is programmable to be active high or active low. It can also be programmed to be a composite reference for applications requiring this instead of sync.
92	H/CSYNCO	Horizontal or composite sync output. This signal provides the horizontal sync function for the outputs. Its polarity is programmable to be active high or active low. This signal can also be programmed to be the composite sync output, CSYNC.
108	FSYNC	Film mode sync output. When film mode is detected this pin will toggle in sync with the 3:2 (NTSC) or 2:2 (PAL and 30 Hz film in NTSC) pulldown sequence detected in the source.
110	FILM	Film mode detector output. This pin will be set high when the FLI2200 detects that the video input was converted from 24 fps film with a teleciné machine. If film mode is not detected this pin will be set low.

Pin#	Name	Description
125-131 133-136	ADDR ₁₀₋₀	SDRAM Address bus. This signal bus is used to address the external SDRAM(s) used for field memories. It should be connected to the A_{10-0} bus of the memory chip(s). Please refer to the Applications section of this data sheet for further details.
176-169 166-160 157-153 150-146 143-139	DATA ₂₉₋₀	SDRAM Data bus. This signal bus is used to transfer the data to and from the external SDRAM(s) used for field memories. It should be connected to the DQ ₂₉₋₀ bus of the memory chip when using a 64 Mbit SDRAM. When using two 16 Mbit SDRAMs this 30-bit bus may be connected to the two 16-bit data busses of the memories in two ways: either connect 16 lines to one chip and 14 to the other, or connect 15 to both. In all cases the two unused data lines on the memory chip(s) should be connected to ground via 22 k? resistors. Please refer to the Applications section of this data sheet for further details.
118	MEMCLKO	SDRAM clock and 2x output sampling clock. This clock is derived from PIXCLK and will be at double the frequency of YCLKO. This active signal should be connected to the CLK pin(s) on the SDRAM(s). When the 10-bit output mode selected the output signals will also change at this clock rate and this should then be used as the output clock
119	WEN	SDRAM Write Enable. This active low signal should be connected to the WE pin(s) on the SDRAM(s).
120	RASN	SDRAM Row Address Select. This active low signal should be connected to the RAS pin(s) on the SDRAM(s).
121	CASN	SDRAM Column Address Select. This active low signal should be connected to the CAS pin(s) on the SDRAM(s).
122	BSEL	SDRAM Bank Select. When using two 16 Mbit SDRAMs this signal should be connected to the BA (also called BS or A ₁₁) pin on both SDRAMs. When using a 64 Mbit SDRAM this signal should be connected to the BA0 (also called BS0 or A ₁₁) pin on the SDRAM and BA1/BS1 (also called BA when BA0 is referred to as A ₁₁) should be tied low.
41, 50, 51, 109, 111	TEST ₄₋₀	These pins are used for test purposes only and should always be tied low for normal operation.
112, 113	TESTO ₁₋₀	These pins are test outputs and should be left unconnected in normal operation.

9.11.2 ADV7196

ADV7196A

INPUT FORMATS

YCrCb in 2x10-Bit (4:2:2) or 3x10-Bit (4:4:4) format compliant to SMPTE-293M (525p), ITU-R.BT1358 (625p), SMPTE274M (1080i), SMPTE296M (720p) and any other High Definition standard using Async Timing Mode RGB in 3x10 Bit 4:4:4 format

OUTPUT FORMATS

YPrPb Progressive Scan (EIA-770.1, EIA-770.2) YPrPb HDTV (EIA 770.3) RGB levels compliant to RS-170 and RS-343A 11-Bit + Sync (DAC A) 11-Bit DACs (DAC B, DAC C)

PROGRAMMABLE FEATURES

Internal Testpattern Generator with Color Control Y/C delay (+/-) Gamma Correction Individual DAC on/off control 54MHz Output (2xOversampling) Sharpness filter with programmable gain/attenuation

GENERAL DESCRIPTION

The ADV7196A is a triple high speed, digital-to-analog encoder on a single monolithic chip. It includes of three high speed video D/A converters with TTL compatible inputs.

The ADV7196A has three separate 10-Bit wide input ports which accept data in 4:4:4 10-Bit YCrCb or RGB or 4:2:2 10-Bit YCrCb. This data is accepted in progressive scan format at 27MHz or HDTV format at 74.25MHZ or 74.1758M Hz. For any other High Definition standard but SMPTE 293M, ITU-R BT.1358, SMPTE274M or SMPTE296M the Async Timing Mode can be used to input data to the ADV7196A. For all standards, external horizontal, vertical and blanking signals or EAV/SAV codes control the insertion of appropriate synchronisation signals into the digital data stream and therefore the output signals.

The ADV7196A outputs analog YPrPb progressive scan format complying to EIA770.1, EIA 770.2 or YPrPb HDTV complying to EIA 770.3 or RGB complying to RS-170/RS 343A.

The ADV7196A requires a single 3.3V power supply, an optional external 1.235 V reference and a 27 MHz clock in Progressive Scan Mode or a 74.25MHz (or 74.1758M Hz) clock in HDTV mode.

Programmable Adaptive Filter Control Undershoot Limiter **VBI Open Control** 12C Filter

Macrovision Rev 1.0 (525p) CGMS-A (525p) 2 Wire Serial MPU Interface

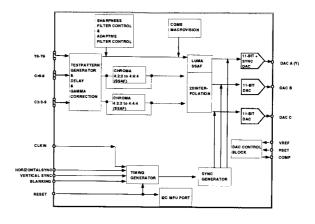
Single Supply +3.3 V Operation 52-MQFP package

APPLICATIONS Progressive Scan / HDTV Display Devices **DVD Players** Progressive Scan/HDTV Projection Systems MPEG2@81MHz Digital Video Systems High Resolution Color Graphics Image Processing/ Instrumentation Digital Radio Modulation/ Video Signal Reconstruction

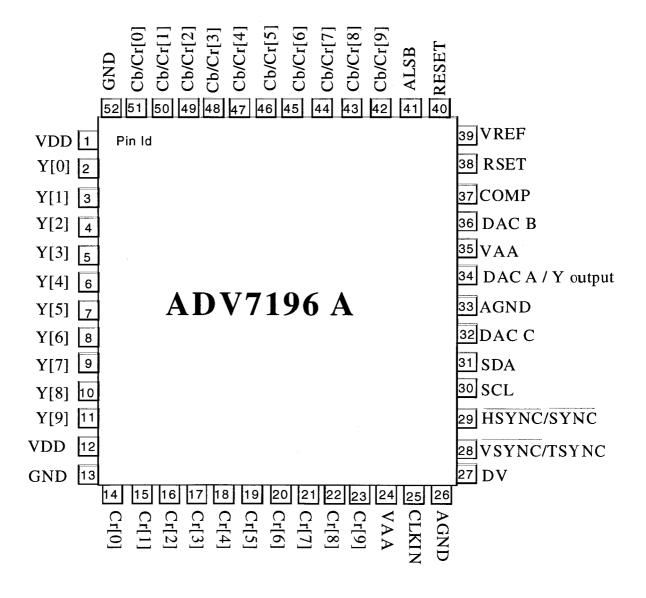
In Progressive Scan Mode, a Sharpness Filter with programmable gain allows high frequency enhancement on the luminance signal. Programmable Adaptive Filter Control which may be used, allows removal of ringing on the incoming Y data. The ADV7196A supports CGMS-A data control generation and the Macrovision Anticopy algorithm in 525p mode.

The ADV7196A is packaged in a 52-Pin MQFP package.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



Pin MnemonicInput/Output		Function	
GND	G	Digital Ground	
AGND	G	Analog Ground	
ALSB	1	TTL Address Input. This signal sets up the LSB of the MPU address. When this pin is tied high the I2C filter is activated which reduces noise on the I2C interface. When this pin is tied low, the input bandwidth on the I2C lines is increased.	
DV	I	Video Blanking Control Signal Input.	
CLKIN	1	Pixel Clock Input. Requires a 27MHz reference clock for standard operation in Progressive Scan Mode or a 74.25MHz (74.1758MHz) reference clock in HDTV mode.	
COMP	0	Compensation Pin for DACs. Connect $0.1\mu F$ Capacitor from COMP pin to V_{AA} .	
DAC A	0	Y analog output.	
DAC B	0	Color component analog output of input data on Cr 9-0 input pins.	
DAC C	0	Color component analog output of input data on Cb/Cr 9-0 input pins.	
HSYNC/ SYNC	ı	HSYNC, horizontal sync control signal input or SYNC input control signal in Async Timing Mode.	
Cr 9-0	I	10-Bit Progressive scan/ HDTV input port for color data in 4:4:4 input mode. In 4:2:2 mode this input port is not used. Input port for R data when RGB data is input.	
Cb/Cr 9-0	I	10-Bit Progressive scan/ HDTV input port for color data. In 4:2:2 mode the multiplexed CrCb data must be input on these pins. Input port for B data when RGB is input.	
RESET	1	This input resets the on-chip timing generator and sets the ADV7196A into Default Register setting. Reset is an active low signal.	
R _{SET}	ı	A 2470 Ohms resistor (for input ranges 64-940 and 64-960, output standards EIA770.1-3) must be connected from this pin to AGND and is used to control the amplitudes of the DAC outputs. For input ranges 0 -1023 (RS-170,RS-343A) the R_{SET} value must be 2820 Ohms.	
SCL	1	MPU Port Serial Interface Clock Input	
SD A	1/0	MPU Port Serial Data Input/Output	
<u>VSYNC/</u> TSYNC	I	<u>VSYNC</u> , vertical sync control signal input or TSYNC input control signal in AsyncTiming Mode.	
V _{DD}	Р	Digital power supply	
VAA	Р	Analog power supply	
V _{REF}	1/0	Optional External Voltage Reference Input for DACs or Voltage Reference Output (1.235V).	
Y9 -Y0	ı	10-Bit Progressive scan/ HDTV input port for Y data. Input for G data when	

		,		
9.12	List of Abbrevia	tions	CPU_RESET	Control processor unit reset
			CPUINT(0-1)	Control processor unit interrupt
9.12.1	Digital Board		CTS1P CVBS_OUT	Clear to send (Service Interface) Composite video output out of the
	+12V	+12V Power Supply	CVPC OUT P	Host Decoder
	+3V3	+3V3 Power Supply	CVBS_OUT_B CVBS_OUT_B_711	Filtered Composite video output
	+5V	+5V Power Supply	8	Composite video output to Video
	+5V_BUFFER	+5V Power Supply for Video Filters	<u>-</u>	Input Processor(digital board video
	24M576_OUT	24M576 X-tal frequency output from		loop)
	27M_CLK_PS	Video Input Processor 27MHz clock to Progressive Scan	CVBS_Y_IN	Composite video/Luminance input
	5505_HS	Horizontal Synchronisation from	CVBS_Y_IN_7118_	
		Host Decoder to Progressive Scan	A	Composite video/Luminance input to Video Input Processor
	5505_ODD_EVEN	Odd - Even control from Host	CVBS_Y_IN_7118_	to video input Processor
		Decoder to Progressive Scan	В	Composite video/Luminance input
	5505_VS_PS	Vertical Synchronisation from Host		to Video Input Processor
	-5V	Decoder to Progressive Scan -5V Power Supply	CVBS_Y_IN_7118_	
	ACC_ACLK_OSC	Audio Clock PLL output sync with	С	Composite video/Luminance input
		incoming video for record	D BAB D(7:0)	to Video Input Processor
	ACC_ACLK_PLL	Audio Clock PLL output for play	D_PAR_D(7:0)	Front-end parallel interface data (record)
		back	D_PAR_DVALID	Front-end parallel interface data
	AD_ACLK	Audio Decoder Clock		valid
	AD_BCLK AD_DATA(0:2)	Audio Decoder I2S bit clock Audio Decoder data (PCM)	D_PAR_REQ	Front-end parallel interface request
	AD_SPDIF	Audio Decoder data (1 CM) Audio digital output to the analog	D_PAR_STR	Front-end parallel interface strobe
	7.15_01 5.11	board	D_PAR_SYNC	Front-end parallel interface sync
	AD_WCLK	Audio Decoder I2S word clock	D_V4	Digital versatile input pin Front-end I2S versatile signal
	ADC_ENABLEN	Analog Digital converter enable	D_WCLK	Front-end I2S word clock
	AE_BCLK	Audio Encoder I2S bit clock	DSP_A(0-9)	Digital sound processor address bus
	AE_CSN	Audio Encoder chip select(LOW	DSP_CE	Digital sound processor chip enable
	AE_DATAI	active) Audio Encoder I2S data input from	DSP_D(0-23)	Digital Sound Processor data bus
	/\L_D/\\/\	analog board	DSP_MA16	Digital Sound Processor Memory
	AE_DATAO	Compressed I2S audio data from	DSP_RDN	Address 16 line Digital Sound Processor read
		DSP to Host Decoder	DSI _IIDIN	enable(LOW active)
	AE_IRQN	Audio Encoder interrupt request	DSP_WRN	Digital Sound Processor write
	AE_WCLK	Audio Encoder I2S word clock		enable(LOW active)
	ANA_WE B_IN_7118	Analog write enable Video blue input to Video Input	DV_IN_CLK	Digital Video in clock from DVIO
	D_III_7 1 10	Processor	DV (AL DATA(7.0)	board
	B_OUT	Video blue output from Host	DV_IN_DATA(7:0) DV_IN_H\$	Digital Video in data bus from DVIO Digital Video in horizontal
		Decoder	DV_IIV_I13	synchronisation from DVIO
	B_OUT_B	Filtered blue video output	DV_IN_VS	Digital Video in vertical
	BCLK_CTRL BE_BCLK	Basic Engine I2S Bit clock control Basic Engine I2S bit clock		synchronisation from DVIO
	BE_BCLK_VSM	Basic Engine I2S bit clock to VSM	EMI_A(1-21)	External Memory in terface Address
	BE_CPR	Basic Engine Control Processor	EM DEAM	Bus(Host Decode)
	_	ready to accept data	EMI_BE1N	External Memory Interface Upper byte enable(Host Decoder)
	BE_DATA_RD	Basic Engine Data read	EMI_BEON	External Memory hterface Lower
	BE_DATA_WR	Basic Engine Data write		byte enable(Host Decoder)
	BE_FAN BE_FLAG	Basic Engine FAN Basic Engine error flag	EMI_CASN	External Memory h terface SDRAM
	BE_IRQ	Basic Engine entri hag Basic Engine interrupt request		column address stobe(Host
	BE_LOADN	Basic Engine LOAD(LOW active)	EMI OF IN	Decoder)
	BE_RXD	Basic Engine S2B received data	EMI_CE1N	External Memory Interface VSM
	BE_SUR	Basic Engine servo unit ready to	EMI_CE2N	Lower bank enable External Memory hterface VSM
		accept data (S2B)	2111_02211	Higher bank enable
	BE_SYNC	Basic Engine sector/abs time sync	EMI_CE3N	External Memory lit erface flash IC's
	BE_TXD BE_V4	Basic Engine S2B transmitted data Basic Engine versatile input pin		enable
	BE_WCLK	Basic Engine 12S word clock	EMI_D(0-15)	External Memory hterface Data
	C_IN	Video Chrominance input	EMI OEN	Bus(Host Decoder
	C_IN_7118	Chrominance input to Video Input	EMI_OEN	External Memory hterface Output enable(Host Decoler)
		Processor	EMI_PROCCLK	External Memory hterface
	C_OUT	Chrominance output from Host	_	Processor Clock(Ho st Decoder)
	C_OUT_B	Decoder Filtered Chrominance output	EMI_RASN	External Memory Interface SDRAM
	C_OUT_B CENTRE_ON_STE	i mered Omorninance output		row address strob(Host Decoder)
	REO	Control signal from Host Decoder to	EMI_RWN	External Memory Interface Read/
		AV board to switch Stereo Output	EMI_WAIT	Write control signa(Host Decoder) External Memory Int erface Wait
		cinch to mono.	-14U-14-VI	state request(HostDecoder)
	COAX_IN	Coaxial input	ERROROUT	Control port P3 I/Of rom Host
	CPU_ANALYSE	Control processor unit analyse		Decoder

FB	Fast Blanking	RTS1P	Ready To Send data to service
FLASH_OEN	FLASH output enable control signal		serial interface
G_IN_7118	Video green input to Video Input	RX1P	Receive data from service serial
COUT	Processor	201	interface
G_OUT	Video green output from Host	SCL	I2C bus clock
G_OUT_B	Decoder Filtered green video output from	SDA	I2C bus data
G_001_B	Host Decoder	SEL_ACLK(1-2) SERVICES	Select audio clock(playback)
HD_M_AD(11:0)	Host Decoder SDRAM address bus	SERVICES	Control signal of service serial interface
HD_M_CASN	Host Decoder SDRAM column	SYSCLK_5505	
IIB_III_OAOI1	address strobe	SYSCLK_VSM	Video system Clock Host Decoder System clock Versatile Stream
HD_M_CLK	Host Decoder SDRAM clock	OTOOLIN_VOIVI	Manager
HD_M_CSN	Host Decoder SDRAM chip select	TX1P	Transmit data to service serial
HD_M_DQ(15:0)	Host Decoder SDRAM data bus	.,,,,	interface
HD_M_DQML	Host Decoder SDRAM data mask	U_IN	Video U input
	enable(Lower)	U_IN_7118	Video U input to Video Input
HD_M_DQMU	Host Decoder SDRAM data mask		Processor
	enable(Upper)	V_IN	Video V input
HD_M_RASN	Host Decoder SDRAM row address	V_IN_7118	Video V input to Video Input
	strobe		Processor
HD_M_WEN	Host Decoder SDRAM write enable	VCC3_CLK_BUF	Power supply 3V3 clock buffer
ION	Inverted ON: Enable the power	VCC3_VE_MEM	Power supply 3V3 Video Encoder
	supply for the digital board when		Memory
	LOW	VCC3_VSM	Power supply 3V3 Versatile Stream
IRESET_DIG	Initialisation of the digital board, high		Manager
	when power on	VCC3_VSM_MEM	Power supply 3V3 Versatile Stream
JTAG_TCK	JTAG Test Clock		Manager Memory
JTAG_TD_AE_TO_		VCC5_4046	Power supply 5V to PLL IC7806
CON	JTAG Transmitted Data Audio	VDD_EMPIRE	Power Supply of EMPIRE IC
17.4.0. TD. 0.011. T	Encoder to Connector	VDD_MEM	Power Supply for Host Decoder
JTAG_TD_CON_T			flashes(7302,7304)
O_AE	JTAG Transmitted Data Connector	VDD_MEM1	Power Supply for Host Decoder
ITAC TO CON T	to Audio Encoder	VDD 145145	DRAMS(7300, 7301)
JTAG_TD_CON_T	ITAC Transmitted Data Commanday	VDD_MEM2	Power Supply for Host Decoder
O_HD	JTAG Transmitted Data Connector	VDD OT	SDRAM's(7306 and 7307)
JTAG_TD_CON_T	to Host Decoder	VDD_STI	Power Supply for Host Decoder
O_VSM	JTAG Transmitted Data Connector	VDD5_MK2703	Power supply +5V IC7800
O_ V 5W	to Versatile Stream Manager	VDD5_OSC	Power supply +5V IC7802
JTAG_TD_HD_TO	to versame stream Manager	VDDE_7118	Power supply +3V3 Video Input
_CON	JTAG Transmitted Data Host	VDDE_LVC32	Processor
_00.11	Decoder to Connector	VDSP VDSP	Power supply +3V3 IC7551 Power supply +3V3 Digital Sound
JTAG_TD_VE_TO_	booder to commoter	V D61	Processor
CON	JTAG Transmitted Data Video	VE_DATA(15:0)	Video Encoder data Bus
	Encoder to Connector	VE_DSN	Video Encoder Data Strobe
JTAG_TD_VIP_TO		VE_DTACKN	Video Encoder Data Transfer
_VE	JTAG Transmitted Data Video Input		acknowledge
	Processor to Video Encoder	VE_M_A(8:0)	Video Encoder Memory address bus
JTAG_TD_VSM_T		VE_M_CASN	Video Encoder DRAM column
O_VIP	JTAG Transmitted Data Versatile		address strobe
	Stream Manager to Video Input	VE_M_D(63:0)	Video Encoder DRAM data Bus
	Processor	VE_M_OEN	Video Encoder DRAM output enable
JTAG_TMS	JTAG Test Mode Select	VE_M_RASN	Video Encoder DRAM row address
JTAG_TRSTN	JTAG Test part ResetN		strobe
LOAD_DVN	LOAD Digital Video(LOW active)	VE_M_WEN	Video Encoder DRAM write enable
MUTEN	Mute enable	VIP _ICLK	Video Input Processor input Clock
OPT_IN	Audio Optical in	VIP_ERROR	Video Input Processor error
R_IN_7118	Video Red input to Video Input	VIP_FB	Video Input Processor Fast Blanking
D 011#	Processor	VIP_HS	Video Input Processor horizontal
R_OUT	Video red output from Host Decoder		synchronisation
R_OUT_B	Filtered red Video output from Host	VIP_IGP1	Video Input Processor input general
DECETAL FEAR	Decoder		purpose 1
RESETN_5505 RESETN_BE	Reset Host Decoder	VIP_RTS	Video Input Processor ready to send
	System reset basic engine	VIP_VS	Video Input Processor vertical
RESETN_DSP	System reset Digital Sound Processor	VID VIIV/7:0\	synchronisation
RESETN_DVIO	System reset Digital Video Input	VIP_YUV(7:0)	Video Input Processor digital
	Output	\/ CNA NA A/12:0\	video(CC7R 656)
RESETN_EMPIRE	Hardware reset input(active LOW) of	VSM_M_A(13:0)	Versatile Stream Manager SDRAM
	the EMPIRE	VSM_M_CASN	address
RESETN_VIP	System reset Video Input Processor	* OWI_IVI_OAGIN	Versatile Stream Manager SDRAM column address strobe
RESETN_VSM	System reset Versatile Stream	VSM_M_CLKEN	Versatile Stream Manager SDRAM
•	Manager	· OM_W_OLIVEIN	clock enable
RESN_BEN	Reset Basic Engine	VSM_M_CLKOUT	Versatile Stream Manager SDRAM
RESN_DSP	Reset Digital Sound Processor	52,1001	clock out
•	-		· · · · · · · · · · · · · · · · · · ·

		Circuit-, IC Descriptions and List of Abbre	eviations DVDR100	0 /0x1 /691 9. GB 305
	VSM_M_D(0-15)	Versatile Stream Manager SDRAM	CLK27M_CON	27MHz Clock to Digital Board
	VO.W_W_D(0 10)	data bus	CLK27M_DV	27MHz Clock Digital Video Codec
	VSM_M_LDQM	Versatile Stream Manager SDRAM	CLK27M_OSC	27MHz Clock IC7304
		lower data mask enable	CLOCKGENAUD	Clock generator Audio
	VSM_M_RASN	Versatile Stream Manager SDRAM	CLOCKGENVID	Clock generator Video
		row address strobe	CTSN	Clear to Send
	VSM_M_UDQM	Versatile Stream Manager SDRAM	DATA	Data from config ROM
		upper data mask enable	DCLK	Data Clock from config ROM
	VSM_M_WEN	Versatile Stream Manager SDRAM write enable	DV_ASN	DVCODEC Address Strobe
	VSM_UART_CTSN	write eriable	DV_DRQN DV_DSLN	DVCODEC Data Request Interrupt DVCODEC Data Strobe Lower 8 bits
	1	Versatile Stream Manager UART	DV_DSUN	DVCODEC Data Strobe Upper 8
	·	clear to send to analog board	B1_B00.1	Bits
		UART1	DV_DTACKN	DVCODEC Data Transfer
	VSM_UART_CTSN			Acknowledge
	2	Versatile Stream Manager UART	DV_ERRN	DVCODEC Error Interrupt
	LIGHT LIABT DTON	clear to send to DVIO UART2	DV_HS_IN	DVCODEC Horizontal
	VSM_UART_RTSN	Verentile Ctroom Manager LIADT	DV UC OUT	synchronisation In
	1	Versatile Stream Manager UART ready to send to analog board	DV_HS_OUT	DVCODEC Horizontal synchronisation Out
		UART1	DV_LCN	DVCODEC Last Code Interrupt
	VSM_UART_RTSN		DV_PDN	DVCODEC Power Down
	2	Versatile Stream Manager UART	DV_RSTN	DVCODEC System Reset for
		ready to send to DVIO UART2		NW701
	VSM_UART_RX1	Versatile Stream Manager UART	DV_RWN	DVCODEC Read/Write control
		received data to analog board		signal
	VCM HADT DVO	UART1	DV_VS	DVCODEC Vertical synchronisation
	VSM_UART_RX2	Versatile Stream Manager UART received data to DVIO UART2	FIFOA_A(0:15) FIFOA_CEN(0:1)	FIFO buffer A Address bus FIFO buffer A Chip enable
	VSM_UART_TX1	Versatile Stream Manager UART	FIFOA_D(0:7)	FIFO buffer A Data bus
		transmitted data to analog board	FIFOA_OEN	FIFO buffer A Output enable
		UART1	FIFOA_WEN	FIFO buffer A Write enable
	VSM_UART_TX2	Versatile Stream Manager UART	FIFOB_A(0:15)	FIFO buffer B Address bus
	N/ 161	transmitted data to DVIO UART2	FIFOB_CEN(0:1)	FIFO buffer B Chip enable
	Y_IN	Luminance input from analog board	FIFOB_D(0:7)	FIFO buffer B Data bus
	Y_IN_7118	Luminance input to Video Input Processor	FIFOB_OEN FIFOB_WEN'	FIFO buffer B Output enable FIFO buffer B Write enable
	Y_OUT	Luminance output from Host	HAD(0:7)	Host Address/Data bus for register
	_	Decoder	, ,	settings of IC7404
	YC(0-7)	Digital Video Bus for progressive	INIT_CONFN	Initiate Configuration of IC7300
		scan board	IO(0:30)	Data bus of IC7404
0.40.0	Divis Dassel		ISPN	In System Program Line(used for programming IC72O3)
9.12.2	Divio Board		LCASN	Lower Column Address strobe for
	+35V_DV_EDO	+3V3 Power supply EDO Bus		IC7404 DRAMS
	1001_51_550	IC7404	LINKFIFO_DQ(0:7)	Audio/Video data
	+3V3_DLY	+3V3 Power supply for IC7500	LINK_AVCLK	LINK IC Audio/Vide o Interface Clock
	+3V3_DV	+3V3 Power supply for IC7404	LINK_AVERRO	LINK IC indicatesan CRC error
	+3V3_FPGAINT	+3V3 Internal Power supply for	LINK_AVERR1 LINK_AVFSYNC	LINK IC Audio/Video sequence error LINK IC Audio/Video frame sync
		IC7303	LINK_AVSYNC	LINK IC Audio/Vide o packet sync
	+3V3_FPGAIO	+3V3 Power supply for I/O pins of IC	LINK_AVVALID	LINK IC Audio/Vide o data valid
	+3V3_IEEE	7303 +3V3 Isolated Power supply for PHY	LINK_CSN	LINK IC chip selet
	+0 V 0_ILLL	domain	LINK_CYCLEOUT	LINK IC Cycle clc⋅κ
	+3V3_LINK	+3V3 Power supply iC7103	LINK_INTN	LINK IC interrupt
	+3V3_PLL	+3V3 Power supply IC7307 &	OE	Output enable
		IC7308	PA(0:15)	SRAM processoraddress
	+3V3_SRAM	+3V3 Power supply IC7301, IC7302,	PAD(0:7) PALE	SRAM processordata Processor Address Latch Enable
	.EV DDOO	IC7305 & IC7306	PHY_CNA	PHY 1394 cable to 1 active
	+5V_PROC	+5V Power supply IC7200, IC7201, IC7203 & IC7208	PHY_LPS	LINK IC power status
	+VCC_DV_RAM	+3V3 Power supply for	PINTON	Processor interrujt 0
		DV_RAM(IC7400> IC7404)	PINT1N	Processor interrupt 1
	1394_RSTN	Reset of LINK IC(7103) and PHY	PORT1_1	Unused free port
	1 (0.0)	IC(7101)	PPSENN' PRDN	Program store en₀b le Processor read
	A(0:8)	Address lines	PRSTN	Processor reset
	AUD_BCLK AUD_MUTE	Audio Bit Clock Audio Mute	PT0	Processor timer 0
	AUD_SDI	Audio Mute Audio Serial Data Input	PT1	Processor timer 1
	AUD_SDO	Audio Serial Data Output	PWRN	Processor write
	AUD_WS	Audio Word Select	RASN	Row address strole
	BUFENN_AUD	Buffer Enable Audio	RESETN	DVIO board reset
	BUFENN_VID	Buffer Enable Video	RTSN RXD	System Reset Receive Data
	CEN	Control Enable	SRAMCE0N	SRAM processor the ip enable O

SRAMCE0N

SRAM processor in ip enable O

GB 306 9. DVDR1000 /0x1 /691 Circuit-, IC Descriptions and List of Abbreviations

SRAMCE1N SRAM processor chip enable 1 SRAMRDN SRAM processor output enable TCK Boundary scan Test Clock TDI Boundary scan Test Data Input TDO Boundary scan Test Data Output TMS Boundary scan Test Mode Select Transmitted Data TXD **UCASN** Upper column address strobe WEN Write Enable control signal to SRAM

YUV(0:7) Digital Video GND Ground

GND_IEEE Ground IEEE

9.12.3 Progressive Scan

+2V5_FLI +2V5 Power Supply for IC7101 +2V5_PLL +2V5 Power Supply for PLL +3V3 +3V3 Power Supply

+3V3_ANA +3V3 Power Supply Analogue +3V3_DD +3V3 Power Supply Digital +3V3_FLI +3V3 Power Supply for IC7101 +5V +5V Power Supply

BA Bank Address
CAS Column Address strobe
CB_OUT(0:9) Chrominance Blue out
CLK_27MHZ 27MHz Clock

CLK4 SDRAM clock
CR_OUT(0:9) Chrominance Red out

D_ADDR(0:10) Address bus
D_DATA(0:29) Data bus
FRAME_IN Picture FrAME
GND Ground

HS_IN Horizontal synchronisation IN HSOUT Horizontal synchronisation OUT

RAS Row Address strobe
SCL I2C bus clock
SDA I2C bus data

VS_IN Vertical synchronisation IN VSOUT Vertical synchronisation OUT

WE Write Enable

Y_OUT(0:9) Luminance output from FLI

YUV_IN(0:7) Digital Video bus

10. Spare Parts List

VAR						ī		
 Variou	IOUS		1157		SWITCH TACT PUSH	3133		22k 5% 0.062W
Variou			1158 1159		SWITCH TACT PUSH SWITCH TACT PUSH	3134 3135		10k 5% 0.062W NTC DC 5W 10k 5%
	us		1160		SWITCH TACT PUSH	3136		4k7 5% 0.062W
			1161		SWITCH TACT PUSH	3137		4k7 5% 0.062W
0027	3104 120 00370	VIDEO PLUS EUR SILVER	1162		SWITCH TACT PUSH	3138	4822 051 30103	10k 5% 0.062W
0027	3104 120 00380	(/051) G-CODE ASIA SILVER	1163		SWITCH TACT PUSH	3139		390Ω 5% 0.062W
		(/691)	1165 1166		SWITCH TACT PUSH SWITCH TACT PUSH	3140 3141		220Ω 5% 0.062W 4k7 5% 0.062W
0027		SHOW VIEW EUR SILVER	1167		SWITCH TACT PUSH	3142		47k 1% 0.063W 0603
0050 0065	3104 120 00272	TRAY FRONT ASSY	1168		SWITCH TACT PUSH	3143		10k 5% 0.062W
0005	3104 127 11143	COMPLETE	1169		SWITCH TACT PUSH	3144		390Ω 5% 0.062W
0081	9305 025 81001		1170		SWITCH TACT PUSH SWITCH TACT PUSH	3145 3146		10k 5% 0.062W 10k 5% 0.062W
0151	3104 127 11162		1172		SWITCH TACT PUSH	3147		10k 5% 0.062W
0191	3104 124 07455	FILTER AIR INLED BOTTOM	1173		SWITCH TACT PUSH	3148		2k2 5% 0.062W
0197	3104 123 30002		1174 1175		SWITCH TACT PUSH	3149 3150		4k7 5% 0.062W
0198	3104 124 07733	FILTER AIR INLET COVER	1176		SWITCH TACT PUSH SWITCH TACT PUSH	3130	4622 051 30362	5k6 5% 0.063W 0603 RC2* RST SM
0199 0251		DC BRUSHLESS FAN	1177		SWITCH TACT PUSH	3151	4822 051 30102	
0252		FOOT SILVER ASSY FOOT SILVER ASSY	1178	2422 128 02947	SWI DET 1P 0,1A 30V	3152	4822 116 52257	
0253		FOOT SILVER ASSY	1179	2422 128 02947	SPP85 SWI DET 1P 0,1A 30V	3153	2322 704 65608	RST SM 603 RC22H 5Ω6 PM1
0254		FOOT SILVER ASSY	' ' '	2 122 120 02041	SPP85	3154	4822 050 21003	
0309	3104 125 24080	UM DVDR1000/001 MID EU	1910	2422 033 00355		3155		2k2 5% 0.062W
0309	3104 125 24090	UM DVDR1000/051 UK	1911		CON BM H 9P M 2.00 PH B	3156	4822 050 21003	
0309		UM DVDR1000/021	1916	2422 025 10//2	CON BM V 12P M 2.00 PH B	3157 3158	4822 116 83884 4822 051 30223	47K 5% 0.5W 22k 5% 0.062W
0000	040440504455	NORDIC	1917	3103 140 27931	CABLE TREE ASSY 7P	3159		5k6 5% 0.063W 0603 RC21
0309 0324		UM DVDR1000/691 ASIA CORDON ANT. L.1,50M	1918	2412 020 00724	CON BM V 2P M 2.50 EH B			RST \$M
1001		DVDR 4278 DIGITAL				3160	2322 704 65608	RST \$M 603 RC22H 5Ω6 PM1
		BOARD MODULE	⊣⊢			3161	4822 116 52297	
1002	3122 427 22711	PSU DVDR1000-2 EURO	2102	4000 406 44044	0603 50V 330P COL R	3162		68k 5% O.062W
1003	3103 608 50010	50PS203 DVDR ANALOG BOARD	2102		0603 50V 330P COL R	3163		10k 5% O.062W
1000	0100 000 00010	EUROP	2106		100nF 10% 16V 0603	3164 3165	4822 050 21003 4822 051 30222	
1005		DVDR 4316 DVIO BOARD	2120	4822 124 80791	470μF 16V 20% 105C	3166	4822 116 83876	
8001	3104 157 11641	CWAS FLEX DVD 22 70	2121	4922 126 14205	DXH=8X11.5 100nF 10% 16V 0603	3167	4822 116 83876	
8002	3104 157 11641	32S CWAS FLEX DVD 22 70	2122		10nF 10% 50V 0603	3168	4822 116 52175	
0002		32S	2123	5322 126 11583	10nF 10% 50V 0603	3169 3171	4822 051 30103	10K 5% O.062W 2k2 5% O.062W
8003	3104 157 11790		2124		10nF 10% 50V 0603	3172	4822 051 30472	
8004	3104 157 11531	32S CWAS FLEX DVD 10 110	2140 2150	4822 124 11946 4822 124 80231		3173	4822 051 30103	
0004	0104 107 11001	32S	2151		100nF 10% 16V 0603	3174 3175	4822 051 30475 4822 051 30103	4M7 5% 0.062W
8013	3104 128 92921	CABLE IEEE-1394 4P AMP	2152		47nF 5% 250V	3176		470Ω5% 0.062W
			2154 2155	4822 124 40849	330μF 20% 16V 100nF 10% 16V 0603	3177	4822 051 30102	1k 5%0.062W
B			2156		0603 50V 100NP80M	3178	4822 051 30222	
TOOL	2104 129 07770	PCB EXTENDER DVIO	2157		10nF_10% 50V 0603	3179 3180	4822 116 52283 4822 051 30103	
TOOL	3104 120 07770	FUD EXTENDED DVIO	2158		100nF 10% 16V 0603			
						3182	4022 00 1 00 102	1k5 5% O.062W
		ASSY	2159	2238 586 59812	0603 50V 100NP80M	3183	4822 051 30222	2k2 5% O.062W
	NT ACCV			2238 586 59812 4822 126 14305		3183 3184	4822 051 30222 4822 051 30221	2k2 5% O.062W 220Ω5% 0.062W
FRO	NT ASSY		2159 2160 2161 2165	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603	3183 3184 3185	4822 051 30222 4822 051 30221 4822 051 30471	2k2 5% O.062W 220Ω5% 0.062W 470Ω5% 0.062W
			2159 2160 2161 2165 2167	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V	3183 3184 3185 3186 3187	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30222	2k2 5% O.062W 220Ω3% O.062W 470Ω3% O.062W 1k 5%0.062W 2k2 5% O.062W
FROI Variou			2159 2160 2161 2165	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 122 31765	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V	3183 3184 3185 3186 3187 3188	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30222 4822 051 30472	2k2 5% O.062W 220Ω 5% O.062W 470Ω 5% O.062W 1k 5% O.062W 2k2 5% O.062W 4k7 5% O.062W
	JS		2159 2160 2161 2165 2167 2168 2170 2171	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 122 31765 5322 126 11583 4822 126 13879	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V	3183 3184 3185 3186 3187 3188 3189	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30222 4822 051 30472 4822 051 30103	2k2 5% O.062W 220Ω5% O.062W 470Ω5% O.062W 1k 5% O.062W 2k2 5% O.062W 4k7 5% O.062W 10k 5% O.062W
Variou 0001 0003	JS 3104 127 12993 3104 127 12287	FRONT & DOOR ASSY FRONT ASSY	2159 2160 2161 2165 2167 2168 2170 2171 2173	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 122 31765 5322 126 11583 4822 126 13879 5322 126 11583	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603	3183 3184 3185 3186 3187 3188	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30222 4822 051 30472 4822 051 30103 4822 117 12925	2k2 5% O.062W 220Ω 5% O.062W 470Ω 5% O.062W 1k 5% O.062W 2k2 5% O.062W 4k7 5% O.062W
Variou 0001 0003 0004	3104 127 12993 3104 127 12287 3104 127 12880	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 122 31765 5322 126 11583 4822 126 13879 5322 126 11583 4822 126 14305	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30222 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30221 4822 051 30102	2k2 5% O.062W 220Q3% 0.062W 470Q3% 0.062W 1k 5% 0.062W 2k2 5% O.062W 4k7 5% O.062W 10k 5% O.062W 47k 1% O.063W 0603 220Q3% 0.062W 1k 5% 0.062W
Variou 0001 0003 0004	3104 127 12993 3104 127 12287 3104 127 12880	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT	2159 2160 2161 2165 2167 2168 2170 2171 2173	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 122 31765 5322 126 11583 4822 126 13879 5322 126 11583 4822 126 14305 3198 017 41050	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192 3193	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30222 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30221 4822 051 30102 4822 051 30103	2k2 5% O.062W 220Ω;% O.062W 470Ω;% O.062W 1k 5% O.062W 2k2 5% O.062W 4k7 5% O.062W 10k 5% O.062W 47k 1% O.063W 0603 220Ω;% O.062W 1k 5% O.062W 10k 5% O.062W
0001 0003 0004 0006	3104 127 12993 3104 127 12287 3104 127 12880 3104 127 12292 3104 124 05450	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2175 2177 2179	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13879 5322 126 11583 4822 126 13879 5322 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 5322 126 11583	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 0603 10V 1μF COL R 10nF 10% 50V 0603 10nF 10% 50V 0603	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192 3193 3194	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30222 4822 051 30103 4822 117 12925 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103	2k2 5% O.062W 220Ω 5% O.062W 470Ω 5% O.062W 1k 5% O.062W 4k7 5% O.062W 4k7 5% O.062W 10k 5% O.062W 47k 1% O.063W 0603 220Ω 5% O.062W 1k 5% O.062W 1k 5% O.062W 2k2 5% O.062W
0001 0003 0004 0006	3104 127 12993 3104 127 12897 3104 127 12880 3104 127 12292	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR HOLDER LEFT	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2175 2177	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13879 5322 126 11583 4822 126 13879 5322 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 5322 126 11583	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 0603 10V 1µF COL R 10nF 10% 50V 0603	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192 3193 3194 3195 3196	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30222 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30221 4822 051 30102 4822 051 30103	2k2 5% O.062W 220Ω;% O.062W 470Ω;% O.062W 1k 5% O.062W 2k2 5% O.062W 4k7 5% O.062W 10k 5% O.062W 47k 1% O.063W 0603 220Ω;% O.062W 1k 5% O.062W 10k 5% O.062W 1k 5% O.062W 1k 5% O.062W 1k 5% O.062W
0001 0003 0004 0006 0010 0012	3104 127 12993 3104 127 12287 3104 127 12880 3104 127 12292 3104 124 05450 3104 127 12873	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR HOLDER LEFT COMPLETE	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2175 2177 2179 2180	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13879 5322 126 11583 4822 126 13879 5322 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 5322 126 11583	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 0603 10V 1μF COL R 10nF 10% 50V 0603 10nF 10% 50V 0603	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192 3193 3194 3195 3196 3197	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30472 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30102 4822 051 30102 4822 051 30222 4822 051 30222 4822 051 30222 4822 051 30222 4822 051 30222	2k2 5% O.062W 220Ω;% O.062W 470Ω;% O.062W 1k 5% O.062W 2k2 5% O.062W 4k7 5% O.062W 47k 1% O.063W 0603 220Ω;% O.062W 1k 5% O.062W 1k 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W
0001 0003 0004 0006 0010 0012	3104 127 12993 3104 127 12287 3104 127 12880 3104 127 12292 3104 124 05450 3104 127 12873	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR HOLDER LEFT	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2175 2177 2179	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13879 5322 126 11583 4822 126 13879 5322 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 5322 126 11583	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 0603 10V 1μF COL R 10nF 10% 50V 0603 10nF 10% 50V 0603	3183 3184 3185 3186 3187 3188 3190 3191 3192 3193 3194 3195 3196 3197 3198	4822 051 30222 4822 051 30221 4822 051 30471 4822 051 30102 4822 051 30222 4822 051 30103 4822 051 30103 4822 051 30102 4822 051 30102 4822 051 30103 4822 051 30222 4822 051 30222 4822 051 30222 4822 051 30222 4822 051 30222 4822 051 30221	2k2 5% O.062W 220Ω;% O.062W 470Ω;% O.062W 2k5 % O.062W 4k7 5% O.062W 10k 5% O.062W 47k 1% O.063W 0603 220Ω;% O.062W 10k 5% O.062W 10k 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W
0001 0003 0004 0006 0010 0012 0014	3104 127 12993 3104 127 12287 3104 127 12880 3104 127 12892 3104 127 12292 3104 124 05450 3104 127 12873 3104 120 00340 4822 380 20505	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR HOLDER LEFT COMPLETE WORDMARK PHILIPS SILVER LIGHT TRANSMITTER	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2175 2177 2179 2180	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13881 4822 126 11583 4822 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 4822 126 14305	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 0603 10V 1μF COL R 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192 3193 3194 3195 3196 3197	4822 051 30222 4822 051 30221 4822 051 30171 4822 051 30102 4822 051 30472 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30222 4822 051 30222 4822 051 30222 4822 051 30472 4822 051 30472	2k2 5% O.062W 220Ω3% O.062W 470Ω3% O.062W 1k 5% O.062W 2k2 5% O.062W 4k7 5% O.062W 10k 5% O.062W 2c0Ω3% O.062W 1k 5% O.062W 1k 5% O.062W 1k 5% O.062W 1k 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k3 5% O.062W 2k4 5% O.062W 2k3 5% O.062W 2k4 5% O.062W 2k7 5% O.062W 4k7 5% O.062W 470Ω3% O.062W
0001 0003 0004 0006 0010 0012 0014 0016 0019	3104 127 12993 3104 127 12287 3104 127 12880 3104 127 12892 3104 124 05450 3104 127 12873 3104 120 00340 4822 380 20505 3104 127 11132	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR HOLDER LEFT COMPLETE WORDMARK PHILIPS SILVER LIGHT TRANSMITTER INNER DOOR ASSY	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2175 2177 2179 2180	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13879 5322 126 11583 4822 126 13879 5322 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 4822 126 14305 4822 126 14305	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 0603 10V 1μF COL R 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192 3193 3194 3195 3196 3197 3198 3199	4822 051 30222 4822 051 30221 4822 051 30171 4822 051 30102 4822 051 30472 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30222 4822 051 30222 4822 051 30221 4822 051 30221 4822 051 30221 4822 051 30247 4822 051 30471 4822 051 30471	2k2 5% O.062W 220Ω;% O.062W 470Ω;% O.062W 2k5 % O.062W 4k7 5% O.062W 10k 5% O.062W 47k 1% O.063W 0603 220Ω;% O.062W 10k 5% O.062W 10k 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W
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Variou 0001 0003 0004 0006 0010 0012 0014 0016 0019 0020 0029 0051 1004 1006 DISP	3104 127 12993 3104 127 12287 3104 127 12880 3104 127 12292 3104 124 05450 3104 127 12873 3104 120 00340 4822 380 20505 3104 127 11132 3104 127 11912 3104 127 11883 3103 608 50030 3104 128 07610	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR HOLDER LEFT COMPLETE WORDMARK PHILIPS SILVER LIGHT TRANSMITTER INNER DOOR ASSY INNER DOOR ASSY LEFT IR-WINDOW MOTOR ASSY DVDR DISPLAY BOARD PCB ASSY 4319 DVIO- FRONT	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2175 2177 2180 ————————————————————————————————————	2238 586 59812 4822 126 14305 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13879 5322 126 11583 4822 126 13879 5322 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 4822 126 14305 4822 126 14305 4822 126 130102 4822 051 30102 4822 051 30105 4822 051 30759 4822 051 30759 4822 051 30759 4822 051 30759 4822 051 30759 4822 051 30103 4822 051 3023 4822 051 30223 4822 051 30223 4822 051 303223 4822 051 30392 4822 051 30392 4822 051 30392 4822 051 30392 4822 051 30392	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 0603 10V 1μF COL R 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 50V 0603 10nF 10% 16V 0603	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192 3193 3194 3195 3196 3197 3198 4xxx 4xxx 5150 5151 5153	4822 051 30222 4822 051 30221 4822 051 30121 4822 051 30102 4822 051 30472 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30222 4822 051 30221 4822 051 30221 4822 051 30221 4822 051 30471 4822 051 30471 4822 051 30471 4822 051 30474 4822 157 51462 4822 157 51462 2422 531 02423	2k2 5% O.062W 220Ω 5% O.062W 470Ω 60.062W 1k 5% O.062W 4k7 5% O.062W 4k7 5% O.062W 10k 5% O.062W 2k2 5% O.062W 10k 5% O.062W 1k 5% O.062W 1k 5% O.062W 20Ω 5% O.062W 20Ω 60.062W 20Ω 60.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2c2 0Ω 9% O.
Variou 0001 0003 0004 0006 0010 0012 0014 0016 0019 0029 0051 1004 1006 DISP Variou	3104 127 12993 3104 127 12287 3104 127 12880 3104 127 12892 3104 124 05450 3104 127 12873 3104 120 00340 4822 380 20505 3104 127 11132 3104 127 11912 3104 124 07213 3104 127 11883 3103 608 50030 3104 128 07610	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR HOLDER LEFT COMPLETE WORDMARK PHILIPS SILVER LIGHT TRANSMITTER INNER DOOR ASSY INNER DOOR ASSY INNER DOOR ASSY IR-WINDOW MOTOR ASSY DVDR DISPLAY BOARD PCB ASSY 4319 DVIO-	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2175 2177 2180 	2238 586 59812 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13881 4822 126 11583 4822 126 11583 4822 126 11583 4822 126 11583 4822 126 11583 4822 126 11583 5322 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 4822 126 14305 4822 051 30102 4822 051 30102 4822 051 30105 4822 051 30759 4822 051 30768	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 100nF 10% 50V 0603 10nF 10% 16V 0603	3183 3184 3185 3186 3187 3188 3190 3191 3192 3193 3194 3195 3196 3197 4xxx 4xxx 5150 5151 5153	4822 051 30222 4822 051 30221 4822 051 30121 4822 051 30102 4822 051 30472 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30222 4822 051 30221 4822 051 30221 4822 051 30221 4822 051 30471 4822 051 30471 4822 051 30471 4822 051 30474 4822 157 51462 4822 157 51462 2422 531 02423	2k2 5% O.062W 220Ω3% O.062W 470Ω3% O.062W 1k 5% O.062W 2k2 5% O.062W 4k7 5% O.062W 4k7 5% O.062W 4k7 5% O.062W 4k8 O.062W 4k8 O.062W 4k8 O.062W 4k8 O.062W 4k9 O.062W
Variou 0001 0003 0004 0006 0010 0012 0014 0016 0019 0020 0029 11004 11006 DISP Variou 1140 1150	3104 127 12993 3104 127 12287 3104 127 12880 3104 127 12892 3104 124 05450 3104 127 12873 3104 120 00340 4822 380 20505 3104 127 11132 3104 127 11912 3104 127 11912 3104 127 1182 3103 608 50030 3104 128 07610	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR HOLDER LEFT COMPLETE WORDMARK PHILIPS SILVER LIGHT TRANSMITTER INNER DOOR ASSY INNER DOOR ASSY INNER DOOR ASSY INNER DOOR ASSY INNER DOOR ASSY IR-WINDOW MOTOR ASSY DVDR DISPLAY BOARD PCB ASSY 4319 DVIO- FRONT SWITCH TACT PUSH PROT DEV 65V 250MA PSC A	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2177 2179 2180 	2238 586 59812 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13881 4822 126 11583 4822 126 11583 4822 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 4822 126 14305 4822 051 30102 4822 051 30102 4822 051 30105 4822 051 30759 4822 051 30759 4822 051 30759 4822 051 30759 4822 051 30101 4822 051 30103 4822 051 30103 4822 051 3092 4822 117 12917 4822 117 12917 4822 117 12917 4822 117 12917 4822 051 30103 4822 051 30103	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 0603 10V 1μF COL R 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 16V 0603	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192 3193 3194 3195 3196 3197 3198 4xxx 4xxx 5150 5151 5153	4822 051 30222 4822 051 30221 4822 051 30121 4822 051 30102 4822 051 30472 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30122 4822 051 30222 4822 051 30222 4822 051 30222 4822 051 30224 4822 051 30224 4822 051 30224 4822 051 30472 4822 051 30472 4822 051 30472 4822 051 30472 4822 051 30472 4822 051 30473 4822 157 51462 4822 157 51462	2k2 5% O.062W 220Ω3% O.062W 470Ω3% O.062W 1k 5% O.062W 4k7 5% O.062W 10k 5% O.062W 4k7 5% O.062W 10k 5% O.062W 1k 5% O.062W 1k 5% O.062W 1k 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2k2 5% O.062W 2b2 5% O.062W 2c2 Ω3% O.062W 2c3 Ω3% O.062W 2c3 Ω3% O.062W 2c4 05% O.062W 2c4 05% O.062W 2c4 05% O.062W 2c4 05% O.062W 2c5% O.062W 2c6 05% O.062W 2c7 0.062W 2c7
Variou 0001 0003 0004 0006 0010 0012 0014 0016 0019 0020 0029 0051 1004 1006 DISP Variou 1140 1150	3104 127 12993 3104 127 12287 3104 127 12880 3104 127 12292 3104 124 05450 3104 127 12873 3104 120 00340 4822 380 20505 3104 127 11132 3104 127 11132 3104 127 11883 3103 608 50030 3104 128 07610	FRONT & DOOR ASSY FRONT ASSY WINDOW ASSY HOLDER RIGHT COMPLETE LIGHT CONDUCTOR HOLDER LEFT COMPLETE WORDMARK PHILIPS SILVER LIGHT TRANSMITTER INNER DOOR ASSY INNER DOOR ASSY INNER DOOR ASSY DVDR DISPLAY BOARD PCB ASSY 4319 DVIO- FRONT SWITCH TACT PUSH PROT DEV 65V 250MA	2159 2160 2161 2165 2167 2168 2170 2171 2173 2174 2175 2177 2180 	2238 586 59812 4822 126 14305 5322 126 11583 4822 126 13881 4822 126 13881 4822 126 11583 4822 126 11583 4822 126 11583 4822 126 11583 4822 126 11583 4822 126 11583 5322 126 11583 4822 126 14305 3198 017 41050 5322 126 11583 4822 126 14305 4822 051 30102 4822 051 30102 4822 051 30105 4822 051 30759 4822 051 30768	0603 50V 100NP80M 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 470pF 5% 50V 100pF 2% 63V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 220nF 20% 16V 10nF 10% 50V 0603 100nF 10% 16V 0603 0603 10V 1μF COL R 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 16V 0603 1k 5% 0.062W 1M 5% 0.062W 15Ω 5% 0.062W 15Ω 5% 0.062W 15Ω 5% 0.062W 10Ω 5% 0.062W	3183 3184 3185 3186 3187 3188 3189 3190 3191 3192 3193 3194 3195 3196 3197 4xxx 4xxx 5150 5151 5153 →I	4822 051 30222 4822 051 30221 4822 051 30121 4822 051 30102 4822 051 30222 4822 051 30472 4822 051 30103 4822 117 12925 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30222 4822 051 30221 4822 051 30221 4822 051 30221 4822 051 3021 4822 051 30471 4822 051 30471 4822 051 30472 4822 157 51462 4822 157 51462 4822 157 51462 9322 146 61685	2k2 5% O.062W 220Ω;% O.062W 470Ω;% O.062W 1k 5% O.062W 1k5% O.062W 10k5% O.062W 10k5% O.062W 10k5% O.062W 10k5% O.062W 1k 5% O.062W 1k5% O.062W 1k5% O.062W 1k5% O.062W 20Ω;% O.062W 20Ω;% O.062W 2k2 5% O.062W 2k2 5% O.062W 220Ω;% O.062W 220Ω;% O.062W 220Ω;% O.062W 47 00;% O.062W 47 00;% O.062W 47 00;% O.062W 47 00;% O.062W 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K 10μH 10% 4X9.8MM LAL041 00K

GB 308 1	0. DVDR10	00 /0x1 /691	Spare Parts List
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6103	9322 146 61685	DIO REG SM DF3A6.8FU	<u> </u>			2005	4822 126 14305	100nF 10% 16V 0603
6104	9322 146 61685	TOSJ DIO REG SM DF3A6.8FU	DIVI	O FRONT		2006 2007	4822 124 40433 4822 126 13883	
6140	9322 140 17676	TOSJ	Vario	ıe		2008	4822 126 14241	0603 50V 330P COL R
0140	9322 140 17676	14CHJ(LITO)A				2009 2010		100nF 10% 16V 0603 100nF 10% 16V 0603
6150	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)	1000 1001		CON BM H 4P F 0.8 B CON BM H 4P F 0.8 IEEE R	2011 2012	4822 124 40433	47μF 20% 25V 100nF 10% 16V 0603
6151	4822 130 83757	BAS216				2013	4822 124 40433	47μF 20% 25V
6152	9340 260 20115	DIO SIG SM BAW56W(PHSE) R	⊣⊢			2014 2015	4822 126 14305 4822 124 40433	100nF 10% 16V 0603
6154	9322 102 64685	DIO REG SM UDZ2.7B	2000	5322 126 10511	1nF 5% 50V	2016	4822 126 14305	100nF 10% 16V 0603
6155	9340 260 20115		2001 2002	5322 126 10511 2020 557 90732	1nF 5% 50V 250V 4N7 PM10 R	2017 2018	4822 124 40433 4822 126 13883	
6156	4822 130 83757	BAW56W(PHSE) R BAS216	2003	2020 557 90732	250V 4N7 PM10 R	2019 2024	4822 126 14305 4822 122 33777	100nF 10% 16V 0603
6157	4822 130 30621	1N4148	2004 2005		250V 4N7 PM10 R 250V 4N7 PM10 R	2030	4822 124 41584	100μF 20% 10V
6158 6159	4822 130 30621 4822 130 30621					2321 2322		100nF 10% 16V 0603 100nF 10% 16V 0603
6160	9340 260 20115	DIO SIG SM BAW56W(PHSE) R	┌──			2323 2324		0603 16V 47nF COL 16V 330nF PM10
6161	9340 260 20115	DIO SIG SM	3000	4822 051 20105	1M 5% 0.1W	2325	4822 126 14305	100nF 10% 16V 0603
6164	4822 130 30621	BAW56W(PHSE) R 1N4148				2328		100μF 20% 10V 0603 10V 470nF COL
6165 6166	4822 130 30621 4822 130 30621					2332	4822 124 40207	100μF 20% 25V
6167	4822 130 30621	1N4148	5000	2422 549 44768	IND FXD SM EMI 100mH z 90R R	2400 2401	4822 126 14305	10nF 10% 50V 0603 100nF 10% 16V 0603
6168	9340 260 20115	DIO SIG SM BAW56W(PHSE) R	5001	2422 549 44768	IND FXD SM EMI 100mH z	2402 2403	4822 126 14305 4822 124 40433	100nF 10% 16V 0603
6169	9340 260 20115	DIO SIG SM			90R R	2404	5322 126 11583	10nF 10% 50V 0603
6170	9340 260 20115		→			2405 2406		10nF 10% 50V 0603 1nF 10% 50V 0603
6171	9340 260 20115	BAW56W(PHSE) R	6000	4822 130 11395	TI MH3100	2407 2408	4822 126 14305	100nF 10% 16V 0603 1nF 10% 50V 0603
		BAW56W(PHSE) R	6001		DIO SUP SM6T39CA	2430	5322 126 11583	10nF 10% 50V 0603
6172	9340 260 20115	DIO SIG SM BAW56W(PHSE) R			(ST00) R	2431 2432	4822 124 40433 5322 126 11583	47μF 20% 25V 10nF 10% 50V 0603
6173	9340 260 20115	DIO SIG SM BAW56W(PHSE) R	Λ NI Λ	LOG PWB		2433	4822 124 81151	22μF 50V
6174	9340 260 20115	DIO SIG SM		LOG FWB		2434 2436	4822 124 40207 4822 124 81151	
6175	4822 130 30621	BAW56W(PHSE) R 1N4148	Variou	ıs		2437 2438		100nF 10% 16V 0603 100nF 10% 16V 0603
6176 6177	4822 130 30621 4822 130 30621	1N4148	1324▲	2422 086 10954	PROT DEV 65V 1A PSC	2439	4822 124 81151	22μF 50V
6178	4822 130 30621				PROT DEV 65V 500MA PSC	2440 2441	4822 124 40207 4822 124 81151	
6179 6180	4822 130 30621 4822 130 30621				PROT DEV 65V 1A PSC	2442 2443	4822 124 11947 4822 124 11947	10μF 20% 16V
6181	4822 130 30621	1N4148	1327▲	2422 086 10951	PROT DEV 65V 500MA PSC	2446	4822 126 13881	470pF 5% 50V
6182 6183	4822 130 30621 4822 130 30621		1600	4822 242 10434	L1101-95263-	2447 2460	4822 126 13881 4822 124 40433	
6184 6185	4822 130 30621 4822 130 30621		1700	4822 242 81436	0E1(18,432MHz) OFWK3953M	2461	4822 124 40769	4.7μF 20% 100V
6186	4822 130 30621	1N4148	1701 1702	4822 242 10307	OFWG3956M FIL SAW 38MHz 9	2462 2463	4822 124 40433 4822 124 40769	4.7μF 20% 100V
6187 6188	4822 130 30621 4822 130 30621				OFWK9656M	2464 2465		100nF 10% 16V 0603 100nF 10% 16V 0603
6189 6190	4822 130 30621 4822 130 30621		1703 1705		TPS5,5MB-TF20 TUNER UV1316MK3(NON	2466	5322 126 11583	10nF 10% 50V 0603
6191	4822 130 30621	1N4148	1802	2/22 5/3 01153	EURO) RES XTL 32KHZ768 12P5	2467 2468	4822 126 13881 4822 126 13881	
6192 6193	4822 130 30621 4822 130 30621				DT-38 B	2469 2470		0603 10V 1μF COL R 100nF 10% 16V 0603
6194 6195	4822 130 30621	1N4148	1900 1932		52030-2210 (22P) CON BM V 07P M 2.50 EH	2473	4822 122 33753	150pF 5% 50V
6196	4822 130 30621 4822 130 30621		1943	9322 155 28667	В	2474 2477		100nF 10% 16V 0603 100nF 10% 16V 0603
6197 6198	4822 130 30621 4822 130 83757				GP1FA550TZ (SRPJ)L	2481 2483	2222 867 15339	0603 50V 33P PM5 0603 10V 1μF COL R
			1945	2422 026 05197	CON BM CINCH H 1P F BK	2484	5322 126 11578	1nF 10% 50V 0603
- BO			1950	2422 033 00334	CON BM EURO H 42P F	2500 2501		100nF 10% 16V 0603 100nF 10% 16V 0603
7120	4822 209 30146	L2722	1953		BK GRND-L CON BMT 9P VERT PH-B	2502 2503	4822 124 40769 4822 124 40769	4.7μF 20% 100V
7140 7141	9322 155 22667 4822 130 61553	DTC124EU			52030-2210 (22P) CON BM MDIN 8P F	2505	4822 126 14305	100nF 10% 16V 0603
7142 7143	3198 010 42310	BC847BW			TCX0310B	2506 2507		100nF 10% 16V 0603 100nF 10% 16V 0603
7144	5322 130 42756 5322 130 42756		1958	2422 026 05093	CON BM CINCH 4P F 2*WHRD	2508	4822 124 40433	47μF 20% 25V
7145 7150	3198 010 42310 2722 171 07721	BC847BW VFD BJ-801GNK 120X32	1959	2422 026 05096	CON BM CINCH H 2P F YEYE	2509 2510	4822 124 40769 4822 124 40433	
7151	3198 010 42310	BC847BW		4822 267 10565	4P	251 1 2512	4822 122 33777 4822 122 33777	
7152	9322 148 79668	STN3NE06(ST00)		4822 267 11031 2422 086 10919	PROT DEV 65V 125MA	2513	4822 126 14305	100nF 10% 16V 0603
7153 7155	3198 O10 42310 3198 O10 42310		1984	2412 020 00724	MP13	2514 2515	4822 126 14305 4822 124 40769	100nF 10% 16V 0603 4.7μF 20% 100V
7156		OTPROM ASSY DDCP1-			CON BM V 2P M 2.50 EH B CON BM V 12P M 2.00 PH	2516 2517	3198 017 41050	0603 10V 1μF COL R 0603 10V 1μF COL R
7157	3198 010 42310	1U BC847BW	1990	4822 242 73552	B 13.875 000 MHz	2518	3198 017 41050	0603 10V 1μF COL R
7160 7164	5322 209 11147	HEF4093BT			20MHz 20P AT-49	2519 2520	3198 017 41050 4822 124 41584	0603 10V 1µF COL R 100µF 20% 10V
7165	3198 O10 42310 4822 130 61553	DTC124EU				2521 2522	4822 126 14305	100nF 10% 16V 0603
7166	3198 O10 42310	BC847BW				2523	4822 126 14305	0603 10V 1µF COL R 100nF 10% 16V 0603
					22nF 10% 25V 0603 0603 50V 330P COL R	2524 2525		0603 10V 1μF COL R 0603 10V 1μF COL R
			2003		22nF 10% 25V 0603	2526 2527	4822 126 14305	100nF 10% 16V 0603 100nF 10% 16V 0603
			2004	TULE 124 4U433		2527 2528		100nF 10% 16V 0603 0603 10V 1µF COL R
					•			

3485

3486

4822 051 30102

1k 5% (62W

4822 051 30151 150Ω 5₈ 0.062W

```
2529
        4822 126 14305
                       100nF 10% 16V 0603
                                                 2902
                                                         4822 126 14305
                                                                        100nF 10% 16V 0603
                                                                                                   3020
                                                                                                          4822 117 12903 1k8 1% 0.063W 0603
                       0603 10V 1μF COL R
       3198 017 41050
2530
                                                         4822 126 13879
                                                                        220nF 20% 16V
                                                 2903
                                                                                                   3030
                                                                                                          4822 117 12139 220 5% 0.062W
        4822 126 14305
                       100nF 10% 16V 0603
                                                  2904
                                                         3198 017 41050
2531
                                                                         0603 10V 1uF COL R
                                                                                                   3032
                                                                                                          4822 051 30008
                                                                                                                         0Ω iumper
                                                         4822 124 40433
                                                                                                                         1k8 1% 0.063W 0603
2532
        4822 124 11947
                       10µF 20% 16V
                                                  2905
                                                                         47μF 20% 25V
                                                                                                   3032
                                                                                                          4822 117 12903
2533
        4822 124 11947
                       10µF 20% 16V
                                                  2906
                                                         4822 126 14305
                                                                         100nF 10% 16V 0603
                                                                                                   3321
                                                                                                          4822 117 12891
                                                                                                                          220k 1% ERJ3\Omega
2534
        4822 126 14305
                       100nF 10% 16V 0603
                                                 2907
                                                         5322 126 11583
                                                                         10nF 10% 50V 0603
                                                                                                   3325
                                                                                                          4822 117 12891
                                                                                                                          220k 1% ERJ3Ω
        4822 124 11947
                       10uF 20% 16V
2535
                                                 2908
                                                         4822 126 11669
                                                                        27pF
                                                                                                  3326
                                                                                                          4822 051 30103
                                                                                                                         10k 5% 0.062W
       3198 017 41050
                       0603 10V 1μF COL R
                                                 2909
                                                         4822 126 14305
                                                                         100nF 10% 16V 0603
2536
                                                                                                          4822 051 30472
                                                                                                                         4k7 5% 0.062W
                                                                                                   3335
        3198 017 41050
                       0603 10V 1μF COL R
2537
                                                 2910
                                                         4822 126 11669
                                                                         27pF
                                                                                                  3336
                                                                                                          4822 051 30103
                                                                                                                         10k 5% 0.062W
2538
        3198 017 41050
                       0603 10V 1μF COL R
                                                         2222 867 15339
                                                                         0603 50V 33P PM5
                                                  2911
                                                                                                   3337
                                                                                                          4822 117 13632
                                                                                                                          100k 1% 0603 0.62W
2539
        4822 124 11947
                       10μF 20% 16V
                                                 2914
                                                         4822 126 14305
                                                                         100nF 10% 16V 0603
                                                                                                   3338
                                                                                                          4822 117 12891
                                                                                                                          220k 1% ERJ3Ω
                       1nF 10% 50V 0603
                                                         4822 126 14305
                                                                         100nF 10% 16V 0603
2540
       5322 126 11578
                                                 2915
                                                                                                  3339
                                                                                                          4822 117 12891
                                                                                                                         220k 1% ERJ3Ω
                       100nF 10% 16V 0603
                                                                         100nF 10% 16V 0603
2541
        4822 126 14305
                                                 2916
                                                         4822 126 14305
                                                                                                   3340
                                                                                                          4822 117 12891
                                                                                                                          220k 1% ERJ3Ω
                       220nF 20% 16V
                                                                                                                          100k 1% 0603 0.62W
2542
        4822 126 13879
                                                 2917
                                                         4822 126 14305
                                                                         100nF 10% 16V 0603
                                                                                                  3402
                                                                                                          4822 117 13632
2544
        4822 126 14305
                       100nF 10% 16V 0603
                                                 2918
                                                         4822 126 14305
                                                                                                          4822 051 30101
                                                                         100nF 10% 16V 0603
                                                                                                   3403
                                                                                                                          100Ω 5% 0.062W
2545
        4822 126 13881
                       470pF 5% 50V
                                                 2950
                                                         4822 126 14305
                                                                         100nF 10% 16V 0603
                                                                                                   3404
                                                                                                          4822 051 30101
                                                                                                                          100Ω 5% 0.062W
                       470pF 5% 50V
2546
       4822 126 13881
                                                 2951
                                                         4822 124 40248
                                                                         10uF 20% 63V
                                                                                                  3405
                                                                                                          4822 051 30759
                                                                                                                         75Ω 5% 0.062W
       3198 017 41050
                       0603 10V 1μF COL R
                                                         4822 126 14238
                                                                        0603 50V 2N2 COL R
2549
                                                 2952
                                                                                                   3406
                                                                                                          4822 051 30759
                                                                                                                          75Ω 5% 0.062W
                       0603 10V 1µF COL R
2550
        3198 017 41050
                                                 2953
                                                         4822 126 14238
                                                                         0603 50V 2N2 COL R
                                                                                                  3407
                                                                                                          4822 051 30101
                                                                                                                          100Ω 5% 0.062W
2551
        5322 126 11583
                       10nF 10% 50V 0603
                                                 2954
                                                         4822 126 14508
                                                                        180pF 5% 50V 0603
180pF 5% 50V 0603
                                                                                                   3408
                                                                                                          4822 051 30759
                                                                                                                          75Ω 5% 0.062W
                       10µF 20% 63V
2600
        4822 124 40248
                                                 2955
                                                         4822 126 14508
                                                                                                  3400
                                                                                                          4822 051 30103
                                                                                                                         10k 5% 0.062W
                       10nF 10% 50V 0603
                                                        3198 017 41050
                                                                        0603 10V 1μF COL R
2601
       5322 126 11583
                                                 2956
                                                                                                  3410
                                                                                                          2322 574 10402
                                                                                                                         VDR 0805 1M A/6V4 MAX
        4822 124 40248
                       10μF 20% 63V
                                                         3198 017 41050
                                                                        0603 10V 1μF COL R
2602
                                                 2957
                                                                                                                          21VR
        4822 126 14305
                       100nF 10% 16V 0603
                                                         4822 124 11947
2603
                                                 2970
                                                                         10μF 20% 16V
                                                                                                          4822 117 13632
                                                                                                                         100k 1% 0603 0.62W
                                                                        100μF 20% 25V
100nF 10% 16V 0603
                                                                                                                         10k 5% 0.062W
2604
       5322 126 11583
                       10nF 10% 50V 0603
                                                 2980
                                                         4822 124 40207
                                                                                                  3412
                                                                                                          4822 051 30103
                       10uF 20% 63V
2605
        4822 124 40248
                                                 2981
                                                         4822 126 14305
                                                                                                  3413
                                                                                                          4822 051 30103
                                                                                                                         10k 5% 0.062W
       5322 126 11583
                       10nF 10% 50V 0603
                                                         4822 124 40207
2606
                                                 2982
                                                                         100uF 20% 25V
                                                                                                  3414
                                                                                                          4822 051 30103
                                                                                                                         10k 5% 0.062W
2607
        4822 126 14225
                       56pF 5% 50V 0603
                                                 2983
                                                        5322 126 11583
                                                                         10nF 10% 50V 0603
                                                                                                  3415
                                                                                                          4822 117 13632
                                                                                                                         100k 1% 0603 0.62W
        4822 124 40248
                       10μF 20% 63V
                                                         3198 016 31020
2608
                                                 2984
                                                                        0603 25V 1nF
                                                                                                   3416
                                                                                                          2322 574 10402
                                                                                                                          VDR 0805 1M A/6V4 MAX
2609
        4822 126 14225
                       56pF 5% 50V 0603
                                                 2990
                                                         4822 126 14305
                                                                         100nF 10% 16V 0603
                       10nF 10% 50V 0603
                                                                        47µF 20% 25V
2610
       5322 126 11583
                                                 2991
                                                        4822 124 40433
                                                                                                  3417
                                                                                                          4822 117 13632
                                                                                                                         100k 1% 0603 0.62W
        4822 124 40769
                       4.7μF 20% 100V
                                                         4822 126 14305
2612
                                                 2992
                                                                        100nF 10% 16V 0603
                                                                                                  3418
                                                                                                          4822 117 13632
                                                                                                                         100k 1% 0603 0.62W
2614
       3198 017 41050
                       0603 10V 1μF COL R
                                                 2993
                                                         4822 126 14305
                                                                         100nF 10% 16V 0603
                                                                                                  3419
                                                                                                          4822 117 13632
                                                                                                                          100k 1% 0603 0.62W
2614
       3198 030 82280
                       EL SM 50V 2U2 PM20 COL
                                                 2994
                                                        4822 126 14305
                                                                        100nF 10% 16V 0603
                                                                                                   3423
                                                                                                          4822 117 12864
                                                                                                                         82k 5% O.6W
                                                 2995
                                                        4822 122 33761
                                                                        22pF 5% 50V
                                                                                                  3424
                                                                                                          4822 051 30474
                                                                                                                         470k 5% 0.062W
2615
       3198 017 41050 0603 10V 1µF COL R
                                                        4822 122 33761 22pF 5% 50V
                                                 2996
                                                                                                  3425
                                                                                                          4822 051 30474
                                                                                                                         470k 5% 0.062W
2615
       3198 030 82280 EL SM 50V 2U2 PM20 COL
                                                                                                  3426
                                                                                                          4822 051 30474
                                                                                                                         470k 5% 0.062W
                                                                                                  3428
                                                                                                          4822 051 30101
                                                                                                                          100Ω 5% 0.062W
                                                 —
2618
       3198 017 41050
                       0603 10V 1μF COL R
                                                                                                  3429
                                                                                                          4822 051 30561
                                                                                                                          560Ω 5% 0.062W
       3198 017 41050 0603 10V 1µF COLB
2619
                                                                                                  3431
                                                                                                          4822 051 30472
                                                                                                                          4k7 5% O.062W
                                                 3000
                                                        4822 051 30472 4k7 5% 0.062W
       3198 016 33380
                      0603 50V 3P3 COL
2620
                                                                                                                         75Ω 5% 0.062W
68Ω 5% 0.063W 0603
                                                                                                  3432
                                                                                                          4822 051 30759
                                                         4822 117 13632
                                                 3001
                                                                        100k 1% 0603 0.62W
2621
       3198 016 33380
                       0603 50V 3P3 COL
                                                                                                  3433
                                                                                                          4822 051 30689
                                                 3002
                                                        4822 051 30103
                                                                        10k 5% 0.062W
       4822 124 40248
                       10μF 20% 63V
2622
                                                                                                                          RC21 RST SM
                                                 3003
                                                        4822 051 30103
                                                                        10k 5% 0.062W
                       10nF 10% 50V 0603
0603 10V 1μF COL R
2623
       5322 126 11583
                                                                                                  3434
                                                                                                          4822 117 12864
                                                                                                                         82k 5% O.6W
                                                 3004
                                                        4822 051 30103
                                                                        10k 5% 0.062W
2624
       3198 017 41050
                                                                                                  3435
                                                                                                          4822 117 13632
                                                                                                                         100k 1% 0603 0.62W
                                                 3005
                                                         4822 051 30472
                                                                         4k7 5% 0.062W
       3198 030 82280
                       EL SM 50V 2U2 PM20 COL
2624
                                                                                                  3436
                                                                                                          4822 051 30759
                                                                                                                         75Ω 5% 0.062W
                                                 3005
                                                        5322 117 13026
                                                                        4k7 1% 0.063W 0603
                                                                                                  3437
                                                                                                          4822 117 12864
                                                                                                                         82k 5% O.6W
                                                                        RC22H
2625
       3198 017 41050 0603 10V 1µF COL R
                                                                                                  3438
                                                                                                          4822 117 13632
                                                                                                                          100k 1% 0603 0.62W
                                                 3006
                                                        4822 051 30472
                                                                        4k7 5% 0.062W
       3198 030 82280 EL SM 50V 2U2 PM20 COL
2625
                                                                                                  3439
                                                                                                          4822 051 30471
                                                                                                                          470Ω 5% 0.062W
                                                 3006
                                                        5322 117 13026
                                                                        4k7 1% 0.063W 0603
                                                                                                  3440
                                                                                                          4822 051 30101
                                                                                                                         100Ω 5% 0.062W
                                                                         RC22H
2626
       3198\,017\,41050\,\,0603\,10V\,1\mu F\,COL\,R
                                                                                                  3441
                                                                                                                         100k 1% 0603 0.62W
                                                                                                          4822 117 13632
                                                 3007
                                                        4822 051 30472
                                                                        4k7 5% 0.062W
       3198 017 41050 0603 10V 1µF COL R
                                                                                                                         4k7 5% O.062W
2627
                                                                                                  3442
                                                                                                          4822 051 30472
                                                 3007
                                                        5322 117 13026
                                                                        4k7 1% 0.063W 0603
2700
       4822 124 81151 22uF 50V
                                                                                                          4822 051 30479
                                                                                                  3443
                                                                                                                         47Ω 5% O.062W
                                                                         RC22H
       5322 122 33861
                       120nF 10% 50V
2701
                                                                                                  3445
                                                                                                          4822 051 30471
                                                                                                                         470Ω 5% 0.062W
                                                 3008
                                                        2120 108 94006
                                                                        RST SM 0603 ERJ3G 1Ω5
                       220pF 5% 50V
2702
       4822 126 13883
                                                                                                  3446
                                                                                                          4822 051 30101
                                                                                                                         100Ω 5% 0.062W
2703
       5322 124 41379
                       2.2µF 20% 50V
                                                                                                  3450
                                                                                                                         100k 1% 0603 0.62W
                                                                                                          4822 117 13632
                      470pF 5% 50V
100nF 10% 16V 0603
                                                 3009
                                                        2322 704 65102
                                                                        RST SM 0603 RC22H 5k1
       4822 126 13881
2704
                                                                                                  3451
                                                                                                          4822 051 30472
                                                                                                                         4k7 5% O.062W
                                                                        PM1
2705
       4822 126 14305
                                                                                                  3455
                                                                                                          4822 117 13632
                                                                                                                          100k 1% 0603 0.62W
                                                 3009
                                                        4822 051 30332
                                                                        3k3 5% 0.062W
                       100nF 10% 16V 0603
2706
       4822 126 14305
                                                                                                  3458
                                                                                                          4822 051 30152
                                                                                                                         1k5 5% O.062W
                                                 3010
                                                        2120 108 94006
                                                                        RST SM 0603 ERJ3G 1Ω5
2707
       5322 126 11583
                       10nF 10% 50V 0603
                                                                                                  3459
                                                                                                         4822 051 30472
                                                                                                                         4k7 5% O.062W
                                                                        PM<sub>5</sub>
2708
        4822 124 40248
                       10μF 20% 63V
                                                                                                  3460
                                                                                                         4822 051 30471
                                                                                                                         470Ω 5% 0.062W
                                                 3011
                                                        4822 051 30472
                                                                        4k7 5% 0.062W
2709
       4822 126 13879
                       220nF 20% 16V
                                                                                                  3461
                                                                                                          4822 051 30472
                                                                                                                         4k7 5% O.062W
                                                 3011
                                                        5322 117 13026
                                                                        4k7 1% 0.063W 0603
2710
       2020 552 94523
                       0603 50V 8P2 PM0P5
                                                                                                  3462
                                                                                                         2322 574 10402
                                                                                                                         VDR 0805 1M A/6V4 MAX
                                                                        RC22H
                       1nF 10% 50V 0603
       5322 126 11578
2711
                                                                                                                         21VR
                                                 3012
                                                        4822 051 30472
                                                                        4k7 5% 0.062W
2712
       5322 126 11578
                       1nF 10% 50V 0603
                                                                                                  3463
                                                                                                         4822 117 13632
                                                                                                                         100k 1% 0603 0.62W
                                                                        4k7 1% 0.063W 0603
                                                 3012
                                                        5322 117 13026
2713
       3198 024 44730
                       47nF 50V 0603
                                                                                                                         100k 1% 0603 0.62W
                                                                                                  3464
                                                                                                         4822 117 13632
                                                                        RC22H
                      2.2μF 20% 50V
2714
       4822 124 22652
                                                                                                  3465
                                                                                                         2322 574 10402
                                                                                                                         VDR 0805 1M A/6V4 MAX
                                                 3013
                                                        4822 117 12139
                                                                        22Ω 5% 0.062W
2715
       5322 126 11578
                      1nF 10% 50V 0603
                                                                                                                         21VR
                                                 3014
                                                        4822 117 12139
                                                                        22Ω 5% 0.062W
       4822 124 41584
                      100uF 20% 10V
                                                                                                         4822 051 30471
2716
                                                                                                  3466
                                                                                                                         470Ω 5% 0.062W
                                                 3015
                                                        4822 117 12139
                                                                        22Ω 5% 0.062W
       4822 124 22652
                      2.2µF 20% 50V
2717
                                                                                                  3467
                                                                                                         4822 051 30472
                                                                                                                         4k7 5% O.062W
                                                 3016
                                                        4822 117 12139
                                                                        22Ω 5% 0.062W
       4822 124 40433
2718
                       47μF 20% 25V
                                                                                                  3468
                                                                                                         2322 574 10402
                                                                                                                         VDR 080.5 1M A/6V4 MAX
                                                 3017
                                                        4822 051 30472
                                                                        4k7 5% 0.062W
2800
       3198 017 44740 0603 10V 470nF COL
                                                                                                                         21VR
                                                 3017
                                                        5322 117 13026
                                                                        4k7 1% 0.063W 0603
2801
       4822 126 14238
                      0603 50V 2N2 COL B
                                                                                                  3469
                                                                                                         4822 117 13632
                                                                                                                         100k 1% 0603 0.62W
                                                                        RC22H
       4822 126 13482
                       470nF 80/20% 16V
2802
                                                                                                  3470
                                                                                                         4822 117 13632
                                                                                                                         100k 1% 0603 0.62W
                                                 3018
                                                        2120 108 94006
                                                                        RST SM 0603 ERJ3G 1\Omega5
                       220pF 5% 50V
2803
       4822 126 13883
                                                                                                  3471
                                                                                                         2322 574 10402
                                                                                                                         VDR 080 5 1M A/6V4 MAX
                                                                        PM<sub>5</sub>
       3198 017 44740
                       0603 10V 470nF COL
2806
                                                                                                                         21VR
                                                 3019
                                                        2120 108 94006
                                                                        RST SM 0603 ERJ3G 1\Omega5
2807
       4822 126 13482
                       470nF 80/20% 16V
                                                                                                         4822 051 30471
                                                                                                                         470Ω 5% 0.062W
                                                                        PM5
2810
       5322 126 11578
                       1nF 10% 50V 0603
                                                                                                         4822 051 30689
                                                                                                                         68Ω 5% O.063W 0603
                                                                                                  3473
                                                 3020
                                                        4822 051 30123
                                                                        12k 5% 0.062W
       4822 124 11968
                      220mF 20% 5.5V
2811
                                                                                                                         RC21 RS T SM
                                                 3020
                                                        5322 117 13028
                                                                        12k 1% 0.063W 0603
       4822 126 14305
                       100nF 10% 16V 0603
2812
                                                                                                  3474
                                                                                                         4822 051 30471
                                                                                                                         470Ω 5% 0.062W
                                                                        RC22H
       5322 126 11583
                       10nF 10% 50V 0603
                                                                                                  3475
                                                                                                         4822 051 30102
                                                                                                                         1k 5% (C)62W
                                                 3021
                                                        4822 051 30123
                                                                        12k 5% 0.062W
                       18pF 5% 50V 0603
2815
       4822 126 14507
                                                                                                  3476
                                                                                                         5322 117 13068
                                                                                                                         82Ω 1% Ø.063W 0603
                                                 3021
                                                        5322 117 13028
                                                                        12k 1% 0.063W 0603
       3198 017 41050
2816
                      0603 10V 1uF COL R
                                                                                                                         RC22H
                                                                        RC22H
       5322 126 11578
                      1nF 10% 50V 0603
2817
                                                                                                  3477
                                                                                                         4822 117 12925
                                                                                                                         47k 1%D .063W 0603
                                                 3022
                                                        2322 704 65102
                                                                       RST SM 0603 RC22H 5k1
2818
       5322 126 11583
                      10nF 10% 50V 0603
                                                                                                  3478
                                                                                                         4822 051 30759
                                                                                                                         75Ω 5% Ø.062W
                                                                        PM<sub>1</sub>
2819
       3198 017 44740
                      0603 10V 470nF COL
                                                                                                  3479
                                                                                                         4822 051 30472
                                                                                                                         4k7 5%) -062W
                                                3022
                                                        4822 051 30332 3k3 5% 0.062W
2820
       3198 017 44740 0603 10V 470nF COL
                                                                                                  3480
                                                                                                         4822 051 30759
                                                                                                                         75Ω 5% Ø.062W
                                                3023
                                                        4822 117 12925
                                                                       47k 1% 0.063W 0603
2821
       2020 552 96305 4U7 20% 10V
                                                                                                  3481
                                                                                                         4822 051 30759
                                                                                                                         75Ω 5%Ø.062W
                                                3024
                                                        4822 117 12925
                                                                        47k 1% 0.063W 0603
       2020 552 96305 4U7 20% 10V
2822
                                                                                                  3482
                                                                                                         4822 051 30101
                                                                                                                         100Ω 5% 0.062W
                                                 3025
                                                        4822 117 12139
                                                                        22\Omega 5% 0.062W
       4822 126 14305 100nF 10% 16V 0603
2823
                                                                                                                         68Ω 5%C .063W 0603
                                                                                                  3483
                                                                                                         4822 051 30689
                                                3026
                                                        4822 117 12139
                                                                       22Ω 5% 0.062W
2831
       4822 124 40433
                      47μF 20% 25V
                                                                                                                         RC21 FS T SM
                                                3027
                                                        4822 117 12139
                                                                       22Ω 5% 0.062W
       4822 126 14305 100nF 10% 16V 0603
2832
                                                                                                  3484
                                                                                                         4822 051 30759
                                                                                                                         75Ω 5% →.062W
                                                3028
                                                        4822 117 13608
                                                                        4.7Ω 5% 0603 0.0016W
       5322 126 11583
                      10nF 10% 50V 0603
```

4822 051 30008 0Ω jumper

3029

2900

2901

4822 124 40433 47μF 20% 25V

GB 310 1	DVDR100	0 /0x1 /691	Spare Parts List
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3487	4822 051 30101	100Ω 5% 0.062W	3708	4822 051 30101	100Ω 5% 0.062W	3872	4822 051 30103	10k 5% 0.062W
3488		100Ω 5% 0.062W	3709		18k 5% 0.062W	3873		10k 5% 0.062W
3489	4822 051 30103	10k 5% 0.062W	3710		100Ω 5% 0.062W	3874		12k 5% 0.062W
3490	4822 051 30471	470Ω 5% 0.062W	3711	4822 051 30008		3875	4822 051 30102	
3492		100k 1% 0603 0.62W	3712	4822 051 30222	2k2 5% 0.062W	3876		330Ω 5% 0.062W
3494		75Ω 5% 0.062W	3713		6k8 5% 0.062W	3877		100Ω 5% 0.062W
3495		2k2 5% 0.062W	3714	4822 051 30472	4k7 5% 0.062W	3878	4822 051 30101	100Ω 5% 0.062W
3497		100Ω 5% 0.062W	3715		100Ω 5% 0.062W	3879	4822 051 30103	10k 5% 0.062W
3499		330Ω 5% 0.062W	3716		100Ω 5% 0.062W	3880	4822 051 30103	10k 5% 0.062W
3500		2k7 5% 0.062W	3717	4822 051 30102		3881		10k 5% 0.062W
3501		2k7 5% 0.062W	3718		4k7 5% 0.062W	3882		100k 1% 0603 0.62W
3503		220Ω 5% 0.062W	3719		4k7 5% 0.062W	3883		330Ω 5% 0.062W
3504		2k2 5% 0.062W	3720		100Ω 5% 0.062W	3885		2k2 5% 0.062W
3505		2k2 5% 0.062W	3721		270Ω 5% 0.062W	3886		47Ω 5% 0.062W
3506		220Ω 5% 0.062W	3722		3k3 5% 0.062W	3887		470k 5% 0.062W
3515 3516		100k 1% 0603 0.62W	3723		100k 1% 0603 0.62W	3888		22k 5% 0.062W
3517		470Ω 5% 0.062W VDR 0805 1M A/6V4 MAX	3724 3725		680Ω 5% 0.062W	3889	4822 051 30102	
3317	2322 374 10402	21VR	3726		4k7 5% 0.062W 5k6 5% 0.063W 0603 RC21	3890		100Ω 5% 0.062W
3518	4822 051 30472	4k7 5% 0.062W	13/20	4022 031 30302	RST SM	3892 3893		10k 5% 0.062W 10k 5% 0.062W
3519		100k 1% 0603 0.62W	3727	4822 051 30272	2k7 5% 0.062W	3896		10k 5% 0.062W
3520		VDR 0805 1M A/6V4 MAX	3728		330Ω 5% 0.062W	3898		10k 5% 0.062W
		21VR	3729		5k6 5% 0.063W 0603 RC21	3899		10k 5% 0.062W
3521	4822 051 30102				RST SM	3900		10k 5% 0.062W
3522		470Ω 5% 0.062W	3730	4822 051 30562	5k6 5% 0.063W 0603 RC21	3901		47k 1% 0.063W 0603
3523		VDR 0805 1M A/6V4 MAX	1		RST SM	3902		4k7 5% 0.062W
		21VR	3800	4822 051 30103	10k 5% 0.062W	3903	4822 051 30102	
3524	4822 051 30101	100Ω 5% 0.062W	3801		27k 5% 0.062W	3904	4822 051 30102	
3525		100Ω 5% 0.062W	3803		6k8 5% 0.062W	3905	4822 051 30102	
3526		100k 1% 0603 0.62W	3804		2k2 5% 0.062W	3906	4822 051 30333	33k 5% 0.062W
3527	4822 051 30472		3805		2k2 5% 0.062W	3907		100Ω 5% 0.062W
3528		470Ω 5% 0.062W	3807	5322 117 13052	2k7 1% 0.063W 0603	3908		100Ω 5% 0.062W
3529		100k 1% 0603 0.62W		1000 051 5555	RC22H	3909		100Ω 5% 0.062W
3530	2322 5/4 10402	VDR 0805 1M A/6V4 MAX	3808		33k 5% 0.062W	3910	4822 051 30102	
2524	4000 0E4 00474	21VR	3809		10k 5% 0.062W	3911		4k7 5% 0.062W
3531 3532		470Ω 5% 0.062W 470Ω 5% 0.062W	3810		100k 1% 0603 0.62W	3912		10k 5% 0.062W
3532		470Ω 5% 0.062W 47k 1% 0.063W 0603	3811 3812		4k7 5% 0.062W 220Ω 5% 0.062W	3913		100k 1% 0603 0.62W
3534		100Ω 5% 0.062W	3813			3914		100Ω 5% 0.062W
3535		470Ω 5% 0.062W	3815		680k 5% 0.062W 1k0 1% 0.063W 0603	3915 3918		100Ω 5% 0.062W
3536		68Ω 5% 0.063W 0603	13013	3322 117 13010	RC22H	3919		10k 5% 0.062W
0000	1022 001 00000	RC21 RST SM	3816	4822 051 30101	100Ω 5% 0.062W	3920		10k 5% 0.062W 220k 1% ERJ3Ω
3537	4822 051 30689	68Ω 5% 0.063W 0603	3817	4822 051 30102		3925		22Ω 5% 0.062W
		RC21 RST SM	3818		100Ω 5% 0.062W	3943		10k 5% 0.062W
3538	4822 051 30102		3819		100Ω 5% 0.062W	3944		220k 1% ERJ3Ω
3539	4822 051 30102		3820	4822 051 30472		3947		10k 5% 0.062W
3540		82Ω 1% 0.063W 0603	3821	4822 051 30103		3948	4822 051 30103	
		RC22H	3822		100k 1% 0603 0.62W	3950		4k7 5% 0.062W
3541	4822 051 30471	470Ω 5% 0.062W	3823	4822 051 30103		3951		100k 1% 0603 0.62W
3542		470Ω 5% 0.062W	3824	4822 051 30103		3952		22k 5% 0.062W
3543		100Ω 5% 0.062W	3825	4822 051 30103	10k 5% 0.062W	3953		15k 5% 0.062W
3544	4822 051 30472		3829		2k7 1% 0.063W 0603	3954	4822 051 30472	
3545	4822 051 30689	68Ω 5% 0.063W 0603			RC22H	3955		4k7 5% 0.062W
		RC21 RST SM	3830	4822 051 30472		3956		2k2 5% 0.062W
3546	4822 051 30102		3831	4822 051 30103		3957		2k2 5% 0.062W
3547		150Ω 5% 0.062W	3832		100k 1% 0603 0.62W	3958	4822 051 30472	
3548		100Ω 5% 0.062W	3833	4822 051 30222		3959	3198 021 31060	RST SM 0603 10M
3549	4822 051 30689	68Ω 5% 0.063W 0603	3834	4822 051 30222				PM5COL R
2550	4900 054 00400	RC21 RST SM	3835	4822 051 30103		3960	3198 021 31060	RST SM 0603 10M
3550 3551	4822 051 30102		3837		100k 1% 0603 0.62W	000:	4000	PM5COL R
3551 3552		100Ω 5% 0.062W	3838	4822 051 30472		3961	4822 051 30333	
عرون	7022 USI 30009	68Ω 5% 0.063W 0603 RC21 RST SM	3839 3840	4822 051 30103	10K 5% 0.062W 100Ω 5% 0.062W	3962	4822 051 30333	
3553	4822 051 30102		3841		100Ω 5% 0.062W 100Ω 5% 0.062W	3963 3964		33k 5% 0.062W
3554	4822 051 30759		3842		680k 5% 0.062W	3964	4822 051 30333 4822 051 30333	
3555	4822 051 30103		3843	4822 051 30103		3966	4822 051 30333 4822 051 30333	
3556		47k 1% 0.063W 0603	3844	4822 051 30102		3967		RST SM 603 RC22H 5Ω6
3557		47k 1% 0.063W 0603	3845	4822 051 30472			, 0 , 00000	PM1
3558	4822 051 30223		3846	4822 051 30102		3967	4822 051 30109	10Ω 5% 0.062W
3559		3k9 5% 0.063W 0603	3847	4822 051 30332		3968		RST SM 603 RC22H 5Ω6
3560	4822 117 12891	220k 1% ERJ3Ω	3848		47k 1% 0.063W 0603			PM1
3561	4822 051 30332	3k3 5% 0.062W	3849	4822 051 30103	10k 5% 0.062W	3968	4822 051 30109	10Ω 5% 0.062W
3562		100Ω 5% 0.062W	3850	4822 051 30472	4k7 5% 0.062W	3969		RST SM 603 RC22H 5Ω6
3563		100Ω 5% 0.062W	3851	4822 051 30103	10k 5% 0.062W			PM1
3567	4822 051 30103		3852		100k 1% 0603 0.62W	3969	4822 051 30109	10Ω 5% 0.062W
3568	4822 051 30472		3853		100k 1% 0603 0.62W	3970	4822 117 12891	220k 1% ERJ3Ω
3570		100k 1% 0603 0.62W	3854	5322 117 13018	1k0 1% 0.063W 0603	3971		33k 1% 0.063W 0603
3600	4822 051 30103			1000	RC22H			RC22H
3601		100Ω 5% 0.062W	3855	4822 051 30472		3972		470Ω 5% 0.062W
3602 3603	4822 051 30472		3856		100k 1% 0603 0.62W	3973	4822 051 30102	
3604		100Ω 5% 0.062W	3857	4822 051 30222		3975	4822 051 30563	
3605	4822 O51 30102 4822 O51 30102		3858		100k 1% 0603 0.62W	3976	4822 051 30393	
3606	4822 O51 30102 4822 O51 30102		3859 3860		100k 1% 0603 0.62W	3976	4822 117 12864	
3607	4822 O51 30102		3861	4822 051 30682 4822 051 30103		3977	4822 051 30223	
3700	4822 O51 30333		3862	4822 051 30103		3978	2322 /04 65608	RST SM 603 RC22H 5Ω6
3701		680Ω 5% 0.062W	3863		22K 5% 0.062W 100Ω 5% 0.062W	3978	4822 OE1 20102	PM1
3702		5k6 5% 0.063W 0603 RC21	3864		100Ω 5% 0.062W	3978	4822 051 30109 4822 051 30102	
	001 00002	RST SM	3865		100Ω 5% 0.062W	3980	4822 051 30102	
3703	4822 O51 30154		3866		47k 1% 0.063W 0603	3981	4822 051 30353	
3704	4822 O51 30472		3867		100Ω 5% 0.062W	3982	4822 051 30183	
3705	4822 O51 30183	18k 5% 0.062W	3868	4822 051 30103		3983	4822 051 30563	
3706	4822 O51 30331	330Ω 5% 0.062W	3869	4822 051 30332	3k3 5% 0.062W	3984	4822 051 30102	
3707	4822 1 00 12158	22k 30%	3870		100Ω 5% 0.062W		· · · · -	1
					•			

3985	4822 051 30562	5k6 5% 0.063W 0603 RC21	6507	9322 129 38685	DIO REG SM BZM55-C6V8	7815	4822 209 16954	ST24E16M6
0000	4000 054 00400	RST SM	0500	0000 400 00005	(TEG0)	7816	3198 010 42310	
3986 3987	4822 051 30103	10k 5% 0.062W 1k 5% 0.062W	6508	9322 129 30000	DIO REG SM BZM55-C6V8 (TEG0)	7817 7900	3198 010 42310 4822 209 16778	TL7705ACD1013TRA
3988	4822 051 30273	27k 5% 0.062W	6509	9322 150 38685	DIO SÍG SM	7901	4822 209 73852	PMBT2369
3989	4822 051 30103		0000	4000 400 00757	BAS385(VISH)R	7902	9340 560 36235	FETSIG SM BSH111
3990 3991		47k 1% 0.063W 0603 47k 1% 0.063W 0603	6600 6700	4822 130 83757 4822 130 11525		7906	9322 152 30668	(PHSE) R ICSM M29F800AT-
3992		47k 1% 0.063W 0603	6701	4822 130 11525		1,000	JOEE 132 00000	70N1(ST00)
3993		100Ω 5% 0.062W	6702	4822 130 11525		7907	9322 161 94668	IC SM CY62128-
3994 3995	4822 051 30101 4822 051 30103	100Ω 5% 0.062W 10k 5% 0.062W	6703 6801	4822 130 83757 9322 150 38685		7909	4822 130 61553	70SC(CYPR)R DTC124FII
3996		10Ω 5% 0.062W	"	100 00000	BAS385(VISH)R	7950	4822 209 60177	
3997	4822 051 30109	10Ω 5% 0.062W	6802	4822 130 83757		7951	3198 010 42310	
-			6803 6805	4822 130 83757 9322 150 38685		7952 7970	3198 010 42310 4822 209 63709	
			l		BAS385(VISH)R	7971	4822 130 44283	
5000	4822 157 11074	100μΗ	6807 6970	4822 130 83757		7972	3198 010 42310	
5001	4822 157 11074		6971	4822 130 83757 4822 130 83757		7974 7975	3198 010 42310 9340 560 36235	FETSIG SM BSH111
5002 5003		EL0305RA-100J BLM11P600SPT	6972	4822 130 83757		ł		(PHSE) R
5004		BLM11P600SPT				7990	4822 209 17505	STV5348D
5009	4822 157 11775		B			1		
5400 5430		EL0305RA-100J EL0305RA-100J	7000	5322 130 42756	BC857C	DIVI	O PWB	
5470		TRANSFORMER 6RG	7001	4822 209 17423				
5000	4000 457 44000	(SAGA) B	7002	4822 209 62312		Vario	us	
5600 5601		EL0305RA-100J IND FXD EL0305 S 100U	7004	935261537118	IC SM UDA1360TS/N1 (PHSE) R	1101	2422 025 17106	CON BM H 4P F 0.8 IEEE R
		PM5 A	7321	9322 147 95668	FET SIG SM 2SK2839	1102		RES XTL SM 24M576 12P
5602		EL0305RA-100J	7000	0000 447 05000	(TOSJ)	1000	0400 540 04450	CX-11F R
5700 5701	4822 157 11074 4822 157 11775		7323	3322 147 95668	FET SIG SM 2SK2839 (TOSJ)	1200	2422 543 01159	RES XTL SM 11M0592 20P DSX840
5702	2422 549 44162	IND VAR 7MM Y 77M8 B	7324	4822 130 61553		1500	2422 025 17084	CON BM V 60P F 0.80
5703 5705		IND VAR 7MM Y 77M8 B	7329	3198 010 42310				179161 R
5705 5706	4822 157 11299	EL0305RA-100J 6.8µH 5% 5X3	7330 7331	3198 010 42310 3198 010 42310				
5707	4822 157 11302	EL0305RA-150J	7332	4822 209 33665	L78M08CV	⊣⊢		
5901 5902	4822 157 11499 4822 157 11074	BLM11P600SPT	7400	9322 143 92668	IC SM BA7652AF (RHM0) R	2146	4822 126 14305	100nF 1 0% 16V 0603
5903		BLM11P600SPT	7401	9322 143 92668	IC SM BA7652AF (RHM0)	2147		100nF 1 0% 16V 0603
5904	4822 157 11499	BLM11P600SPT	l		R	2148 2149		100nF 1 0% 16V 0603 100nF 1 0% 16V 0603
5990 5991	4822 157 11299 4822 157 11074	EL0305RA-100J	7430 7431	9965 000 04716 4822 130 42804	IC BA7660FS-E2 BC817-25	2150		100nF 1 0% 16V 0603
	4022 107 11074	Τοσμιτ	7433	4822 130 42804		2151		100nF 10% 16V 0603
→ -			7460	4822 130 42804		2152 2153		100nF 10% 16V 0603 100nF 10% 16V 0603
			7461 7462	4822 130 42804 3198 010 42310		2154	4822 126 14305	100nF 10% 16V 0603
6000 6402	4822 130 83757	BAS216 DIO REG SM DF3A6.8FU	7463	4822 130 42804		2155 2156		100nF10% 16V 0603
0402	9322 140 0 1003	TOSJ	7464	3198 010 42310 4822 130 42804		2157		100nF 10% 16V 0603 100nF 10% 16V 0603
6403	9322 146 61685	DIO REG SM DF3A6.8FU	7466 7470	5322 209 11517		2158	3198 017 41050	0603 10V 1μF COL R
6405	9322 146 61685	TOSJ DIO REG SM DF3A6.8FU	7500	5322 130 42756	BC857C	2159 2160		0603 10 V 1μF COL R 0603 10 V 1μF COL R
0403		TOSJ	7501 7505	5322 130 42756 4822 130 42804		2161		250V 1n F PM10 R
6430	9322 146 61685	DIO REG SM DF3A6.8FU	7506	4822 130 42804		2162		250V 1n F PM10 R
6431	9322 146 61685	TOSJ DIO REG SM DF3A6.8FU	7507		IC SM STV6410AD (ST00)	2163 2164		270pF 5% 50V 0603 250V 1nF PM10 R
		TOSJ	7508	3198 010 42310	Y BC847RW	2165		250V 1n F PM10 R
6432	9322 146 61685	DIO REG SM DF3A6.8FU	7509	3198 010 42310		2166		250V 1nF PM10 R
6439	9322 146 61685	TOSJ DIO REG SM DF3A6.8FU	7510	3198 010 42310		2167 2168		250V 1nF PM10 R 250V 1nF PM10 R
		TOSJ	751 1 7512	4822 130 42804 3198 010 42310		2169	2020 557 90731	250V 1n F PM10 R
6440	9322 146 61685	DIO REG SM DF3A6.8FU TOSJ	7513	3198 010 42310	BC847BW	2170 2171	4822 126 11663	
6460	9322 129 38685	DIO REG SM BZM55-C6V8	7514 7515	5322 130 42756	-	2172	4822 126 11663 4822 126 14305	100nF 10% 16V 0603
0404	0000 400 4000=	(TEG0)	7516	4822 130 42804 3198 010 42310		2173	4822 124 23002	10μF 16 V
6461	9322 129 42685	DIO REG SM BZM55-C15 (TEG0) R	7517	5322 130 42756	BC857C	2174 2175	4822 126 14305 4822 124 23002	100nF 10% 16V 0603
6462	9322 129 38685	DIO REG SM BZM55-C6V8	7600	9322 167 63668	IC SM MSP3415G-QG-B8 (MIAS) R	2176		100nF 10% 16V 0603
0.400	0000 400 0000	(TEG0)	7700	4822 130 61553		2177	4822 126 14305	100nF 10% 16V 0603
6463	9322 129 38685	DIO REG SM BZM55-C6V8 (TEG0)	7701	4822 130 61553	DTC124EU	2178 2179		100nF 10% 16V 0603 100nF 10% 16V 0603
6464	9322 129 38685	DIO RÉG SM BZM55-C6V8	7702 7703	4822 130 61553 9352 606 11118	DTC124EU IC SM TDA9818T/	2180	2020 557 90732	250V 4N 7 PM10 R
CACE	0222 120 20605	(TEG0)	1.00	0002 000 11110	V1(PHSE) R	2181	4822 124 12095	
6465	9322 129 30003	DIO REG SM BZM55-C6V8 (TEG0)	7704	5322 130 42756		2182 2183	4822 124 23002 4822 126 14305	100nF 10% 16V 0603
6466	9322 146 61685	DIO REG SM DF3A6.8FU	7705 7706	5322 130 42755 5322 130 42756		2184	4822 126 14305	100nF 10% 16V 0603
0.400	4000 400 00757	TOSJ	7707	3198 010 42310		2185		100nF 10% 16V 0603
6468 6501	4822 130 83757 9322 129 42685	DIO REG SM BZM55-C15	7708	4822 130 61553		2186 2187		100nF 10% 16V 0603 100nF 10% 16V 0603
0001	3022 123 1233	(TEG0) R	7709 7800	3198 010 42310	IC SM TL074CD (ST00) R	2188		250V 4N 7 PM10 R
6502	9322 129 38685	DIO RÉG SM BZM55-C6V8	7801	3198 010 42310		2189	2020 557 90732	250V 417 PM10 R
6503	9322 129 38685	(TEG0) DIO REG SM BZM55-C6V8	7803	4822 209 16884		2190 2200	2020 557 90719 4822 126 11663	1206 B 2 50V 47nF PM10 R
5000		(TEG0)	7804 7805	5322 130 42756		2201		100nF 107% 16V 0603
6504	9322 129 38685	DIO RÉG SM BZM55-C6V8	7806	3198 010 42310 5322 130 42756		2202	4822 126 14305	100nF 15 % 16V 0603
	0022 120 00000					2203	4822 126 14305	100nF 101% 16V 0603
		(TEG0) DIO REG SM DF3A6.8FU	7807	4822 130 60854		2204	4822 126 1/205	100nF 103% 16V 0600
6505	9322 146 61685	DIO RÉG SM DF3A6.8FU TOSJ	7809	3198 010 42310	BC847BW	2204 2205	4822 126 14305 4822 126 11663	100nF 107% 16V 0603 12pF
	9322 146 61685	DIO RÉG SM DF3A6.8FU TOSJ DIO REG SM BZM55-C6V8			BC847BW BA7046F	2205 2206	4822 126 11663 4822 122 31765	12pF 100pF 2⁵⁄₀ 63V
6505	9322 146 61685	DIO RÉG SM DF3A6.8FU TOSJ	7809 7810	3198 010 42310 4822 209 63604	BC847BW BA7046F PCF8593T BC857C	2205	4822 126 11663 4822 122 31765 4822 126 14305	12pF

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200						0.000			
2003 422 129 1405 1006 1006 100 140 140 1001 315 402 201 3003 30 50 50 50 000 W 5 100 400 201 315 400 400 100 100 100 100 100 100 100 100		4822 126 14305	100nF 10% 16V 0603	3148	2322 704 66342	RST SM 0603 RC22H 6k34	-		
2004									
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2507 4822 128 14305 100nF 10% 16V 0603 3305 4822 051 30102 1k 5% 0.062W 4822 128 14305 100nF 10% 16V 0603 3317 4822 051 30102 1k 5% 0.062W 4822 128 14305 100nF 10% 16V 0603 3317 4822 051 30102 1k 5% 0.062W 4822 128 14305 100nF 10% 16V 0603 3314 4822 051 30103 10k 5% 0.062W 4822 128 14305 100nF 10% 16V 0603 3314 4822 051 30103 10k 5% 0.062W 4822 128 14305 100nF 10% 16V 0603 3314 4822 051 30103 10k 5% 0.062W 4822 128 1014 47µF 16V 3316 4822 051 30103 301.5% 0.062W 4822 128 1014 47µF 16V 3316 4822 051 30103 301.5% 0.062W 4822 128 1014 47µF 16V 3316 4822 051 30133 301.5% 0.062W 4822 128 1014 47µF 16V 3316 4822 051 30133 301.5% 0.062W 4822 128 10415 47µF 16V 3316 4822 051 30133 301.5% 0.062W 4822 128 14305 10nF 10% 50V 0603 3319 4822 051 30133 301.5% 0.062W 4822 128 14305 100nF 10% 16V 0603 3324 4822 051 30134 4822 128 14305 100nF 10% 16V 0603 3324 4822 051 30134 4822 128 14305 100nF 10% 16V 0603 3324 4822 051 30134 4822 128 14305 100nF 10% 16V 0603 3324 4822 051 30134 4822 128 14305 100nF 10% 16V 0603 3324 4822 051 30134 4822 128 14305 100nF 10% 16V 0603 3324 4822 051 30134 4822 100nF 10% 100nF 10% 16V 0603 3316 4822 128 14305 100nF 10% 16V 0603 3316 4822 051 30133 10k 5% 0.062W 4822 100nF 10% 100nF 10% 16V 0603 3324 4822 100nF 100nF 10% 16V 0603 3324 4822 100nF 100nF 10% 16V 0603 3316 4822 100nF 100nF 10% 100	2418 2419 2420 2421 2500 2501 2502 2503	4822 126 14305 4822 126 14305	100nF 10% 16V 0603 100nF 10% 16V 0603	3198 3199 3201 3214 3216 3224 3300 3301	4822 051 30103 4822 051 30103 4822 051 30479 4822 051 30102 4822 051 30102 4822 051 30331 4822 051 30109 4822 051 30109	10k 5% 0.062W 10k 5% 0.062W 47Ω 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 330Ω 5% 0.062W 10Ω 5% 0.062W 1k 5% 0.062W	7301 7302 7303	9322 166 64668 9322 166 64668 9322 150 51671	IC OTÉ EPC1441 ASSY IC SM CY7C1019BV33- 10VC(CYPR)R IC SM CY7C1019BV33- 10VC(CYPR)R IC SM EPF6024AQC208-3 (ALT0) Y
2507 4822 126 490151 47μF 16V 3306 4822 051 30102 1 k 5% 0.062W 7306 9322 166 64668 IC SM CYTC710198V33-10VC(CYPR)R 2508 4822 126 14305 100nF 10% 16V 0603 3317 4822 051 30103 10k 5% 0.062W 7307 3104 123 96402 IC FLASH CY2071 AUDIO ASSY 2511 4822 124 64051 74 7μF 16V 3316 4822 051 30103 10k 5% 0.062W 7308 3104 123 96402 IC FLASH CY2071 AUDIO ASSY 2512 4822 124 80151 47μF 16V 3316 4822 051 30103 10k 5% 0.062W 7308 3104 123 96402 IC FLASH CY2071 VIDEO ASSY 2516 5322 126 11583 10nF 10% 50V 0603 3317 4822 051 30339 330 5% 0.062W 7402 4822 209 17375 GM71V18163CJ-6 2517 5322 126 11583 10nF 10% 50V 0603 3318 4822 051 30339 330 5% 0.062W 7402 4822 209 17375 GM71V18163CJ-6 2519 4822 124 80151 47μF 16V 3316 4822 051 30339 330 5% 0.062W 3316 4822 051 30339 330 5% 0.062W 2510 4822 126 14305 100nF 10% 50V 0603 3318 4822 051 30339 330 5% 0.062W 3318 4822 051 30339 330 5% 0.062W 2518 4822 126 14305 100nF 10% 16V 0603 3329 4822 051 300479 470 5% 0.062W 4702 4822 209 17375 GM71V18163CJ-6 2519 4822 126 14305 100nF 10% 16V 0603 3321 4822 051 300479 470 5% 0.062W 3325 4822 051 300479 470 5% 0.062W 3100 4822 051 30103 10k 5% 0.062W	2418 2419 2420 2421 2500 2501 2502 2503 2504	4822 126 14305 4822 126 14305	100nF 10% 16V 0603 100nF 10% 16V 0603	3198 3199 3201 3214 3216 3224 3300 3301 3303	4822 051 30103 4822 051 30103 4822 051 30479 4822 051 30102 4822 051 30102 4822 051 30331 4822 051 30109 4822 051 30102 4822 051 30102	10k 5% 0.062W 10k 5% 0.062W 47Ω 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 33Ω 5% 0.062W 10Ω 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W	7301 7302 7303 7304	9322 166 64668 9322 166 64668 9322 150 51671	IC OTP EPC1441 ASSY IC SM CY7C1019BV33- 10VC(CYPR)R IC SM CY7C1019BV33- 10VC(CYPR)R IC SM EPF6024AQC208-3 (ALT0) Y OSC XTL SM 27MHZ 15P
2508 4822 126 14305 100nF 10% 16V 6603 3307 4822 051 30102 1 k 5% 0.062W 7307 3104 123 96402 IC FLASH CY2071 AUDIO ASSY 0.062W 2509 4822 126 14305 100nF 10% 16V 0603 3312 4822 051 30103 10k 5% 0.062W 3314 4822 051 30103 10k 5% 0.062W 7307 3104 123 96402 IC FLASH CY2071 AUDIO ASSY 0.062W 2511 4822 124 80151 47μF 16V 3315 4822 051 30103 10k 5% 0.062W 3316 4822 051 30303 30.5 % 0.062W 7402 4822 209 17375 GM71V18163CJ-6 2515 4822 124 80151 47μF 16V 3316 4822 051 30339 33.0 5% 0.062W 7402 4822 209 17375 GM71V18163CJ-6 2516 5322 126 11583 10nF 10% 50V 0603 3318 4822 051 30339 33.0 5% 0.062W 7403 4822 209 17375 GM71V18163CJ-6 2518 4822 124 80151 47μF 16V 3316 4822 051 30339 33.0 5% 0.062W 7402 4822 209 17375 GM71V18163CJ-6 2518 4822 126 11583 10nF 10% 50V 0603 3319 4822 051 30339 33.0 5% 0.062W 7403 4822 209 17375 GM71V18163CJ-6 2518 4822 126 14305 100nF 10% 16V 0603 3321 4822 051 30479 47.0 5% 0.062W 7500 9352 424 20118 IC SM 74VC04APW 2519 4822 126 14305 100nF 10% 16V 0603 3322 4822 051 30479 47.0 5% 0.062W 3325 4822 051 30479 47.0 5% 0.062W 3101 4822 051 30103 10k 5% 0.062W 3326 4822 051 30479 47.0 5% 0.062W 3104	2418 2419 2420 2421 2500 2501 2502 2503 2504 2505	4822 126 14305 4822 126 14305	100nF 10% 16V 0603 100nF 10% 16V 0603 47µF 16V	3198 3199 3201 3214 3216 3224 3300 3301 3303 3304	4822 051 30103 4822 051 30103 4822 051 30179 4822 051 30102 4822 051 30102 4822 051 30331 4822 051 30109 4822 051 30102 4822 051 30102 4822 051 30102	$\begin{array}{l} 10k\ 5\%\ 0.062W \\ 10k\ 5\%\ 0.062W \\ 47\Omega\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 330\Omega\ 5\%\ 0.062W \\ 10\Omega\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \end{array}$	7301 7302 7303 7304	9322 166 64668 9322 166 64668 9322 150 51671 2422 543 89006	IC OTÉ EPC1441 ASSY IC SM CY7C1019BV33- 10VC(CYPR)R IC SM CY7C1019BV33- 10VC(CYPR)R IC SM EPF6024AQC208-3 (ALTO) Y OSC XTL SM 27MHZ 15P FX0-35F R IC SM CY7C1019BV33-
2509 4822 126 14305 100nF 10% 16V 0603 3312 4822 051 30103 10k 5% 0.062W 7308 3104 123 96402 IC FLASH CY2071 AUDIO ASSY	2418 2419 2420 2421 2500 2501 2502 2503 2504 2505 2506	4822 126 14305 4822 126 14305	100nF 10% 16V 0603 100nF 10% 16V 0603 47µF 16V 100nF 10% 16V 0603	3198 3199 3201 3214 3216 3224 3300 3301 3303 3304 3305	4822 051 30103 4822 051 30103 4822 051 30179 4822 051 30102 4822 051 30331 4822 051 30109 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102	$\begin{array}{l} 10k\ 5\%\ 0.062W \\ 10k\ 5\%\ 0.062W \\ 47\Omega\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 330\Omega\ 5\%\ 0.062W \\ 10\Omega\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \\ 1k\ 5\%\ 0.062W \end{array}$	7301 7302 7303 7304 7305	9322 166 64668 9322 166 64668 9322 150 51671 2422 543 89006 9322 166 64668	IC OTÉ EPC1441 ASSY IC SM CY7C1019BV33- 10VC(CYPR)R IC SM CY7C1019BV33- 10VC(CYPR)R IC SM EPF6024AQC208-3 (ALT0) Y OSC XTL SM 27MHZ 15P FX0-35F R IC SM CY7C1019BV33- 10VC(CYPR)R
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0.5 4022 UST 300308 3312 5% U.UDZYY 0.5 TT	2418 2419 2420 2421 2500 2501 2503 2504 2505 2506 2507 2508 2507 2511 2512 2514 2515 2516 2517 2518 2519 2520 2510 3100 3101 3102 3104 3108 3109 3111 3112 3113 3114 3115	4822 126 14305 4822 124 80151 4822 124 80151 4822 124 80151 4822 124 80151 4822 124 80151 4822 126 11583 5322 126 11583 4822 126 14305 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30393 4822 051 30103 4822 051 30393 4822 051 30103 4822 051 30103 4822 051 30393 4822 051 30103 4822 051 30393 4822 051 30391 4822 051 30391 4822 051 30391 4822 051 30391 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103	100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 47μF 16V 100nF 10% 16V 0603 47μF 16V 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 16V 0603 10nF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603 10xF 10% 16V 0603	3198 3199 3201 3214 3216 3224 3300 3301 3303 3304 3305 3307 3312 3313 3315 3316 3317 3318 3319 3320 3321 3322 3323 3401 3402 3403 3404 3405 3505 3506 3501 3502 3501 3502 3501 3502 3501 3502 3501 3502 3501 3502 3501 3502 3501 3502 3501 3502 3501 3502 3501 3502 3503 3503 3504 3503 3504 3503 3504 3503 3504 3503 3603 3603 3603 3603 3603 3603 3603	4822 051 30103 4822 051 30103 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30109 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30103 4822 051 30103 4822 051 30133 4822 051 30339 4822 051 30339 4822 051 30339 4822 051 30339 4822 051 30339 4822 051 30339 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30579 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30479 4822 051 30579	10k 5% 0.062W 10k 5% 0.062W 47Ω 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 10Ω 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 10Ω 5% 0.062W 47Ω 5% 0.062W 47Ω 5% 0.062W 47Ω 5% 0.062W 47Ω 5% 0.062W 47Ω 5% 0.062W 47Ω 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Κ 5% 0.062W 10Ω 5% 0.062W	7301 7302 7303 7304 7305 7306 7307 7308 7402 7403 7404 7500 7505 7506 SERV Variou 1100 1100 1201 1300 1302	9322 166 64668 9322 150 51671 2422 543 89006 9322 166 64668 9322 166 64668 9322 166 64668 3104 123 96511 4822 209 17375 4822 209 17375 9322 169 98671 9352 424 20118 9352 351 50118 9352 351 50118 9352 668 39118 /O PWB 8 2422 025 16143 2422 025 17425 2422 540 98428 4822 267 51454 2422 025 16158	IC OTÉ EPC1441 ASSY IC SM CY7C1019BV33- 10VC(CYPR)R IC SM CY7C1019BV33- 10VC(CYPR)R IC SM EPF6024AQC208-3 (ALT0) Y OSC XTL SM 27MHZ 15P FX0-35F R IC SM CY7C1019BV33- 10VC(CYPR)R IC SM CY7C1019BV33- 10VC(CYPR)R IC FLASH CY2071 AUDIO ASSY IC FLASH CY2071 VIDEO ASSY GM71V18163CJ-6 IC SM NW701 TQFP160 (DIIN) Y IC SM 74LVC04APW (PHSE) R IC SM 74LVC16244ADGG (PHSE) R IC SM UDA1334ATS/N2 (PHSE) R IC SM UDA1334ATS/N2 (PHSE) R CON BM H 45P F 0.5 54132 R CON BM H45P F 0.5 54132 R RES CER SM 8M467 CSTCC8.46MHz R CONN. 11P FEMALE CON BM H 8P F 1.00 FFC 0.3 R
	2418 2419 2420 2421 2500 2501 2503 2504 2505 2506 2507 2508 2507 2511 2512 2514 2515 2516 2517 2518 2519 2520 2510 3100 3101 3102 3104 3108 3109 3111 3112 3113 3114 3115	4822 126 14305 4822 124 80151 4822 124 80151 4822 124 80151 4822 124 80151 4822 124 80151 4822 126 11583 5322 126 11583 4822 126 14305 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30393 4822 051 30103 4822 051 30393 4822 051 30103 4822 051 30103 4822 051 30393 4822 051 30103 4822 051 30393 4822 051 30391 4822 051 30391 4822 051 30391 4822 051 30391 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103	100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 47µF 16V 100nF 10% 16V 0603 47µF 16V 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 16V 0603 100nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 50V 0603 10nF 10% 16V 0603 10nF 10% 16V 0603 100nF 10% 16V 0603	3198 3199 3201 3214 3216 3224 3300 3301 3303 3304 3305 3306 3307 3312 3318 3316 3317 3318 3319 3320 3321 3322 3325 3327 3328 3329 3400 3401 3402 3403 3404 3505 3506 3519 3506 3519 3520 3521 3522 3523 3524	4822 051 30103 4822 051 30103 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30109 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30102 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30103 4822 051 30339 4822 051 30339 4822 051 30339 4822 051 30339 4822 051 30479 4822 051 30101	10k 5% 0.062W 10k 5% 0.062W 47Ω 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 1k 5% 0.062W 10Ω 5% 0.062W	7301 7302 7303 7304 7305 7306 7307 7308 7402 7403 7404 7500 7505 7506 SERV Variou 1100 1100 1201 1300 1302	9322 166 64668 9322 150 51671 2422 543 89006 9322 166 64668 9322 166 64668 9322 166 64668 3104 123 96511 4822 209 17375 4822 209 17375 9322 169 98671 9352 424 20118 9352 351 50118 9352 668 39118 /O PWB 8 2422 025 16143 2422 025 16143 2422 025 16158 2422 025 16158	IC OTÉ EPC1441 ASSY IC SM CY7C1019BV33- 10VC(CYPR)R IC SM CY7C1019BV33- 10VC(CYPR)R IC SM CY7C1019BV33- 10VC(CYPR)R IC SM EPF6024AQC208-3 (ALT0) Y OSC XTL SM 27MHZ 15P FX0-35F R IC SM CY7C1019BV33- 10VC(CYPR)R IC SM CY7C1019BV33- 10VC(CYPR)R IC FLASH CY2071 AUDIO ASSY GM71V18163CJ-6 GM71V18163CJ-6 IC SM NW701 TQFP160 (DIIN) Y IC SM 74LVC04APW (PHSE) R IC SM 74LVC16244ADGG (PHSE) R IC SM UDA1334ATS/N2 (PHSE) R IC SM UDA1334ATS/N2 (PHSE) R CON BM H 45P F 0.5 54132 R CON BM H 45P F 0.5 54132 R CON BM H 45P F 0.5 54132 R CON BM H 45P F 0.5 54132 R CON BM H 45P F 0.5 54132 R CON BM H 45P F 0.5 54132 R CON BM H 45P F 0.5 54132 R CON BM H 45P F 0.5

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1401	2422 540 98428	RES CER SM 8M467 CSTCC8.46MHz R	2333 2334	5322 124 41945	22μF 20% 35V 100nF 10% 16V 0603	3256		27k 5% 0.062W
1402	2422 025 17276	CON BM H 30P F 1.00 FFC	2335		0603 16V 2N2 PM5 R	3257 3258		27k 5% 0.062W 27k 5% 0.062W
		SMT R	2336		0603 16V 47nF COL	3259		NETW 4 X 47Ω 5% MNR14
			2337	3198 017 34730	0603 16V 47nF COL	3260		NETW 4 X 47Ω 5% MNR14
⊣⊢			2338		0603 16V 2N2 PM5 R	3261		10k 5% 0.062W
••			2339	4822 124 23002		3262	4822 117 11817	
2002	5322 126 11583	10nF 10% 50V 0603	2400 2401	4822 124 23002	10µF 16 V 10nF 10% 50V 0603	3264 3265		100k 1% 0603 0.62W 100k 1% 0603 0.62W
2003	4822 124 23002		2402		100nF 10% 16V 0603	3266		10k 1% 0603 0.02W
2004		10nF 10% 50V 0603	2403		100nF 10% 16V 0603	3267		10k 5% 0.062W
2005 2008	4822 124 23002	10nF 10% 50V 0603	2404		22nF 10% 25V 0603	3268	4822 051 30103	10k 5% 0.062W
2009	4822 124 23002		2405		22nF 10% 25V 0603	3269	4822 051 30102	
2010		10nF 10% 50V 0603	2406 2407		100nF 10% 16V 0603 100nF 10% 16V 0603	3270 3271	4822 051 30102 4822 051 30102	
2011	4822 124 23002		2409		100nF 10% 16V 0603	3272		10k 5% 0.062W
2012 2013		10nF 10% 50V 0603	2410	4822 122 33777	47pF 5% 63V	3274		10k 5% 0.062W
2013	4822 124 23002 4822 124 12084	1μF 20% SM 50V	2411	3198 030 74780	EL SM 35V 4U7 PM20 COL	3275		10k 5% 0.062W
2015		100nF 10% 16V 0603	2412	4000 100 14404	R 22nF 10% 25V 0603	3276		10k 5% 0.062W
2016	4822 124 23002		2412		EL SM 35V 4U7 PM20 COL	3300 3302		2k7 5% 0.062W 2k7 5% 0.062W
2017		10nF 10% 50V 0603		0.0000007.7700	R	3303	4822 051 30102	
2018 2019	4822 126 14305 4822 124 23002	100nF 10% 16V 0603	2414	4822 126 14238	0603 50V 2N2 COL R	3304	4822 051 30102	
2020		100nF 10% 16V 0603	2421	4822 122 33761		3305		4.7Ω 5% 0603 0.0016W
2100		100nF 10% 16V 0603	2422 2423		100nF 10% 16V 0603 100nF 10% 16V 0603	3307	5322 117 13068	82Ω 1% 0.063W 0603 RC22H
2102		100nF 10% 16V 0603	2424		100nF 10% 16V 0603	3308	4822 051 20108	
2104		10nF 10% 50V 0603	2425	4822 126 14305	100nF 10% 16V 0603	3309	4822 051 20108	
2105 2106	4822 122 33735	10nF 10% 50V 0603 27nF 10% 63V	2426		100nF 10% 16V 0603	3310	4822 117 12917	1Ω 5% 0.062W CASE0603
2110		100nF 10% 16V 0603	2427		100nF 10% 16V 0603	3311		1Ω 5% 0.062W CASE0603
2111	4822 126 14305	100nF 10% 16V 0603	2428 2429		100nF 10% 16V 0603 100nF 10% 16V 0603	3312 3314	4822 117 12917 4822 051 20108	1Ω 5% 0.062W CASE0603 1Ω 5% 0.1W
2116		100nF 10% 16V 0603	2430		100nF 10% 16V 0603	3315	4822 051 20108	
2121 2122	5322 126 11579 5322 126 11582		2431	4822 126 14305	100nF 10% 16V 0603	3316	4822 051 20228	2Ω2 5% 0.1W
2125		10nF 10% 50V 0603	2432		100nF 10% 16V 0603	3317	4822 051 20228	
2200		100nF 10% 16V 0603	2434 2435	4822 122 33741 4822 122 33761		3318 3319	4822 051 20228 4822 051 20228	
2202		100nF 10% 16V 0603	2436	4822 122 33761		3320		3k3 5% 0.062W
2203 2207	4822 124 23002 4822 126 14305	100nF 10% 16V 0603	2437	4822 122 33761		3321		56k 5% O.062W
2208		100nF 10% 16V 0603	2438 2439	4822 122 33761		3323		2k2 5% 0.062W
2209		100nF 10% 16V 0603	2440	4822 122 33761 4822 122 33761		3324	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
2210 2211		100nF 10% 16V 0603	2441	4822 122 33761		3325	5322 117 13049	470Ω 1% 0.063W 0603
2212		100nF 10% 16V 0603 10nF 10% 50V 0603	2446	5322 126 11583	10nF 10% 50V 0603	l		RC22H
2214	4822 126 14305	100nF 10% 16V 0603				3326	5322 117 13049	470Ω 1% 0.063W 0603 RC22H
2218		100nF 10% 16V 0603	\Box			3327	4822 051 30103	10k 5% O.062W
2219 2220		100nF 10% 16V 0603 100nF 10% 16V 0603	3005	4822 051 30121	120Ω 5% 0.062W	3328		470Ω 1% 0.063W 0603
2221		100nF 10% 16V 0603	3006		RST SM 0603 RC22H 43Ω		1000 117 10000	RC22H
2222		100nF 10% 16V 0603			PM1	3329 3330		100k 1% 0603 0.62W 3k3 5% 0.062W
2223 2224		100nF 10% 16V 0603 100nF 10% 16V 0603	3100 3103	4822 051 30103	10k 5% 0.062W 47k 1% 0.063W 0603	3331	4822 051 30103	
2225		100nF 10% 16V 0603	3103	3322 117 13029	RC22H	3332	2322 704 62003	RST SM 0603 RC22H 20k
2226		100nF 10% 16V 0603	3105	4822 051 30681	680Ω 5% 0.062W	3335	5322 117 12068	PM1 R 82Ω 1% 0.063W 0603
2227		100nF 10% 16V 0603	3107		100Ω 5% 0.062W	5555	3322 117 13000	RC22H
2228 2232		100nF 10% 16V 0603 100nF 10% 16V 0603	3108 3114		100Ω 5% 0.062W 100Ω 5% 0.062W	3336	4822 117 12864	82k 5% O.6W
2233	4822 122 33753		3115		100Ω 5% 0.062W	3337	4822 051 30273	
2234	4822 122 33753		3121		680Ω 5% 0.062W	3338 3339	4822 051 30103 4822 117 12864	
2235		100nF 10% 16V 0603	3122		1k5 5% 0.062W	3340	4822 051 30332	
2236 2237		100nF 10% 16V 0603 100nF 10% 16V 0603	3129 3130		150k 5% 0.062W 100Ω 5% 0.062W	3341	4822 051 30102	
2238		100nF 10% 16V 0603	3200	4822 051 30103		3342	4822 051 30273	
2300	5322 126 11583	10nF 10% 50V 0603	3201	4822 051 30103	10k 5% 0.062W	3343 3344	4822 051 30103 4822 051 30332	
2301	4822 124 23002		3204		1Ω 5% 0.062W CASE0603	3345	4822 051 30302	
2302 2303		0603 16V 47nF COL EL SM 35V 4U7 PM20 COL	3205 3210	4822 051 30103 4822 117 13573	10k 5% 0.062W NETW 4 X 47Ω 5% MNR14	3346		470Ω 1% 0.063W 0603
_500	3.33 000 1 7100	R	3214	4822 051 30103		2247	E000 447 40040	RC22H
2304		10nF 10% 50V 0603	3216	4822 051 30103	10k 5% 0.062W	3347	JOZZ 11/ 13049	470Ω 1% 0.063W 06 0 3 RC22H
2305 2309	4822 124 23002 3198 016 31020		3217 3221	4822 051 30103		3348	4822 117 13632	100k 1% 0603 0.62W
2309	3198 016 31020		3221	4822 051 30472 4822 051 30103		3351	4822 051 30472	4k7 5% D.062W
2311		22nF 10% 25V 0603	3224	4822 051 30105		3352	4822 051 30153	
2312	2238 786 11554	0603 16V 2N2 PM5 R	3225	4822 051 30331	330Ω 5% 0.062W	3353 3354	4822 051 30123 4822 117 11817	
2313		100nF 10% 16V 0603	3226		NETW 4 X 47Ω 5% MNR14	3355	4822 051 30332	
2314 2315	3198 016 31020 4822 126 14305	0603 25V 1nF 100nF 10% 16V 0603	3227	4022 11/ 13525	24k 1% 0.62W RC22H 0603	3356	4822 051 30472	4k7 5% O.062W
2316		100nF 10% 16V 0603	3231	4822 117 13573	NETW 4 X 47Ω 5% MNR14	3357		100k 1% 0603 0.62W
2317	5322 126 11583	10nF 10% 50V 0603	3235	4822 051 30103	10k 5% 0.062W	3358 3359	4822 051 30102 2322 704 62002	1 k 5% 0.062W RST SM 0603 RC22H 2k
2318 2319	3198 016 31020	0603 25V 1nF 100nF 10% 16V 0603	3236 3237	4822 051 30103		5500		PM1 R
2320	3198 016 31020		3237	4822 051 30223 4822 051 30222		3361	4822 051 30563	56k 5% ⊅ .062W
2321	3198 016 31020		3241	4822 051 30103		3362	4822 051 30103	
2322	4822 126 14305	100nF 10% 16V 0603	3244	4822 051 30103	10k 5% 0.062W	3364 3365	4822 051 30272 4822 051 30272	
2323		22nF 10% 25V 0603		4822 051 30472		3366		470Ω 5% 0.062W
2324 2325	5322 124 41945 4822 126 14305	22μF 20% 35V 100nF 10% 16V 0603		4822 051 30479 4822 051 30103		3368	4822 051 30471	470Ω 5% 0.062W
2326		0603 50V 15nF COL R		4822 051 30479		3370	4822 051 30103	
2327	4822 126 14305	100nF 10% 16V 0603	3251	4822 051 30222	2k2 5% 0.062W	3400 3401	4822 117 11817 2350 035 10152	1k2 1% /16W RST NET W SM ARV24
2328 2329		0603 50V 15nF COL R 100nF 10% 16V 0603		4822 051 30222 4822 051 30273				4X1k5 P▶15 R
2331		100nF 10% 16V 0603		4822 051 30273		3407	4822 117 13525	24k 1% () .62W RC22H
2332		100nF 10% 16V 0603	3255	4822 051 30273		3408	4822 051 30103	0603 10k 5% i . 062W
					ı	5-700	.022 001 00100	TOR U JOU SUCKY

3409	4822 051 30183	18k 5% 0.062W				2226	4822 126 14305	100nF 10% 16V 0603
3410	2350 035 10152	RST NETW SM ARV24	LACC	ESSORIES		2227	4822 126 14305	100nF 10% 16V 0603
		4X1k5 PM5 R	^			2228	4822 126 14305	100nF 10% 16V 0603
3411	4822 117 12139	22Ω 5% 0.062W				2229		EL SM 35V 4U7 PM20 COL
3415		100Ω 5% 0.062W	Vario	us		2220	3130 030 14100	
			• • • • •	40			1000 100 1100=	R
3416	4822 051 30105		0040	2104 207 10652	IDT DDOD ACCV	2230		100nF 10% 16V 0603
3417	4822 051 30331	330Ω 5% 0.062W	0318	3104 207 10052	IRT PROD ASSY	2231	3198 030 74780	EL SM 35V 4U7 PM20 COL
3418	4822 117 13578	4X10k 5% MNR14			RC2050/01 PACKED			R
3419	4822 117 13573	NETW 4 X 47Ω 5% MNR14	0320	4822 321 22611	AUDIO CORD GOLD	2241	3198 016 31020	0603 25V 1nF
3420		RST NETW SM ARV24 4X			PLATED	2300		100nF 10% 16V 0603
0720	2000 000 01001		0321	3104 128 92490	VIDEO CORD SET GOLD			
0.400	4000 447 40570	jumper R	1	010112002100	PLATED	2301		100nF 10% 16V 0603
3430		4X10k 5% MNR14	0222	2422 070 00122		2302		100nF 10% 16V 0603
3431		NETW 4 X 47Ω 5% MNR14	0322		MAINSCORD EUR	2303	4822 126 14305	100nF 10% 16V 0603
3439	4822 051 30109	10Ω 5% 0.062W	0322		MAINSCORD UK	2304	4822 126 14305	100nF 10% 16V 0603
3440	4822 051 30109	10Ω 5% 0.062W	0323	4822 321 61847	SCART CABLE	2305	4822 126 14305	100nF 10% 16V 0603
3448	2350 035 91001	RST NETW SM ARV24 4X	0324	3111 170 21592	CORDON ANT, L.1,50M	2306		100nF 10% 16V 0603
		iumper R	0370	4822 321 61849	S-VIDEO CORD	2307		100nF 10% 16V 0603
3449	4000 117 10570							
		NETW 4 X 47Ω 5% MNR14				2308		100nF 10% 16V 0603
3450		NETW 4 X 47Ω 5% MNR14	DICI	TAL DWD		2309	4822 126 14305	100nF 10% 16V 0603
3451	4822 117 11817	1k2 1% 1/16W	Digi	TAL PWB		2310	4822 126 14305	100nF 10% 16V 0603
3461	4822 051 30102	1k 5% 0.062W				2311	4822 126 14305	100nF 10% 16V 0603
3463	4822 051 30101	100Ω 5% 0.062W	Vario	110		2312	4822 126 14305	100nF 10% 16V 0603
3468	4822 051 30101	100Ω 5% 0.062W	Vario	uə		2313		100nF 10% 16V 0603
3469		100Ω 5% 0.062W		0.100.005.150.10	0011011111	2314		100nF 10% 16V 0603
0.100	1022 001 00101	10022 5 /0 0.00211	1100	2422 025 17018	CON BM V 15P F 1.00 FFC			
			1		0.3 R	2315		100nF 10% 16V 0603
			1101	2422 025 17018	CON BM V 15P F 1.00 FFC	2316		100nF 10% 16V 0603
					0.3 R	2317	4822 126 14305	100nF 10% 16V 0603
5100	1000 157 11071	100	1200	2422 025 16957	CON BM V 24P F 1.00 FFC	2318	4822 126 14305	100nF 10% 16V 0603
5100	4822 157 11074		l	020 10001	0.3 R	2319		100nF 10% 16V 0603
5102	4822 157 11074		4504	0400 005 40000		2320		100μF 20% 16V
5104	4822 157 11074		1501	2422 025 16939	CON BM V 60P F 0.80	2321		100μF 20% 16V
5200	4822 157 11074	100μH	l		84616 R			
5201		IND FXD SM EMI 100mH z	1600	2422 025 16729	CON BM V 10P F 1.00 FFC	2322		100μF 20% 16V
	0 10 401 00	30R R	l .		0.3 R	2323		100nF 10% 16V 0603
E202	0400 E40 40700		1601	2422 025 16389	CON BM V 22P F 1.00 FFC	2400	4822 126 14305	100nF 10% 16V 0603
5202	2422 549 43/69	IND FXD SM EMI 100mH z	1001	2422 020 10000	0.3 R	2401		100nF 10% 16V 0603
		30R R	4000	0400 005 40000		2402		100nF 10% 16V 0603
5203	2422 549 43769	IND FXD SM EMI 100mH z	1602	2422 025 16389	CON BM V 22P F 1.00 FFC	2403		
		30R R			0.3 R			100nF 10% 16V 0603
5300	2422 549 43769	IND FXD SM EMI 100mH z				2404		100nF 10% 16V 0603
0000	Z-122 0-10 101 00	30R R				2405	4822 126 14305	100nF 10% 16V 0603
E004	0400 540 40700		- -			2406	4822 126 14305	100nF 10% 16V 0603
5301	2422 549 43/69	IND FXD SM EMI 100mH z				2407		100nF 10% 16V 0603
		30R R	2100	4822 126 14305	100nF 10% 16V 0603	2408		100nF 10% 16V 0603
5302	2422 549 43769	IND FXD SM EMI 100mH z	2101		100nF 10% 16V 0603			
		30R R				2409		100nF 10% 16V 0603
5400	4822 157 11074		2102		100nF 10% 16V 0603	2410		100nF 10% 16V 0603
			2103		100nF 10% 16V 0603	2411	4822 126 14305	100nF 10% 16V 0603
5401	4822 157 11074		2104	4822 126 14305	100nF 10% 16V 0603	2412		EL SM 50V 2U2 PM20 COL
5402	2422 549 43769	IND FXD SM EMI 100mH z	2105	4822 126 14305	100nF 10% 16V 0603			R
		30R R	2106		100nF 10% 16V 0603	2413	4000 100 14005	
_			2107		100nF 10% 16V 0603			100nF 10% 16V 0603
-						2414		100nF 10% 16V 0603
→			2108		100nF 10% 16V 0603	2415	4822 126 14305	100nF 10% 16V 0603
			2109	4822 126 14305	100nF 10% 16V 0603	2416	4822 126 14305	100nF 10% 16V 0603
6301	4822 130 11397	BAS316	2110	4822 126 14305	100nF 10% 16V 0603	2417		100nF 10% 16V 0603
	1022 100 11007	BAGGTO	2111		100nF 10% 16V 0603	2418		100nF 10% 16V 0603
			2112		100nF 10% 16V 0603			
B			2113		100nF 10% 16V 0603	2419		100nF 10% 16V 0603
						2420		100nF 10% 16V 0603
7000	0222 450 00000	IC CM I MOSTDOT (ONICE)	2114		100nF 10% 16V 0603	2421	4822 126 14305	100nF 10% 16V 0603
7000	9322 100 69666	IC SM LM337D2T (ONSE)	2115	4822 126 14305	100nF 10% 16V 0603	2422	4822 126 14305	100nF 10% 16V 0603
		R	2116	4822 126 14305	100nF 10% 16V 0603	2423	4822 126 14305	100nF 10% 16V 0603
7001	9322 121 67668	IC SM LF33CD (ST00) R	2117	4822 126 14305	100nF 10% 16V 0603	2424		100nF 10% 16V 0603
7101	9352 688 06157	IC SM TZA1031HL (PHSE)	2118		100nF 10% 16V 0603			
		Υ	2119		EL SM 35V 4U7 PM20 COL	2425	J 190 USU /4/80	EL SM 35V 4U7 PM20 COL
7200	4822 130 60373	· · ·	- ' ' ' ' '	0100 000 74700				R
7201		IC SM ADM810SART	٠	4000 400 4400	R	2426	3198 030 82280	EL SM 50V 2U2 PM20 COL
1201	JULE 100 20000		2120		100nF 10% 16V 0603			R
700-	0404 :	(ANAO) Y	2121	4822 126 14305	100nF 10% 16V 0603	2550	4822 126 14305	100nF 10% 16V 0603
7202	3104 123 96450	IC FLASH BASIC ENGINE	2122	4822 126 14305	100nF 10% 16V 0603	2551		100nF 10% 16V 0603
		DVD+RW	2123		100nF 10% 16V 0603	2552		
7203	9352 687 34557	IC SM SAA7830HL (PHSE)	2124		100nF 10% 16V 0603			100nF 10% 16V 0603
-		Y	2125			2553		100nF 10% 16V 0603
7204	9322 026 00695	CY7C1399-15ZC			100nF 10% 16V 0603	2554		100nF 10% 16V 0603
7204			2126		100nF 10% 16V 0603	2555	4822 126 14305	100nF 10% 16V 0603
	4822 130 60373		2127	3198 030 74780	EL SM 35V 4U7 PM20 COL	2556	4822 126 14305	100nF 10% 16V 0603
7206		IC EPLD BASIC ENGINE	1		R	2557		100nF 10% 16V 0603
7301	9322 139 85668		2128	4822 126 14494	22nF 10% 25V 0603	2558		100nF 10% 16V 0603
7302	4822 209 17229	BA5938FM	2129					
7304	4822 209 30095				100nF 10% 16V 0603	2559	4822 122 33761	
7306			2202		100nF 10% 16V 0603	2560	4822 122 33761	22pF 5% 50V
1300	200 DDDDB	IC SM BA5944FP (RHM0)	2203	4822 124 12095		2561	4822 126 14305	100nF 10% 16V 0603
700-	0040 = :-	R	2207	4822 124 23002	10μF 16V	2562		100nF 10% 16V 0603
7308	9340 547 21215	FET POW SM BSH205	2208		100nF 10% 16V 0603	2563		EL SM 35V 4U7 PM20 COL
		(PHSE) R	2209	5322 126 11579			2100 000 (4100	_
7309	4822 130 60511		2210		0603 50V 330P COL R	0564	4000 400 4 400	R
7310	4822 130 60511		2211			2564		100nF 10% 16V 0603
7311	4822 130 60511				100nF 10% 16V 0603	2565	3198 030 74780	EL SM 35V 4U7 PM20 COL
			2212		100nF 10% 16V 0603			R
7312		IC SM LD1117DT (ST00) R	2213	4822 126 14305	100nF 10% 16V 0603	2566	4822 126 14305	100nF 10% 16V 0603
7400	5322 209 30676	TDA8703T/C4	2214		100nF 10% 16V 0603	2567		EL SM 35V 4U7 PM20 COL
7401	9322 171 97671	IC SM UPD65943GC-081	2215		100nF 10% 16V 0603	_507	2100 000 14100	_
		(NEC0) Y	2216			0500	4000 400 4 :	R
7402	9352 697 26557	IC SM SAA7831HL (PHSE)			100nF 10% 16V 0603	2568		100nF 10% 16V 0603
,	2002 001 30001		2217		100nF 10% 16V 0603	2569	3198 030 74780	EL SM 35V 4U7 PM20 COL
		Y	2218		100nF 10% 16V 0603			R
			2219	4822 126 14305	100nF 10% 16V 0603	2570	4822 126 14305	100nF 10% 16V 0603
			2220		100nF 10% 16V 0603	2571		
		İ	2221		100nF 10% 16V 0603			100nF 10% 16V 0603
			2222			2572		100nF 10% 16V 0603
					100nF 10% 16V 0603	2573		100nF 10% 16V 0603
			2223		100nF 10% 16V 0603	2574		100nF 10% 16V 0603
			2224		100nF 10% 16V 0603	2575		100nF 10% 16V 0603
			2225	4822 126 14305	100nF 10% 16V 0603	2576		100nF 10% 16V 0603
				-	I	_0,0	.522 120 14000	10/0 10 7 0000

2577	4822 126 14305	100nF 10% 16V 0603	2814	4822 126 14305	100nF 10% 16V 0603	3273	5322 117 13051	680Ω 1% 0.063W 0603
2578		100nF 10% 16V 0603	2818	5322 124 41945		02.0	0022 111 10001	RC22H
2579		100nF 10% 16V 0603	2819		68pF 5% 63V CASE 0603	3304	4822 051 30103	10k 5% 0.062W
2580		EL SM 35V 4U7 PM20 COL	2821		EL SM 50V 2U2 PM20 COL	3305	4822 051 30103	
		R			R	3400	4822 051 30472	
2581	4822 126 14305	100nF 10% 16V 0603	2900	4822 126 14305	100nF 10% 16V 0603	3401	4822 051 30472	
2582		100nF 10% 16V 0603	2901		100nF 10% 16V 0603	3402	4822 051 30472	
2583		100nF 10% 16V 0603	2902		100nF 10% 16V 0603	3403	4822 051 30103	
2584		100nF 10% 16V 0603	2903		100nF 10% 16V 0603	3405		100Ω 5% 0.062W
2585		100nF 10% 16V 0603	2904		100nF 10% 16V 0603	3406		100Ω 5% 0.062W
2586		100nF 10% 16V 0603	2912	4822 122 33741	10pF 10% 50V	3407		33Ω 5% 0.062W
2587		100nF 10% 16V 0603	2914	4822 122 33741		3408		NETW 4 X 33Ω 5% 1206
2588		EL SM 35V 4U7 PM20 COL	2916	4822 122 33741		3409		NETW 4 X 33Ω 5% 1206
2000	0100 000 7 17 00	R	2917	4822 122 33741	•	3410		NETW 4 X 33Ω 5% 1206
2589	4822 126 14305	100nF 10% 16V 0603	2918	4822 122 33741		3552		100Ω 5% 0.062W
2590		100nF 10% 16V 0603	2919	4822 122 33741		3553		100Ω 5% 0.062W
2591		100nF 10% 16V 0603	2920	4822 122 33761		3554		1Ω 5% 0.062W CASE0603
2592		100nF 10% 16V 0603	2921		100nF 10% 16V 0603	3555	4822 051 30103	
2593		100nF 10% 16V 0603	2922		100nF 10% 16V 0603	3556	4822 051 30222	
2594	3198 030 74780	EL SM 35V 4U7 PM20 COL	2923		100nF 10% 16V 0603	3557	4822 051 30472	
		R	2924	4822 126 14305	100nF 10% 16V 0603	3559	4822 051 30103	10k 5% 0.062W
2595	4822 126 14305	100nF 10% 16V 0603	2925	4822 126 14305	100nF 10% 16V 0603	3560	4822 051 30103	10k 5% 0.062W
2596	3198 030 74780	EL SM 35V 4U7 PM20 COL				3561	4822 051 30222	2k2 5% 0.062W
		R				3562	4822 051 30472	4k7 5% 0.062W
2600	4822 126 14305	100nF 10% 16V 0603				3563	4822 051 30008	0Ω jumper
2601	4822 122 33777	47pF 5% 63V	2100	4922 DE1 20102	10k E9/ 0 060W	3601	2322 704 64301	RST SM 0603 RC22H
2602	4822 122 33777	•	3100 3101		10k 5% 0.062W 2k2 5% 0.062W	l		430ΩP M 1 R
2603		100nF 10% 16V 0603	3102		4k7 5% 0.062W	3602	2322 704 64301	RST SM 0603 RC22H
2605		100nF 10% 16V 0603	3102		10Ω 5% 0.062W	l		430ΩPM1 R
2606	4822 122 33777		3104		10Ω 5% 0.062W	3603	4822 051 30102	
2607	4822 122 33777		3106		10Ω 5% 0.062W	3604		22Ω 5% 0.062W
2608		100nF 10% 16V 0603	3107		10Ω 5% 0.062W	3605		1Ω 5% O.062W CASE0603
2609		100nF 10% 16V 0603	3108		10Ω 5% 0.062W	3606	2322 704 64301	RST SM 0603 RC22H
2610		100nF 10% 16V 0603	3109		10Ω 5% 0.062W	l		430ΩPM1 R
2611	4822 122 33777		3110		10Ω 5% 0.062W	3607	2322 704 64301	RST SM 0603 RC22H
2612	4822 122 33777	•	3111		4k7 5% 0.062W	l		430ΩP M 1 R
2613		100nF 10% 16V 0603	3112	4822 051 30472		3608	4822 051 30102	
2614		100nF 10% 16V 0603	3113		4k7 5% 0.062W	3610		1Ω 5% O.062W CASE0603
2615		100nF 10% 16V 0603	3114		4k7 5% 0.062W	3611	2322 /04 64301	RST SM 0603 RC22H
2616 2617	4822 122 33777 4822 122 33777		3115	4822 051 30103	10k 5% 0.062W	3612	0000 704 64004	430ΩPM1 R
2618		100nF 10% 16V 0603	3116	4822 051 30103	10k 5% 0.062W	3012	2322 / 04 64301	RST \$M 0603 RC22H 430ΩPM1 R
2619		100nF 10% 16V 0603	3117		2k2 5% 0.062W	3613	4822 051 30102	
2620		100nF 10% 16V 0603	3119		47Ω 5% 0.062W	3616		RST SM 0603 RC22H
2621	4822 122 33777		3120		47Ω 5% 0.062W			430ΩP M 1 R
2622	4822 122 33777	47pF 5% 63V	3121		NETW 4 X 33Ω 5% 1206	3617	2322 704 64301	RST \$M 0603 RC22H
2625	4822 126 14305	100nF 10% 16V 0603	3122		NETW 4 X 33Ω 5% 1206	1		430ΩP M 1 R
2626	4822 122 33777	47pF 5% 63V	3123		1Ω 5% 0.062W CASE0603	3618	4822 051 30102	1k 5% 0.062W
2627	4822 122 33777	47pF 5% 63V	3124 3125		1Ω 5% 0.062W CASE0603 1Ω 5% 0.062W CASE0603	3619	4822 051 30109	10Ω 5% 0.062W
2628		100nF 10% 16V 0603	3126		1Ω 5% 0.062W CASE0603	3621	2322 704 64301	RST SMI 0603 RC22H
2629		100nF 10% 16V 0603	3200	4822 051 30332				430ΩP M 1 R
2630	3198 030 74780	EL SM 35V 4U7 PM20 COL	3201		82Ω 1% 0.063W 0603	3622	2322 704 64301	RST \$M 0603 RC22H
2633	4922 126 14205	R 100nF 10% 16V 0603			RC22H	3624	4822 051 30102	430ΩP M 1 R
2634		EL SM 35V 4U7 PM20 COL	3205	4822 051 30101	100Ω 5% 0.062W	3626		RST \$M 0603 RC22H
	0100 000 1 1700	R	3206		100Ω 5% 0.062W	0020	2022 704 04301	430ΩP M 1 R
2637	4822 126 14305	100nF 10% 16V 0603	3207		10k 5% 0.062W	3627	2322 704 64301	RST SM 0603 RC22H
2642	4822 122 33761		3208	5322 117 13068	82Ω 1% 0.063W 0603			430ΩPM1 R
2643	4822 122 33761	22pF 5% 50V	2000	4000 447 40570	RC22H	3628	4822 051 30102	
2644	4822 122 33761	22pF 5% 50V	3209		4X10k 5% MNR14	3629		180Ω5% 0.062W
2645	4822 126 14305	100nF 10% 16V 0603	3210		1Ω 5% 0.062W CASE0603	3630		180Ω5% 0.062W
2646	4822 126 14494	22nF 10% 25V 0603	3211 3212	4822 051 30222		3631		1Ω 5% O .062W CASE0603
2647	4822 126 14247	0603 50V 1N5 COL R	3212	3196 031 11010	RST NETW 1206 4X100Ω	3632	4822 051 30561	560Ω;% 0.062W
2648		0603 50V 1N5 COL R	3213	3108 031 11010	PM5 COL R RST NETW 1206 4X100Ω	3633	4822 051 30561	560Ω 5% 0.062W
2700		10nF 10% 50V 0603	ا کا کا	0100000111010	PM5 COL R	3641	4822 117 12139	22Ω 5% O.062W
2701		0603 10V 470nF COL	3214	4822 051 30101	100Ω 5% 0.062W	3642		100Ω 5% 0.062W
2702		100nF 10% 16V 0603	3215		100Ω 5% 0.062W	3643		100Ω ;% 0.062W
2703		100nF 10% 16V 0603	3216		10Ω 5% 0.062W	3644		100Ω 1% 0.062W
2704	3198 030 74780	EL SM 35V 4U7 PM20 COL	3217		100Ω 5% 0.062W	3645	4822 051 30222	
6767	4000 404 4555	R	3218		100Ω 5% 0.062W	3646		180Ω 1% 0.062W
2705		1μF 20% SM 50V	3221		22Ω 5% 0.062W	3647		560Ω 1% 0.062W
2706		100nF 10% 16V 0603	3236	4822 051 30152		3648		100Ω 1% 0.062W
2707		1μF 20% SM 50V	3237	4822 051 30152		3649		100Ω % 0.062W
2708 2709		100nF 10% 16V 0603 1μF 20% SM 50V	3238	4822 051 30332		3650		100k 1% 0603 0.62W
			3240	4822 051 30332		3651	4822 051 30103	
2710 2711		100nF 10% 16V 0603 1μF 20% SM 50V	3241	4822 051 30103		3652 3653	4822 051 30682	
2712		100nF 10% 16V 0603	3242	4822 051 30103		3654		100k 1% 0603 0.62W 100Ω % 0.062W
2713		100nF 10% 16V 0603	3243	4822 051 30103		3655		100k 1% 0603 0.62W
2800		100nF 10% 16V 0603	3250	4822 051 30103		3656	4822 051 30103	
2801		100nF 10% 16V 0603	3251	4822 051 30332		3657	4822 051 30682	
2802		100nF 10% 16V 0603	3252	4822 051 30103		3700	4822 051 30103	
2803		EL SM 35V 4U7 PM20 COL	3253	4822 051 30332		3701	4822 051 30103	
		R	3254 3263	4822 051 30103		3702	4822 051 30103	
2804		100nF 10% 16V 0603	3264	4822 051 30103		3703	4822 051 30222	
2805	3198 030 74780	EL SM 35V 4U7 PM20 COL	3266	4822 051 30103 4822 051 30221	220Ω 5% 0.062W	3704	4822 051 30103	10k 5% (> .062W
000-	1000 100 1100	R	3267	4822 051 30103		3705	4822 051 30103	
2806		100nF 10% 16V 0603	3269		10k 1% 0.063W CASE0603	3706	4822 051 30103	
2807		EL SM 35V 4U7 PM20 COL		12,00	RC22H	3707	4822 051 30101	
2808		R 100nF 10% 16V 0603	3270	5322 117 13033	15k 1% 0.063W 0603	3708	4822 051 30101	
2808		100nF 10% 16V 0603			RC22H	3709 3710	4822 051 30103	
2813		EL SM 35V 4U7 PM20 COL	3272	5322 117 13047	330Ω 1% 0.063W 0603	3710	4822 051 30103 4822 051 30103	
_0.0		R			RC22H	3712	4822 051 30103	
		l l			l	J. 1		. S. CAU ASSETY

GB 316 10.	DVDR1000 /0x1 /691	Spare Parts List
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3713	4822 051 30472	4k7 5% 0.062W	5606	4822 157 70649	4.7μH (NL322522T-4R7J)	0101▲	4822 265 31015	
3714		4k7 5% 0.062W	5607	4822 157 70649	4.7µH (NL322522T-4R7J)			FUSE HOLDER 2P
3715	4822 051 30102		5610		15μH (NL322522T-150J)		4822 253 30383	
3716		10k 5% 0.062W	5615		15μH (NL322522T-150J)	1520▲	4822 252 11144	19398E1(3,150A)
3717		10k 5% 0.062W	5620		15μH (NL322522T-150J)			
3718		10k 5% 0.062W	5625		15μH (NL322522T-150J)	 ⊣⊢		
3719 3720		NETW 4 X 33Ω 5% 1206	5700		BLM11P600SPT	1 "		
3720		NETW 4 X 33Ω 5% 1206 NETW 4 X 33Ω 5% 1206	5701		BLM31P500SPT	2119▲	2020 554 90186	CERSAF KX 250V S 1nF
3722		NETW 4 X 33Ω 5% 1206 NETW 4 X 33Ω 5% 1206	5801 5802		BLM11P600SPT			PM20 A
3723		NETW 4 X 33Ω 5% 1206 NETW 4 X 33Ω 5% 1206	5803		BLM11P600SPT BLM11P600SPT	2120▲	4822 121 10697	220nF 20% 275V
3724		33Ω 5% 0.062W	5805		BLM11P600SPT	2125	2222 151 90053	EL 151 400V S 68µF PM20
3725		33Ω 5% 0.062W	5807		BLM11P600SPT	2129		10nF 5% 400V
3800		10k 5% 0.062W	5813		BLM11P600SPT	2130	4822 126 14525	
3802		75Ω 5% 0.062W	5900		BLM31P500SPT	2131▲	2020 554 90186	CERSAF KX 250V S 1nF
3803	4822 051 30121	120Ω 5% 0.062W	5901	4822 157 11717	BLM31P500SPT			PM20 A
3804	4822 117 12917	1Ω 5% 0.062W CASE0603				2136		220pF 10%) 1KV
3805	2322 704 62002	RST SM 0603 RC22H 2k	-QE			2139 2140		100nF 10% 50V
0000	4000 447 40400	PM1 R	00,400			2141		100nF 10% 50V 470pF 5% 50V
3806		22Ω 5% 0.062W	7100	9352 692 48557	IC SM SAA7333HL/M1	2142		220pF 5% 63V CASE
3807	5322 117 13068	82Ω 1% 0.063W 0603			(PHSE) Y	2143		100nF 10% 16V 0603
3809	4822 051 20122	RC22H 12k 5% 0.062W	7101	9322 144 96668	IC SM MT48LC4M16A2TG-	2144		470nF 10% 16V XTR
3810		RST SM 0603 RC22H 3k	l		8E (MRN)R	2145		470nF 10% 16V XTR
3010	, , , , , , , , , , , , , , , , , ,	PM1 R	7102		IC SM NC7SZ58 (FSC0) R	2146	5322 122 34099	470pF 10% 63V
3811	4822 117 12891	220k 1% ERJ3Ω	7103	9352 456 80115		2147	4822 124 40248	
3812		22Ω 5% 0.062W	7200	9322 130 41668	IC SM M24C64-WMN6	2151		100nF 10% 50V
3814		15k 1% 0.063W 0603	7000	0000 454 40073	(ST00) R	2152		0603 50V 330P COL R
		RC22H	7202	9322 151 16671		2153	4822 126 13694	
3815		2k2 5% 0.062W	7300 7301		GM71V18163CJ-6 GM71V18163CJ-6	2200	4822 124 11566	
3816		47k 1% 0.063W 0603	7301		IC SM 74LVC00AD (PHSE)	2201		100nF 10% 50V
3817		100k 1% 0603 0.62W	1,303	JUUL 400 UU I IO	R PHSE	2210	2020 021 9105/	EL YXG 16V S 680μF PM20 B
3818		22Ω 5% 0.062W	7306	9322 144 59668	IC SM MT48LC1M16A1TG-	2211	4822 124 40255	РМ20 В 100μF 20% 63V
3819	os∠∠ 11/ 13068	82Ω 1% 0.063W 0603			7S (MRN)R	2214		2200μF 20% 16V YXG EL
3820	2120 611 00010	RC22H NTC SM 0603 0W1 4k7	7307	9322 144 59668	IC SM MT48LC1M16A1TG-	2220		220µF 20% 25V
J020	4120 011 00019	PM5 R		34	7S (MRN)R	2221		100μF 20% 63V
3900	4822 051 30103		7400	4822 209 17375	GM71V18163CJ-6	2223		100nF 10% 50V
3901		100Ω 5% 0.062W	7401		GM71V18163CJ-6	2230		100μF 20% 63V
3902		100Ω 5% 0.062W	7402		GM71V18163CJ-6	2235	2020 012 93762	EL YK 50V S 330μF PM20
3906		47k 1% 0.063W 0603	7403		GM71V18163CJ-6	1		В
3907		47k 1% 0.063W 0603	7410	9352 378 90557	IC SM SAA6750H/V1	2240	2020 021 91664	EL YXG 16V S 1000μF
3908	4822 117 12925	47k 1% 0.063W 0603	7554	0050 500 00440	(PHSE) Y		1000 101 100-	PM20 B
3911	4822 051 30101	100Ω 5% 0.062W	7551	9352 500 60118		2241		100μF 20% 63V
3912		100Ω 5% 0.062 W	7552	0252 672 05510	R IC CM CAAZIIIOFAII	2251		22nF 10% 25V 0603
3913	4822 051 30103		/552	9332 073 93310	IC SM SAA7118E/V1 (PHSE) R	2501 2502		22nF 10% 25V 0603
3914		47Ω 5% 0.062W	7553	5322 130 60803		2502		100μF 20% 63V 100μF 20% 63V
3915		47Ω 5% 0.062W	7554	5322 130 60803		2511		100nF 10% 16V 0603
3916 3917		47Ω 5% 0.062W	7600	4822 130 60511		2512		100μF 20% 63V
3918		47Ω 5% 0.062W 47Ω 5% 0.062W	7601	9352 456 80115		2513		100nF 10% 50V
3919		47Ω 5% 0.062W	7602	5322 209 71568	PC74HCT14T	2515		100μF 20% 63V
3920	4822 051 30479		7606	4822 130 60511	BC847B	2520		22nF 10% 25V 0603
3921	4822 051 30479		7610	4822 130 60511	BC847B	2521	4822 124 40255	100μF 20% 63V
3922	4822 051 30479		7615	4822 130 60511				
3923	4822 051 30479		7620	4822 130 60511		ـــــا		
3924	4822 051 30479		7625	4822 130 60511				
3925	4822 051 30479		7644	4822 130 60511		31204	2122 550 00147	VDR DC 1M A/423V S MAX
3926	4822 051 30479	47Ω 5% 0.062W	7700	9322 166 64668	IC SM CY7C1019BV33-	0,20_	2122 000 00147	775V B
3927	4822 051 30479		7701	0222 166 64660	10VC(CYPR)R	3122▲	4822 053 21684	
3928	4822 051 30222		l''''	JULE 100 04008	IC SM CY7C1019BV33- 10VC(CYPR)R		4822 116 83866	
3929	4822 117 12925	47k 1% 0.063W 0603	7702	9322 166 64669	IC SM CY7C1019BV33-	3126	4822 116 83866	
			1	,00 04000	10VC(CYPR)R	3127	4822 116 83874	220k 5% 0.5W
			7703	9322 131 98671	IC SM DSP56362-80	3128	4822 116 83874	
			1		(MOTA) Y	3131	4822 116 52195	
5100	4822 157 11717		7704	2422 543 01185	OSC XTL SM 8MHZ00 15P	3132	4822 116 52195	
5101	4822 157 11717				FX0-31 R	3133 3134	4822 116 80676	
5102	4822 157 11499		7800	9322 151 71668	IC SM MK2703STR (MICL)	3134	4822 116 80676 4822 116 80676	
5103	4822 157 11717		700:	4000 000 :	R	3135		100k 1% 0603 0.62W
5200 5201	4822 157 11717		7801	4822 209 16399		3140	4822 051 30272	
5201		4.7µH (NL322522T-4R7J)	7802		27MHZ 120P FX0-31FT	3141	4822 116 52257	
5300	4822 157 70649 4822 157 11499	4.7µH (NL322522T-4R7J)	7803 7806	4822 130 60511				220Ω 5% 0.062W
5301	4822 157 11499		7900	5322 209 16384 5322 209 11578	PC74HCT9046AD		4822 051 30102	
5302	4822 157 11499		7900	9352 456 50115		3144	4822 051 30102	1k 5% 0.062W
5400	4822 157 11499		7913	4822 209 16318		3145	4822 051 20223	22k 5% 0.1W
5402	4822 157 11499		7916	9352 317 00118		3146	4822 116 52175	100Ω 5% 0.5W
5404	4822 157 11499		7917	5322 209 11578		3147	4822 051 30222	2k2 5% 0.062W
5550		RES XTL SM 24M576 12P	7918		IC SM 74LVC08AD (PHSE)		4822 116 52256	
		CX-11F R			R		4822 116 52256	
5552	4822 157 11499						4822 053 10689	
5553	4822 157 11499		D	FARCAS		3151		100k 1% 0603 0.62W
5554	4822 157 11499		PSU	50PS203	ļ		4822 116 52261 4822 116 52263	
5555 5556	4822 157 11499						4822 116 52263	
5556 5557	4822 157 11499		Variou	ıs	l		4822 051 30222	
5558	4822 157 11499			-			4822 051 30223	
5559	4822 157 11499 4822 157 11499		0010	4822 492 63066	1		4822 051 30472	
5560	4822 157 11499		0021	4822 492 63066	l		4822 116 52283	
5600		15μH (NL322522T-150J)	0025	4822 492 63524	FIX. TRANSISTOR		4822 052 10479	
		BLM31P500SPT	0040	4822 492 63066		3233	4822 117 10833	
5601			0060	4822 492 63066			4822 117 10833	
5602		BLM31P500SPT I	0000					
	4822 1 57 11717	BLM31P500SPT 15μH (NL322522T-150J)	0090	4822 492 63066			4822 116 83883	
5602	4822 1 57 11717		0090					

3253	4822 117 129	25 47k 1% 0.063W 0603 7
3254		83 470Ω 5% 0.5W
3255	5322 117 130	26 4k7 1% 0.063W 0603
3256	5322 117 130	RC22H 26 4k7 1% 0.063W 0603 7
		RC22H 7
3501 3502		56 2k2 5% 0.5W 26 4k7 1% 0.063W 0603
3302	5522 117 130	26 4k7 1% 0.063W 0603 7 RC22H 7
3503		81 680Ω 5% 0.062W
3504	5322 117 130	26 4k7 1% 0.063W 0603 7 RC22H 7
3511	4822 051 301	03 10k 5% 0.062W
3512		72 4k7 5% 0.1W 7
3513 3514		25 47k 1% 0.063W 0603 7 03 10k 1% 0.6W
3515		33 10k 1% 0.6W
3516	4822 051 3010	03 10k 5% 0.062W
3520	4822 051 205	11 510Ω 5% 0.1W 02 1k 5% 0.062W
3521 3522	4822 051 3010	49 2k2 5% 0.1W 0805
3523	4822 051 306	B1 680Ω 5% 0.062W
3524		32 3k3 5% 0.1W
3525	5322 117 130	36 1k2 1% 0.063W 0603 RC22H
		1102211
5110	2422 525 046	M IND EVD I HI 00 C OHO
5110	2422 535 946	34 IND FXD LHL08 S 2U2 PM20 A
5115	2422 535 9463	34 IND FXD LHL08 S 2U2
E400 A	4822 157 1184	PM20 A
5120	4822 157 7082	
5131▲	4822 146 1040	02 TRAFO CT395FANF/PVF
5210	2422 535 9463	
5240	2422 535 9463	PM20 32 IND FXD LHL08 S 1U
		PM30 A
5501	2422 535 9463	34 IND FXD LHL08 S 2U2 PM20 A
5505	2422 535 9463	
5511	2422 535 9463	PM20 39 IND FXD LHL08 S 10U
		PM20
5515	2422 535 9463	39 IND FXD LHL08 S 10U PM20
5520	2422 535 9463	
		FIVIZU A
→		,
6125	4822 130 4260	06 BYD33J
6130	5322 130 3457	74 1N4004G
6131	5322 130 3457	74 1N4004G
6140	4822 130 3084	12 BAV21
6141	4822 130 8375	74 1N4004G 74 1N4004G 74 1N4004G 12 BAV21 67 BAS216 12 BAV21 12 BAV21 5 DIO REG SM BZX284-C16
6142	4822 130 3084	I2 BAV21
6144	9340 387 3011	5 DIO REG SM BZX284-C16
• • • • •		(PHSE) R
	4822 130 8375	
6146 6151	4822 130 8375 4822 130 3160	67 BAS216 03 1N4006
6152	4822 130 3160 4822 130 3160	3 1N4006 3 1N4006
6153	4822 130 3160 4822 130 3160 4822 130 4260	3 1N4006
6154	4822 130 3160	3 1N4006
6201	4822 130 4260	2 BZX79-B33
6210	4822 130 1159	12 BZX79-B33 16 BYW29EX-200 14 1N4004G 17 DIO REC STPS745FP
6211	5322 130 3457	4 1N4004G
6215	9322 161 4668	7 DIO REC STPS745FP (ST00) L
6220	5322 130 3193	
0004	4000 400 000 4	0. DAVIO4
6230	4822 130 4260	6 BYD33J
6240	4822 130 3414	6 BYW29EX-200
6505	4822 130 3224	5 BYV10-40
6511	4822 130 1166	6 BZX284-C8V2
6515	5322 130 3457 4822 130 3427	4 1N4004G 8 BZX79_B6\/9
6520	4822 130 8375	2 BAV21 6 BYD33J 2 BZX79-B33 6 BYW29EX-200 5 BYV10-40 6 BZX284-C8V2 4 1N4004G 8 BZX79-B6V8 7 BAS216
- C -		
		7 OTDENDOGED
7125 7140	5322 126 6568 5322 130 6015	7 STP5NB60FP 9 BC846B 3 BC856B
7141	4822 130 6037	3 BC856B
7142	5322 130 6015 5322 130 6015	9 BC846B I
7 143	JJZZ 13U 6015	3 DC840B

	-	
7200▲	9322 149 04682	OPT CP TCET1102(G)
		(VISH) L
7220	4822 209 72684	L7905CV
7241	4822 130 60373	BC856B
7251	4822 209 81397	TL431CLPST
7501	9322 163 53685	FET POW SM IRLML2502
l		(INR0) R
7502	4822 209 81397	TL431CLPST
7511	9322 163 53685	FET POW SM IRLML2502
l		(INR0) R
7512	5322 130 60159	BC846B
7515	9322 163 53685	FET POW SM IRLML2502
		(INR0) R
7520	4822 130 11336	STP16NE06FP
7521	4822 209 81397	TL431CLPST